OMAP™

OMAP4430

Multimedia Device

Engineering Sample ES2.0 ES2.1 ES2.2 ES2.3

Version D

Data Manual

TEXAS INSTRUMENTS

PRODUCT PREVIEW

Public Version

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Literature Number: SWPS041D

December 2010–Revised January 2012

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Multimedia Device

Check for Samples: OMAP4430

1 Introduction

NOTE

OMAP™ 4 processors are intended for manufacturers of Smartphones and other mobile devices.

This Data Manual describes the electrical and mechanical specifications of the OMAP4430 processor. It consists of the following sections:

- A description of the device terminals: balls assignments, electrical characteristics, multiplexing modes, and signal descriptions (Section 2)
- A presentation of the required electrical characteristics: absolute maximum ratings, operating conditions, dc characteristics, voltage decoupling capacities, and device power-up and power-down sequences (Section 3)
- The clock specifications: input and output clocks characteristics, PLL and DLL specifications (Section 4)
- The timing requirements and switching characteristics (ac timings) of the video DAC (Section 5)
- The timing requirements and switching characteristics (ac timings) of the interfaces (Section 6)
- A description of thermal resistance characteristics, the device nomenclature, and mechanical data (Section 8)
- The OMAP4430 processor multimedia device PCB guideline (Section A)
- A glossary of the acronyms and abbreviations used in the Data Manual (Section B)

1.1 About This Manual

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A caution statement describes a situation that could potentially damage your software or equipment.

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WARNING

This is an example of a warning statement.

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1.4 History

The following table summarizes the OMAP4430 Public DM versions.

Version	Literature Number	Date	Notes
A	SWPS041A	December 2010	See[1]
B	SWPS041B	December 2010	See[2]
C	SWPS041C	January 2011	See[3]
D	SWPS041D	December 2011	See[4]

(1) *OMAP4430 Multimedia Device Silicon Revision 2.0 2.1 2.2 Data Manual*, public version A (SWPS041A)—Not released to the public domain.

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1.5 Community Resources

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TI Embedded Processors Wiki ***Texas Instruments Embedded Processors Wiki.***
Established to help developers get started with Embedded Processors from Texas Instruments and to foster innovation and growth of general knowledge about the hardware and software surrounding these devices.

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2 Terminal Description

2.1 Terminal Assignments

Figure 2-1 and Figure 2-2 show the ball locations for the 547-ball plastic ball grid array (PBGA) package and are used in conjunction with all tables in this chapter to locate signal names and ball grid numbers.

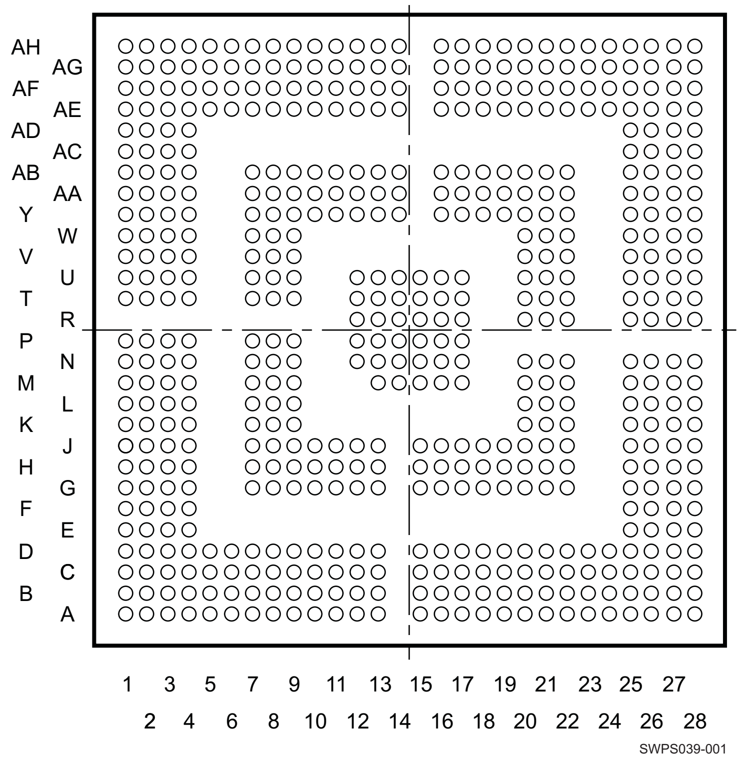

Figure 2-1. S-PBGA-N547 Package (Bottom View)

NOTE

The following bottom balls are unconnected: A28 / B1 / B28 / K21 / K22 / M27 / N27 / T21.

NOTE

The following bottom balls are reserved: C4 / C5 / C6 / D3 / D4 / D5 / D6 / L22 / N7 / H15.

These balls must be left unconnected.

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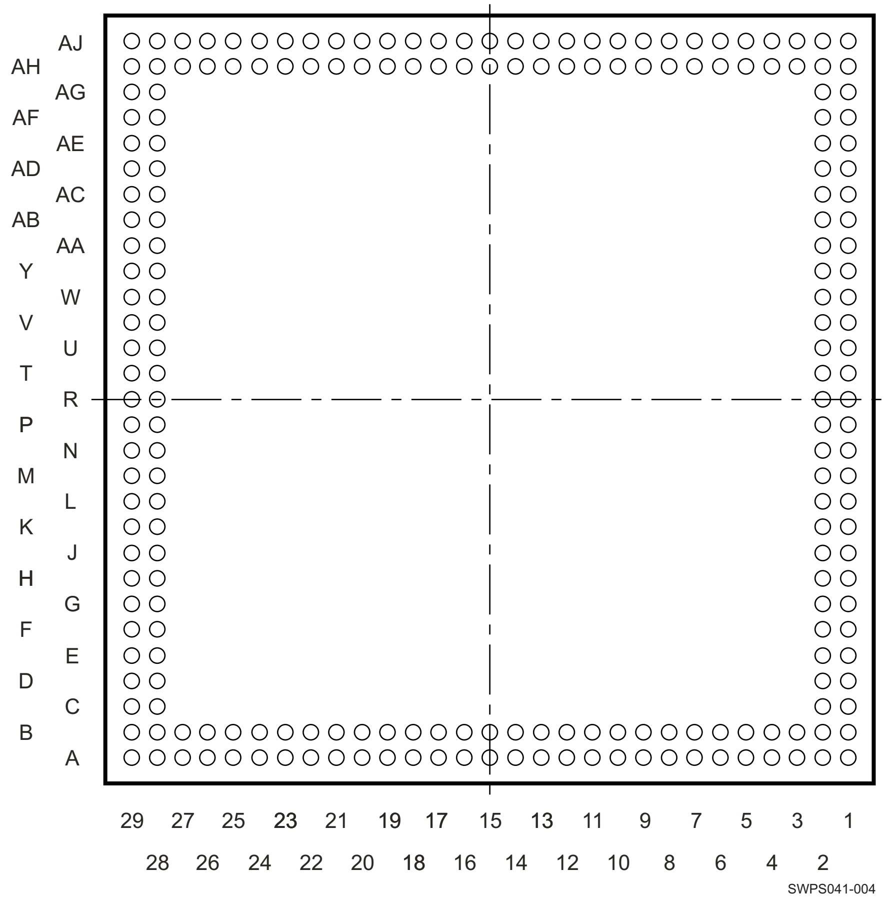

Figure 2-2. S-PBGA-N547 Package (Top View)

NOTE

The following top balls are unconnected: A1 / A29 / AJ1 / AJ29.

2.2 Ball Characteristics

Table 2-1 describes the terminal characteristics and the signals multiplexed on each ball. The following list describes the table column headers:

1. **BALL BOTTOM:** Ball number(s) on the bottom side associated with each signal(s) on the bottom.
2. **BALL TOP:** Ball number(s) on the top side associated with each signal(s) on the top.
3. **PIN NAME:** Names of signals multiplexed on each ball (also notice that the name of the pin is the signal name in mode 0).

NOTE

Table 2-1 doesn't take into account subsystem multiplexing signals. Subsystem multiplexing signals are described in Section 2.4, *Signal Descriptions*.

NOTE

In the safe_mode, the buffer is configured in high-impedance.

4. **MODE:** Multiplexing mode number:
   (a) Mode 0 is the primary mode; this means that when mode 0 is set, the function mapped on the pin

corresponds to the name of the pin. There is always a function mapped on the primary mode. Note that the primary mode is not necessarily the default mode.

NOTE

The default mode is the mode at the release of the reset; also see the RESET REL. MODE column.

(b) Modes 1 to 7 are possible modes for alternate functions. On each pin, some modes are effectively used for alternate functions, while some modes are not used and correspond to a safe mode per design implementation.

5. **TYPE:** Signal type and direction:
   - I = Input
   - O = Output
   - I/O = Input/Output
   - D = Open drain
   - DS = Differential
   - A = Analog
   - PWR = Power
   - GND = Ground
6. **BALL RESET STATE:** The state of the terminal at power-on reset:
   - 0: The buffer drives V_{OL} (pulldown/pullup resistor not activated)
   - 0(PD): The buffer drives V_{OL} with an active pulldown resistor.
   - 1: The buffer drives V_{OH} (pulldown/pullup resistor not activated)
   - 1(PU): The buffer drives V_{OH} with an active pullup resistor.
   - Z: High-impedance
   - L: High-impedance with an active pulldown resistor
   - H: High-impedance with an active pullup resistor
7. **BALL RESET REL. STATE:** The state of the terminal at the release of the System Control Module reset (PRCM CORE_PWRON_RET_RST reset signal).
   - 0: The buffer drives V_{OL} (pulldown/pullup resistor not activated)
   - 0(PD): The buffer drives V_{OL} with an active pulldown resistor.
   - 1: The buffer drives V_{OH} (pulldown/pullup resistor not activated)
   - 1(PU): The buffer drives V_{OH} with an active pullup resistor.
   - Z: High-impedance
   - L: High-impedance with an active pulldown resistor
   - H: High-impedance with an active pullup resistor

NOTE

For more information on the CORE_PWRON_RET_RST reset signal and its reset sources, see the Power Reset and Clock Management / PRCM Reset Management Functional Description section of the OMAP4430 TRM.

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8. **RESET REL. MODE:** This mode is automatically configured at the release of the System Control Module reset (PRCM CORE_PWRON_RET_RST reset signal).

NOTE

For more information on the CORE_PWRON_RET_RST reset signal and its reset sources, see the Power Reset and Clock Management / PRCM Reset Management Functional Description section of the OMAP4430 TRM.

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9. **POWER:** The voltage supply that powers the terminal I/O buffers.

10. **HYS:** Indicates if the input buffer is with hysteresis:
    - Yes: With high hysteresis
    - No: Without low hysteresis

NOTE

The hysteresis value is equal to minimum 150 mV for 1.8 V, or minimum 135 mV for 1.2 V, unless otherwise specified. For more information, see the hysteresis values in Section 3.3, *DC Electrical Characteristics*.

11. **BUFFER STRENGTH:** Drive strength of the associated output buffer.

NOTE

For programmable buffer strength:
- The default value is given in Table 2-1
- A note describes all possible values according to the selected mode.
- The pin is assured to supply up to this amount in steady-state.

12. **PULL U/D – TYPE:** Denotes the presence of an internal pullup or pulldown resistor. Pullup and pulldown resistors can be enabled or disabled via software.

NOTE

The pullup/pulldown drive strength is equal to 100 μA (PU/ PD), unless otherwise specified.

13. **IO CELL:** IO cell information:
    - LVCMOS: The IO buffer receives or drives a standard GPIO signal.
    - Open Drain: The IO buffer outputs an open drain signal.
    - PHY: This is for MIPI D-PHY signals.
    - Analog: For Analog signals
    - SubLVDS: The IO buffer supports the differential mode.
    - Dual Voltage: The IO buffer is designed to support two voltages (for instance, 1.2 V and 1.8 V, or 1.8 V and 3.0 V).

NOTE

Configuring two pins to the same input signal is not supported as it can yield unexpected results. This can be easily prevented with the proper software configuration. (safe_mode is not an input signal.)

NOTE

When a pad is set into a multiplexing mode which is not defined by pin multiplexing, this pad is actually set undriven (HiZ) with potential pullup/pulldown. Pulls need to be disabled to have a pure HiZ.

NOTE

All balls not described in Table 2-1 are not connected.

NOTE

In the OMAP4430 device, new far end load settings registers are added for some IOs. This new feature configures the IO according to the transmission line and the application/peripheral load. For a full description on these registers, see the System Control Module / Programming Model / Feature Settings section of the OMAP4430 TRM.

Table 2-1. Ball Characteristics(1)

BALL BOTTOM [1]	BALL TOP [2]	PIN NAME [3]	MODE [4]	TYPE [5]	BALL RESET STATE [6]	BALL RESET REL. STATE [7]	RESET REL. MODE [8]	POWER [9]	HYS [10]	BUFFER STRENGTH (mA) [11]	PULL U/D TYPE [12]	IO CELL [13]
C12	-	gpmc_ad0	0	IO	H	H	0	vdds_dv_sdmmc2	Yes	6	PU/PD	LVCMOS Dual Voltage
		sdmmc2_dat0	1	IO								
D12	-	gpmc_ad1	0	IO	H	H	0	vdds_dv_sdmmc2	Yes	6	PU/PD	LVCMOS Dual Voltage
		sdmmc2_dat1	1	IO								
C13	-	gpmc_ad2	0	IO	H	H	0	vdds_dv_sdmmc2	Yes	6	PU/PD	LVCMOS Dual Voltage
		sdmmc2_dat2	1	IO								
D13	-	gpmc_ad3	0	IO	H	H	0	vdds_dv_sdmmc2	Yes	6	PU/PD	LVCMOS Dual Voltage
		sdmmc2_dat3	1	IO								
C15	-	gpmc_ad4	0	IO	H	H	0	vdds_dv_sdmmc2	Yes	6	PU/PD	LVCMOS Dual Voltage
		sdmmc2_dat4	1	IO								
		sdmmc2_dir_dat0	2	O								
D15	-	gpmc_ad5	0	IO	H	H	0	vdds_dv_sdmmc2	Yes	6	PU/PD	LVCMOS Dual Voltage
		sdmmc2_dat5	1	IO								
		sdmmc2_dir_dat1	2	O								
A16	-	gpmc_ad6	0	IO	H	H	0	vdds_dv_sdmmc2	Yes	6	PU/PD	LVCMOS Dual Voltage
		sdmmc2_dat6	1	IO								
		sdmmc2_dir_cmd	2	O								
B16	-	gpmc_ad7	0	IO	H	H	0	vdds_dv_sdmmc2	Yes	6	PU/PD	LVCMOS Dual Voltage
		sdmmc2_dat7	1	IO								
		sdmmc2_clk_fdbk	2	I								
C16	-	gpmc_ad8	0	IO	H	H	0	vdds_dv_c2c	Yes	6	PU/PD	LVCMOS Dual Voltage
		kpd_row0	1	I								
		gpio_32	3	IO								
		sdmmc1_dat0	5	IO								
D16	-	gpmc_ad9	0	IO	H	H	0	vdds_dv_c2c	Yes	6	PU/PD	LVCMOS Dual Voltage
		kpd_row1	1	I								
		gpio_33	3	IO								
		sdmmc1_dat1	5	IO								
C17	-	gpmc_ad10	0	IO	H	H	0	vdds_dv_c2c	Yes	6	PU/PD	LVCMOS Dual Voltage
		kpd_row2	1	I								
		gpio_34	3	IO								
		sdmmc1_dat2	5	IO								

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Table 2-1. Ball Characteristics(1) (continued)

BALL BOTTOM [1]	BALL TOP [2]	PIN NAME [3]	MODE [4]	TYPE [5]	BALL RESET STATE [6]	BALL RESET REL. STATE [7]	RESET REL. MODE [8]	POWER [9]	HYS [10]	BUFFER STRENGTH (mA) [11]	PULL U/D TYPE [12]	IO CELL [13]
D17	-	gpmc_ad11	0	IO	H	H	0	vdds_ dv_c2c	Yes	6	PU/ PD	LVCMOS Dual Voltage
		kpd_row3	1	I								
		gpio_35	3	IO								
		sdmmc1_ dat3	5	IO								
C18	-	gpmc_ad12	0	IO	L	L	0	vdds_ dv_c2c	Yes	6	PU/ PD	LVCMOS Dual Voltage Open Drain
		kpd_col0	1	OD								
		gpio_36	3	IO								
		sdmmc1_ dat4	5	IO								
D18	-	gpmc_ad13	0	IO	L	L	0	vdds_ dv_c2c	Yes	6	PU/ PD	LVCMOS Dual Voltage Open Drain
		kpd_col1	1	OD								
		gpio_37	3	IO								
		sdmmc1_ dat5	5	IO								
C19	-	gpmc_ad14	0	IO	L	L	0	vdds_ dv_c2c	Yes	6	PU/ PD	LVCMOS Dual Voltage Open Drain
		kpd_col2	1	OD								
		gpio_38	3	IO								
		sdmmc1_ dat6	5	IO								
D19	-	gpmc_ad15	0	IO	L	L	0	vdds_ dv_c2c	Yes	6	PU/ PD	LVCMOS Dual Voltage Open Drain
		kpd_col3	1	OD								
		gpio_39	3	IO								
		sdmmc1_ dat7	5	IO								
B17	-	gpmc_a16	0	O	L	L	0	vdds_ dv_c2c	Yes	6	PU/ PD	LVCMOS Dual Voltage
		kpd_row4	1	I								
		gpio_40	3	IO								
		venc_656_ data0	4	I								
		safe_mode	7									
A18	-	gpmc_a17	0	O	L	L	7	vdds_ dv_c2c	Yes	6	PU/ PD	LVCMOS Dual Voltage
		kpd_row5	1	I								
		gpio_41	3	IO								
		venc_656_ data1	4	I								
		safe_mode	7									
B18	-	gpmc_a18	0	O	L	L	7	vdds_ dv_c2c	Yes	6	PU/ PD	LVCMOS Dual Voltage
		kpd_row6	1	I								
		gpio_42	3	IO								
		venc_656_ data2	4	I								
		safe_mode	7									

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Table 2-1. Ball Characteristics(1) (continued)

BALL BOTTOM [1]	BALL TOP [2]	PIN NAME [3]	MODE [4]	TYPE [5]	BALL RESET STATE [6]	BALL RESET REL. STATE [7]	RESET REL. MODE [8]	POWER [9]	HYS [10]	BUFFER STRENGTH (mA) [11]	PULL U/D TYPE [12]	IO CELL [13]
A19	-	gpmc_a19	0	O	L	L	7	vdds_dv_c2c	Yes	6	PU/PD	LVCMOS Dual Voltage
		kpd_row7	1	I								
		gpio_43	3	IO								
		venc_656_data3	4	I								
		safe_mode	7									
B19	-	gpmc_a20	0	O	H	L	7	vdds_dv_c2c	Yes	6	PU/PD	LVCMOS Dual Voltage Open Drain
		kpd_col4	1	OD								
		gpio_44	3	IO								
		venc_656_data4	4	I								
		safe_mode	7									
B20	-	gpmc_a21	0	O	H	L	7	vdds_dv_c2c	Yes	6	PU/PD	LVCMOS Dual Voltage Open Drain
		kpd_col5	1	OD								
		gpio_45	3	IO								
		venc_656_data5	4	I								
		safe_mode	7									
A21	-	gpmc_a22	0	O	H	L	7	vdds_dv_c2c	Yes	6	PU/PD	LVCMOS Dual Voltage Open Drain
		kpd_col6	1	OD								
		gpio_46	3	IO								
		venc_656_data6	4	I								
		safe_mode	7									
B21	-	gpmc_a23	0	O	H	L	7	vdds_dv_c2c	Yes	6	PU/PD	LVCMOS Dual Voltage Open Drain
		kpd_col7	1	OD								
		gpio_47	3	IO								
		venc_656_data7	4	I								
		safe_mode	7									
C20	-	gpmc_a24	0	O	H	L	7	vdds_dv_c2c	Yes	6	PU/PD	LVCMOS Dual Voltage Open Drain
		kpd_col8	1	OD								
		gpio_48	3	IO								
		safe_mode	7									
D20	-	gpmc_a25	0	O	H	L	7	vdds_dv_c2c	Yes	6	PU/PD	LVCMOS Dual Voltage
		gpio_49	3	IO								
		safe_mode	7									
B25	-	gpmc_ncs0	0	O	H	1	0	vdds_dv_gpmc	Yes	6	PU/PD	LVCMOS Dual Voltage
		gpio_50	3	IO								
		sys_ndmareq0	4	I								
C21	-	gpmc_ncs1	0	O	H	H	7	vdds_dv_c2c	Yes	6	PU/PD	LVCMOS Dual Voltage
		gpio_51	3	IO								
		safe_mode	7									

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Table 2-1. Ball Characteristics(1) (continued)

BALL BOTTOM [1]	BALL TOP [2]	PIN NAME [3]	MODE [4]	TYPE [5]	BALL RESET STATE [6]	BALL RESET REL. STATE [7]	RESET REL. MODE [8]	POWER [9]	HYS [10]	BUFFER STRENGTH (mA) [11]	PULL U/D TYPE [12]	IO CELL [13]
D21	-	gpmc_ncs2	0	O	H	H	7	vdds_dv_c2c	Yes	6	PU/PD	LVCMOS Dual Voltage
		kpd_row8	1	I								
		gpio_52	3	IO								
		safe_mode	7									
C22	-	gpmc_ncs3	0	O	H	H	7	vdds_dv_c2c	Yes	6	PU/PD	LVCMOS Dual Voltage
		gpmc_dir	1	O								
		gpio_53	3	IO								
		safe_mode	7									
C25	-	gpmc_nwp	0	O	L	0	0	vdds_dv_gpmc	Yes	4	PU/PD	LVCMOS Dual Voltage SubLVDS
		dsi1_te0	1	IDS								
		gpio_54	3	IO								
		sys_ndmareq1	4	I								
B22	-	gpmc_clk	0	O	L	0	0	vdds_dv_gpmc	Yes	6	PU/PD	LVCMOS Dual Voltage
		gpio_55	3	IO								
		sys_ndmareq2	4	I								
		sdmmc1_cmd	5	IO								
D25	-	gpmc_nadv_ale	0	O	L	0	0	vdds_dv_gpmc	Yes	6	PU/PD	LVCMOS Dual Voltage SubLVDS
		dsi1_te1	1	IDS								
		gpio_56	3	IO								
		sys_ndmareq3	4	I								
		sdmmc1_clk	5	O								
B11	-	gpmc_noe	0	O	H	1	0	vdds_dv_sdmmc2	Yes	6	PU/PD	LVCMOS Dual Voltage
		sdmmc2_clk	1	O								
B12	-	gpmc_nwe	0	O	H	1	0	vdds_dv_sdmmc2	Yes	6	PU/PD	LVCMOS Dual Voltage
		sdmmc2_cmd	1	IO								
C23	-	gpmc_nbe0_cle	0	O	L	0	0	vdds_dv_gpmc	Yes	6	PU/PD	LVCMOS Dual Voltage SubLVDS
		dsi2_te0	1	IDS								
		gpio_59	3	IO								
D22	-	gpmc_nbe1	0	O	L	L	7	vdds_dv_c2c	Yes	6	PU/PD	LVCMOS Dual Voltage
		gpio_60	3	IO								
		safe_mode	7									
B26	-	gpmc_wait0	0	I	H	H	0	vdds_dv_gpmc	Yes	4	PU/PD	LVCMOS Dual Voltage SubLVDS
		dsi2_te1	1	IDS								
		gpio_61	3	IO								
B23	-	gpmc_wait1	0	I	H	H	7	vdds_dv_c2c	Yes	6	PU/PD	LVCMOS Dual Voltage
		gpio_62	3	IO								
		safe_mode	7									

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Table 2-1. Ball Characteristics(1) (continued)

BALL BOTTOM [1]	BALL TOP [2]	PIN NAME [3]	MODE [4]	TYPE [5]	BALL RESET STATE [6]	BALL RESET REL. STATE [7]	RESET REL. MODE [8]	POWER [9]	HYS [10]	BUFFER STRENGTH (mA) [11]	PULL U/D TYPE [12]	IO CELL [13]
D23	-	gpmc_wait2	0	I	L	L	7	vdds_dv_c2c	Yes	6	PU/PD	LVCMOS Dual Voltage
		usbc1_icusb_txen	1	O								
		gpio_100	3	IO								
		sys_ndmareq0	4	I								
		safe_mode	7									
A24	-	gpmc_ncs4	0	O	L	L	7	vdds_dv_c2c	Yes	6	PU/PD	LVCMOS Dual Voltage SubLVDS
		dsi1_te0	1	IDS								
		gpio_101	3	IO								
		sys_ndmareq1	4	I								
		safe_mode	7									
B24	-	gpmc_ncs5	0	O	L	L	7	vdds_dv_c2c	Yes	6	PU/PD	LVCMOS Dual Voltage SubLVDS
		dsi1_te1	1	IDS								
		gpio_102	3	IO								
		sys_ndmareq2	4	I								
		safe_mode	7									
C24	-	gpmc_ncs6	0	O	L	L	7	vdds_dv_c2c	Yes	6	PU/PD	LVCMOS Dual Voltage SubLVDS
		dsi2_te0	1	IDS								
		gpio_103	3	IO								
		sys_ndmareq3	4	I								
		safe_mode	7									
D24	-	gpmc_ncs7	0	O	L	L	7	vdds_dv_c2c	Yes	6	PU/PD	LVCMOS Dual Voltage SubLVDS
		dsi2_te1	1	IDS								
		gpio_104	3	IO								
		safe_mode	7									
-	E29	lpddr21_dq0	0	IO	L	L	0	vddq_lpddr2	NA	0.1	PUy/PDy(2)	LVCMOS
-	D28	lpddr21_dq1	0	IO	L	L	0	vddq_lpddr2	NA	0.1	PUy/PDy(2)	LVCMOS
-	B27	lpddr21_dq2	0	IO	L	L	0	vddq_lpddr2	NA	0.1	PUy/PDy(2)	LVCMOS
-	A27	lpddr21_dq3	0	IO	L	L	0	vddq_lpddr2	NA	0.1	PUy/PDy(2)	LVCMOS
-	A26	lpddr21_dq4	0	IO	L	L	0	vddq_lpddr2	NA	0.1	PUy/PDy(2)	LVCMOS
-	B26	lpddr21_dq5	0	IO	L	L	0	vddq_lpddr2	NA	0.1	PUy/PDy(2)	LVCMOS
-	A25	lpddr21_dq6	0	IO	L	L	0	vddq_lpddr2	NA	0.1	PUy/PDy(2)	LVCMOS
-	A24	lpddr21_dq7	0	IO	L	L	0	vddq_lpddr2	NA	0.1	PUy/PDy(2)	LVCMOS
-	B19	lpddr21_dq8	0	IO	L	L	0	vddq_lpddr2	NA	0.1	PUy/PDy(2)	LVCMOS
-	A19	lpddr21_dq9	0	IO	L	L	0	vddq_lpddr2	NA	0.1	PUy/PDy(2)	LVCMOS

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Table 2-1. Ball Characteristics(1) (continued)

BALL BOTTOM [1]	BALL TOP [2]	PIN NAME [3]	MODE [4]	TYPE [5]	BALL RESET STATE [6]	BALL RESET REL. STATE [7]	RESET REL. MODE [8]	POWER [9]	HYS [10]	BUFFER STRENGTH (mA) [11]	PULL U/D TYPE [12]	IO CELL [13]
-	A18	lpddr21_dq10	0	IO	L	L	0	vddq_ lpddr2	NA	0.1	PUy/ PDy(2)	LVCMOS
-	A17	lpddr21_dq11	0	IO	L	L	0	vddq_ lpddr2	NA	0.1	PUy/ PDy(2)	LVCMOS
-	B17	lpddr21_dq12	0	IO	L	L	0	vddq_ lpddr2	NA	0.1	PUy/ PDy(2)	LVCMOS
-	A13	lpddr21_dq13	0	IO	L	L	0	vddq_ lpddr2	NA	0.1	PUy/ PDy(2)	LVCMOS
-	A12	lpddr21_dq14	0	IO	L	L	0	vddq_ lpddr2	NA	0.1	PUy/ PDy(2)	LVCMOS
-	B12	lpddr21_dq15	0	IO	L	L	0	vddq_ lpddr2	NA	0.1	PUy/ PDy(2)	LVCMOS
-	N28	lpddr21_dq16	0	IO	L	L	0	vddq_ lpddr2	NA	0.1	PUy/ PDy(2)	LVCMOS
-	N29	lpddr21_dq17	0	IO	L	L	0	vddq_ lpddr2	NA	0.1	PUy/ PDy(2)	LVCMOS
-	M29	lpddr21_dq18	0	IO	L	L	0	vddq_ lpddr2	NA	0.1	PUy/ PDy(2)	LVCMOS
-	L28	lpddr21_dq19	0	IO	L	L	0	vddq_ lpddr2	NA	0.1	PUy/ PDy(2)	LVCMOS
-	K28	lpddr21_dq20	0	IO	L	L	0	vddq_ lpddr2	NA	0.1	PUy/ PDy(2)	LVCMOS
-	K29	lpddr21_dq21	0	IO	L	L	0	vddq_ lpddr2	NA	0.1	PUy/ PDy(2)	LVCMOS
-	J29	lpddr21_dq22	0	IO	L	L	0	vddq_ lpddr2	NA	0.1	PUy/ PDy(2)	LVCMOS
-	H29	lpddr21_dq23	0	IO	L	L	0	vddq_ lpddr2	NA	0.1	PUy/ PDy(2)	LVCMOS
-	B8	lpddr21_dq24	0	IO	L	L	0	vddq_ lpddr2	NA	0.1	PUy/ PDy(2)	LVCMOS
-	A8	lpddr21_dq25	0	IO	L	L	0	vddq_ lpddr2	NA	0.1	PUy/ PDy(2)	LVCMOS
-	A7	lpddr21_dq26	0	IO	L	L	0	vddq_ lpddr2	NA	0.1	PUy/ PDy(2)	LVCMOS
-	B6	lpddr21_dq27	0	IO	L	L	0	vddq_ lpddr2	NA	0.1	PUy/ PDy(2)	LVCMOS
-	B5	lpddr21_dq28	0	IO	L	L	0	vddq_ lpddr2	NA	0.1	PUy/ PDy(2)	LVCMOS
-	A5	lpddr21_dq29	0	IO	L	L	0	vddq_ lpddr2	NA	0.1	PUy/ PDy(2)	LVCMOS
-	A4	lpddr21_dq30	0	IO	L	L	0	vddq_ lpddr2	NA	0.1	PUy/ PDy(2)	LVCMOS
-	B3	lpddr21_dq31	0	IO	L	L	0	vddq_ lpddr2	NA	0.1	PUy/ PDy(2)	LVCMOS
-	AJ27	lpddr21_ca0	0	O	L	L	0	vddca_ lpddr21	NA	0.1	PUy/ PDy(2)	LVCMOS
-	AH27	lpddr21_ca1	0	O	L	L	0	vddca_ lpddr21	NA	0.1	PUy/ PDy(2)	LVCMOS
-	AH26	lpddr21_ca2	0	O	L	L	0	vddca_ lpddr21	NA	0.1	PUy/ PDy(2)	LVCMOS
-	AH25	lpddr21_ca3	0	O	L	L	0	vddca_ lpddr21	NA	0.1	PUy/ PDy(2)	LVCMOS
-	AJ25	lpddr21_ca4	0	O	L	L	0	vddca_ lpddr21	NA	0.1	PUy/ PDy(2)	LVCMOS

Table 2-1. Ball Characteristics(1) (continued)

BALL BOTTOM [1]	BALL TOP [2]	PIN NAME [3]	MODE [4]	TYPE [5]	BALL RESET STATE [6]	BALL RESET REL. STATE [7]	RESET REL. MODE [8]	POWER [9]	HYS [10]	BUFFER STRENGTH (mA) [11]	PULL U/D TYPE [12]	IO CELL [13]
-	AJ20	lpddr21_ca5	0	O	L	L	0	vddca_ lpddr21	NA	0.1	PUy/ PDy(2)	LVCMOS
-	AH20	lpddr21_ca6	0	O	L	L	0	vddca_ lpddr21	NA	0.1	PUy/ PDy(2)	LVCMOS
-	AH19	lpddr21_ca7	0	O	L	L	0	vddca_ lpddr21	NA	0.1	PUy/ PDy(2)	LVCMOS
-	AJ18	lpddr21_ca8	0	O	L	L	0	vddca_ lpddr21	NA	0.1	PUy/ PDy(2)	LVCMOS
-	AH17	lpddr21_ca9	0	O	L	L	0	vddca_ lpddr21	NA	0.1	PUy/ PDy(2)	LVCMOS
-	A23	lpddr21_dqs0	0	IO	L	L	0	vddq_ lpddr2	NA	0.1	PUy/ PDy(3)	LVCMOS
-	B23	lpddr21_ ndqs0	0	IO	H	H	0	vddq_ lpddr2	NA	0.1	PUy/ PDy(3)	LVCMOS
-	A20	lpddr21_dqs1	0	IO	L	L	0	vddq_ lpddr2	NA	0.1	PUy/ PDy(3)	LVCMOS
-	B20	lpddr21_ ndqs1	0	IO	H	H	0	vddq_ lpddr2	NA	0.1	PUy/ PDy(3)	LVCMOS
-	G28	lpddr21_dqs2	0	IO	L	L	0	vddq_ lpddr2	NA	0.1	PUy/ PDy(3)	LVCMOS
-	G29	lpddr21_ ndqs2	0	IO	H	H	0	vddq_ lpddr2	NA	0.1	PUy/ PDy(3)	LVCMOS
-	B10	lpddr21_dqs3	0	IO	L	L	0	vddq_ lpddr2	NA	0.1	PUy/ PDy(3)	LVCMOS
-	A10	lpddr21_ ndqs3	0	IO	H	H	0	vddq_ lpddr2	NA	0.1	PUy/ PDy(3)	LVCMOS
-	B22	lpddr21_dm0	0	IO	L	L	0	vddq_ lpddr2	NA	0.1	PUy/ PDy(2)	LVCMOS
-	A21	lpddr21_dm1	0	IO	L	L	0	vddq_ lpddr2	NA	0.1	PUy/ PDy(2)	LVCMOS
-	F28	lpddr21_dm2	0	IO	L	L	0	vddq_ lpddr2	NA	0.1	PUy/ PDy(2)	LVCMOS
-	B11	lpddr21_dm3	0	IO	L	L	0	vddq_ lpddr2	NA	0.1	PUy/ PDy(2)	LVCMOS
-	AJ21	lpddr21_ck	0	O	L	L	0	vddca_ lpddr21	NA	0.1	PUy/ PDy(3)	LVCMOS
-	AH21	lpddr21_nck	0	O	H	H	0	vddca_ lpddr21	NA	0.1	PUy/ PDy(3)	LVCMOS
AH28	AH24	lpddr21_ncs0	0	O	L	L	0	vddca_ lpddr21	NA	0.1	PUy/ PDy(2)	LVCMOS
-	AJ24	lpddr21_ncs1	0	O	L	L	0	vddca_ lpddr21	NA	0.1	PUy/ PDy(2)	LVCMOS
-	AH23	lpddr21_cke0	0	O	L	L	0	vddca_ lpddr21	NA	0.1	PUy/ PDy(2)	LVCMOS
-	AJ23	lpddr21_cke1	0	O	L	L	0	vddca_ lpddr21	NA	0.1	PUy/ PDy(2)	LVCMOS
-	AH16	lpddr21_vref_ ca	0	PWR	Z	NA	0	vddca_ vref_ lpddr21	No	NA	See(4)	NA
-	B15	lpddr21_vref_ dq	0	PWR	Z	NA	0	vddq_ vref_ lpddr21	No	NA	See(4)	NA
-	L2	lpddr22_dq0	0	IO	L	L	0	vddq_ lpddr2	NA	0.1	PUy/ PDy(2)	LVCMOS

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Table 2-1. Ball Characteristics(1) (continued)

BALL BOTTOM [1]	BALL TOP [2]	PIN NAME [3]	MODE [4]	TYPE [5]	BALL RESET STATE [6]	BALL RESET REL. STATE [7]	RESET REL. MODE [8]	POWER [9]	HYS [10]	BUFFER STRENGTH (mA) [11]	PULL U/D TYPE [12]	IO CELL [13]
-	M1	lpddr22_dq1	0	IO	L	L	0	vddq_ lpddr2	NA	0.1	PUy/ PDy(2)	LVCMOS
-	N1	lpddr22_dq2	0	IO	L	L	0	vddq_ lpddr2	NA	0.1	PUy/ PDy(2)	LVCMOS
-	U2	lpddr22_dq3	0	IO	L	L	0	vddq_ lpddr2	NA	0.1	PUy/ PDy(2)	LVCMOS
-	V1	lpddr22_dq4	0	IO	L	L	0	vddq_ lpddr2	NA	0.1	PUy/ PDy(2)	LVCMOS
-	W2	lpddr22_dq5	0	IO	L	L	0	vddq_ lpddr2	NA	0.1	PUy/ PDy(2)	LVCMOS
-	W1	lpddr22_dq6	0	IO	L	L	0	vddq_ lpddr2	NA	0.1	PUy/ PDy(2)	LVCMOS
-	Y2	lpddr22_dq7	0	IO	L	L	0	vddq_ lpddr2	NA	0.1	PUy/ PDy(2)	LVCMOS
-	AE1	lpddr22_dq8	0	IO	L	L	0	vddq_ lpddr2	NA	0.1	PUy/ PDy(2)	LVCMOS
-	AF1	lpddr22_dq9	0	IO	L	L	0	vddq_ lpddr2	NA	0.1	PUy/ PDy(2)	LVCMOS
-	AG1	lpddr22_dq10	0	IO	L	L	0	vddq_ lpddr2	NA	0.1	PUy/ PDy(2)	LVCMOS
-	AG2	lpddr22_dq11	0	IO	L	L	0	vddq_ lpddr2	NA	0.1	PUy/ PDy(2)	LVCMOS
-	AJ3	lpddr22_dq12	0	IO	L	L	0	vddq_ lpddr2	NA	0.1	PUy/ PDy(2)	LVCMOS
-	AH4	lpddr22_dq13	0	IO	L	L	0	vddq_ lpddr2	NA	0.1	PUy/ PDy(2)	LVCMOS
-	AJ5	lpddr22_dq14	0	IO	L	L	0	vddq_ lpddr2	NA	0.1	PUy/ PDy(2)	LVCMOS
-	AH6	lpddr22_dq15	0	IO	L	L	0	vddq_ lpddr2	NA	0.1	PUy/ PDy(2)	LVCMOS
-	C2	lpddr22_dq16	0	IO	L	L	0	vddq_ lpddr2	NA	0.1	PUy/ PDy(2)	LVCMOS
-	D1	lpddr22_dq17	0	IO	L	L	0	vddq_ lpddr2	NA	0.1	PUy/ PDy(2)	LVCMOS
-	E1	lpddr22_dq18	0	IO	L	L	0	vddq_ lpddr2	NA	0.1	PUy/ PDy(2)	LVCMOS
-	E2	lpddr22_dq19	0	IO	L	L	0	vddq_ lpddr2	NA	0.1	PUy/ PDy(2)	LVCMOS
-	F2	lpddr22_dq20	0	IO	L	L	0	vddq_ lpddr2	NA	0.1	PUy/ PDy(2)	LVCMOS
-	G1	lpddr22_dq21	0	IO	L	L	0	vddq_ lpddr2	NA	0.1	PUy/ PDy(2)	LVCMOS
-	H1	lpddr22_dq22	0	IO	L	L	0	vddq_ lpddr2	NA	0.1	PUy/ PDy(2)	LVCMOS
-	H2	lpddr22_dq23	0	IO	L	L	0	vddq_ lpddr2	NA	0.1	PUy/ PDy(2)	LVCMOS
-	AJ9	lpddr22_dq24	0	IO	L	L	0	vddq_ lpddr2	NA	0.1	PUy/ PDy(2)	LVCMOS
-	AJ10	lpddr22_dq25	0	IO	L	L	0	vddq_ lpddr2	NA	0.1	PUy/ PDy(2)	LVCMOS
-	AH10	lpddr22_dq26	0	IO	L	L	0	vddq_ lpddr2	NA	0.1	PUy/ PDy(2)	LVCMOS
-	AH11	lpddr22_dq27	0	IO	L	L	0	vddq_ lpddr2	NA	0.1	PUy/ PDy(2)	LVCMOS

Table 2-1. Ball Characteristics(1) (continued)

BALL BOTTOM [1]	BALL TOP [2]	PIN NAME [3]	MODE [4]	TYPE [5]	BALL RESET STATE [6]	BALL RESET REL. STATE [7]	RESET REL. MODE [8]	POWER [9]	HYS [10]	BUFFER STRENGTH (mA) [11]	PULL U/D TYPE [12]	IO CELL [13]
-	AJ12	lpddr22_dq28	0	IO	L	L	0	vddq_ lpddr2	NA	0.1	PUy/ PDy(2)	LVCMOS
-	AJ13	lpddr22_dq29	0	IO	L	L	0	vddq_ lpddr2	NA	0.1	PUy/ PDy(2)	LVCMOS
-	AH13	lpddr22_dq30	0	IO	L	L	0	vddq_ lpddr2	NA	0.1	PUy/ PDy(2)	LVCMOS
-	AJ14	lpddr22_dq31	0	IO	L	L	0	vddq_ lpddr2	NA	0.1	PUy/ PDy(2)	LVCMOS
-	R29	lpddr22_ca0	0	O	L	L	0	vddca_ lpddr22	NA	0.1	PUy/ PDy(2)	LVCMOS
-	T29	lpddr22_ca1	0	O	L	L	0	vddca_ lpddr22	NA	0.1	PUy/ PDy(2)	LVCMOS
-	U29	lpddr22_ca2	0	O	L	L	0	vddca_ lpddr22	NA	0.1	PUy/ PDy(2)	LVCMOS
-	V29	lpddr22_ca3	0	O	L	L	0	vddca_ lpddr22	NA	0.1	PUy/ PDy(2)	LVCMOS
-	W28	lpddr22_ca4	0	O	L	L	0	vddca_ lpddr22	NA	0.1	PUy/ PDy(2)	LVCMOS
-	AC29	lpddr22_ca5	0	O	L	L	0	vddca_ lpddr22	NA	0.1	PUy/ PDy(2)	LVCMOS
-	AD29	lpddr22_ca6	0	O	L	L	0	vddca_ lpddr22	NA	0.1	PUy/ PDy(2)	LVCMOS
-	AD28	lpddr22_ca7	0	O	L	L	0	vddca_ lpddr22	NA	0.1	PUy/ PDy(2)	LVCMOS
-	AE28	lpddr22_ca8	0	O	L	L	0	vddca_ lpddr22	NA	0.1	PUy/ PDy(2)	LVCMOS
-	AF29	lpddr22_ca9	0	O	L	L	0	vddca_ lpddr22	NA	0.1	PUy/ PDy(2)	LVCMOS
-	AA1	lpddr22_dqs0	0	O	L	L	0	vddq_ lpddr2	NA	0.1	PUy/ PDy(3)	LVCMOS
-	AA2	lpddr22_ ndqs0	0	O	H	H	0	vddq_ lpddr2	NA	0.1	PUy/ PDy(3)	LVCMOS
-	AD2	lpddr22_dqs1	0	O	L	L	0	vddq_ lpddr2	NA	0.1	PUy/ PDy(3)	LVCMOS
-	AD1	lpddr22_ ndqs1	0	O	H	H	0	vddq_ lpddr2	NA	0.1	PUy/ PDy(3)	LVCMOS
-	K2	lpddr22_dqs2	0	O	L	L	0	vddq_ lpddr2	NA	0.1	PUy/ PDy(3)	LVCMOS
-	K1	lpddr22_ ndqs2	0	O	H	H	0	vddq_ lpddr2	NA	0.1	PUy/ PDy(3)	LVCMOS
-	AH8	lpddr22_dqs3	0	O	L	L	0	vddq_ lpddr2	NA	0.1	PUy/ PDy(3)	LVCMOS
-	AJ8	lpddr22_ ndqs3	0	O	H	H	0	vddq_ lpddr2	NA	0.1	PUy/ PDy(3)	LVCMOS
-	AB1	lpddr22_dm0	0	IO	L	L	0	vddq_ lpddr2	NA	0.1	PUy/ PDy(2)	LVCMOS
-	AC2	lpddr22_dm1	0	IO	L	L	0	vddq_ lpddr2	NA	0.1	PUy/ PDy(2)	LVCMOS
-	L1	lpddr22_dm2	0	IO	L	L	0	vddq_ lpddr2	NA	0.1	PUy/ PDy(2)	LVCMOS
-	AH7	lpddr22_dm3	0	IO	L	L	0	vddq_ lpddr2	NA	0.1	PUy/ PDy(2)	LVCMOS
-	AB28	lpddr22_ck	0	O	L	L	0	vddca_ lpddr22	NA	0.1	PUy/ PDy(3)	LVCMOS

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Table 2-1. Ball Characteristics(1) (continued)

BALL BOTTOM [1]	BALL TOP [2]	PIN NAME [3]	MODE [4]	TYPE [5]	BALL RESET STATE [6]	BALL RESET REL. STATE [7]	RESET REL. MODE [8]	POWER [9]	HYS [10]	BUFFER STRENGTH (mA) [11]	PULL U/D TYPE [12]	IO CELL [13]
-	AB29	lpddr22_nck	0	O	H	H	0	vddca_ lpddr22	NA	0.1	PUy/ PDy(3)	LVCMOS
-	Y28	lpddr22_ncs0	0	O	L	L	0	vddca_ lpddr22	NA	0.1	PUy/ PDy(2)	LVCMOS
-	W29	lpddr22_ncs1	0	O	L	L	0	vddca_ lpddr22	NA	0.1	PUy/ PDy(2)	LVCMOS
-	AA29	lpddr22_cke0	0	O	L	L	0	vddca_ lpddr22	NA	0.1	PUy/ PDy(2)	LVCMOS
-	Y29	lpddr22_cke1	0	O	L	L	0	vddca_ lpddr22	NA	0.1	PUy/ PDy(2)	LVCMOS
-	U28	lpddr22_vref_ ca	0	PWR	Z	NA	0	vddca_ vref_ lpddr22	No	NA	See(4)	NA
-	R2	lpddr22_vref_ dq	0	PWR	Z	NA	0	vddq_ vref_ lpddr22	No	NA	See(4)	NA
P3	-	dsi1_dx0	0	IODS	0	0	0	vdda_ dsi1(24)	NA	See(12)	PU/ PD	PHY SubLVDS
P4	-	dsi1_dy0	0	IODS	0	0	0	vdda_ dsi1(24)	NA	See(12)	PU/ PD	PHY SubLVDS
N3	-	dsi1_dx1	0	IODS	0	0	0	vdda_ dsi1(24)	NA	See(12)	PU/ PD	PHY SubLVDS
N4	-	dsi1_dy1	0	IODS	0	0	0	vdda_ dsi1(24)	NA	See(12)	PU/ PD	PHY SubLVDS
M3	-	dsi1_dx2	0	IODS	0	0	0	vdda_ dsi1(24)	NA	See(12)	PU/ PD	PHY SubLVDS
M4	-	dsi1_dy2	0	IODS	0	0	0	vdda_ dsi1(24)	NA	See(12)	PU/ PD	PHY SubLVDS
L3	-	dsi1_dx3	0	IODS	0	0	0	vdda_ dsi1(24)	NA	See(12)	PU/ PD	PHY SubLVDS
L4	-	dsi1_dy3	0	IODS	0	0	0	vdda_ dsi1(24)	NA	See(12)	PU/ PD	PHY SubLVDS
K3	-	dsi1_dx4	0	IODS	0	0	0	vdda_ dsi1(24)	NA	See(12)	PU/ PD	PHY SubLVDS
K4	-	dsi1_dy4	0	IODS	0	0	0	vdda_ dsi1(24)	NA	See(12)	PU/ PD	PHY SubLVDS
T3	-	dsi2_dx0	0	IODS	0	0	0	vdda_ dsi2(24)	NA	See(12)	PU/ PD	PHY SubLVDS
T4	-	dsi2_dy0	0	IODS	0	0	0	vdda_ dsi2(24)	NA	See(12)	PU/ PD	PHY SubLVDS
U3	-	dsi2_dx1	0	IODS	0	0	0	vdda_ dsi2(24)	NA	See(12)	PU/ PD	PHY SubLVDS
U4	-	dsi2_dy1	0	IODS	0	0	0	vdda_ dsi2(24)	NA	See(12)	PU/ PD	PHY SubLVDS
V3	-	dsi2_dx2	0	IODS	0	0	0	vdda_ dsi2(24)	NA	See(12)	PU/ PD	PHY SubLVDS
V4	-	dsi2_dy2	0	IODS	0	0	0	vdda_ dsi2(24)	NA	See(12)	PU/ PD	PHY SubLVDS
B7	-	cvideo_tvout	0	AO	Z	NA	0	vdda_ hdmi_ vdac(25)	NA	NA(7)	NA	Analog
C7	-	cvideo_vfb	0	AO	Z	NA	0	vdda_ hdmi_ vdac(25)	NA	NA(8)	NA	Analog

Table 2-1. Ball Characteristics[(1)] (continued)

BALL BOTTOM [1]	BALL TOP [2]	PIN NAME [3]	MODE [4]	TYPE [5]	BALL RESET STATE [6]	BALL RESET REL. STATE [7]	RESET REL. MODE [8]	POWER [9]	HYS [10]	BUFFER STRENGTH (mA) [11]	PULL U/D TYPE [12]	IO CELL [13]
D7	-	cvideo_rset	0	AIO	Z	NA	0	vdda_ hdmi_ vdac(25)	NA	NA	NA	LVCMOS Analog
B9	-	hdmi_hpd	0	I	L	L	7	vdds_ 1p8v	Yes	4	PU/ PD	LVCMOS
		gpio_63	3	IO								
		safe_mode	7									
B10	-	hdmi_cec	0	IO	H	H	7	vdds_ 1p8v	Yes	4	PU/ PD	LVCMOS
		gpio_64	3	IO								
		safe_mode	7									
A8	-	hdmi_ddc_scl	0	OD	H	H	7	vdds_ 1p8v	Yes	3	PUx/ PDy- GPIO	LVCMOS Open Drain
		gpio_65	3	IO						4		
		safe_mode	7							4		
B8	-	hdmi_ddc_ sda	0	IOD	H	H	7	vdds_ 1p8v	Yes	3	PUx/ PDy- GPIO	LVCMOS Open Drain
		gpio_66	3	IO						4		
		safe_mode	7							4		
C8	-	hdmi_data2x (29)	0	ODS	Z	Z	0	vdda_ hdmi_ vdac(25)	NA	See(13)	PD(30)	PHY SubLVDS FS
D8	-	hdmi_data2y (29)	0	ODS	Z	Z	0	vdda_ hdmi_ vdac(25)	NA	See(13)	PD(30)	PHY SubLVDS FS
C9	-	hdmi_data1x (29)	0	ODS	Z	Z	0	vdda_ hdmi_ vdac(25)	NA	See(13)	PD(30)	PHY SubLVDS FS
D9	-	hdmi_data1y (29)	0	ODS	Z	Z	0	vdda_ hdmi_ vdac(25)	NA	See(13)	PD(30)	PHY SubLVDS FS
C10	-	hdmi_data0x (29)	0	ODS	Z	Z	0	vdda_ hdmi_ vdac(25)	NA	See(13)	PD(30)	PHY SubLVDS FS
D10	-	hdmi_data0y (29)	0	ODS	Z	Z	0	vdda_ hdmi_ vdac(25)	NA	See(13)	PD(30)	PHY SubLVDS FS
C11	-	hdmi_clockx (29)	0	ODS	Z	Z	0	vdda_ hdmi_ vdac(25)	NA	See(13)	PD(30)	PHY SubLVDS FS
D11	-	hdmi_clocky (29)	0	ODS	Z	Z	0	vdda_ hdmi_ vdac(25)	NA	See(13)	PD(30)	PHY SubLVDS FS
R26	-	csi21_dx0	0	IDS	L	L	7	vdda_ csi21(23)	Yes (19)	NA	PU/ PD	PHY SubLVDS LVCMOS
		gpi_67	3	I								
		safe_mode	7									
R25	-	csi21_dy0	0	IDS	L	L	7	vdda_ csi21(23)	Yes (19)	NA	PU/ PD	PHY SubLVDS LVCMOS
		gpi_68	3	I								
		safe_mode	7									
T26	-	csi21_dx1	0	IDS	L	L	7	vdda_ csi21(23)	Yes (19)	NA	PU/ PD	PHY SubLVDS LVCMOS
		gpi_69	3	I								
		safe_mode	7									

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Table 2-1. Ball Characteristics[(1)] (continued)

BALL BOTTOM [1]	BALL TOP [2]	PIN NAME [3]	MODE [4]	TYPE [5]	BALL RESET STATE [6]	BALL RESET REL. STATE [7]	RESET REL. MODE [8]	POWER [9]	HYS [10]	BUFFER STRENGTH (mA) [11]	PULL U/D TYPE [12]	IO CELL [13]
T25	-	csi21_dy1	0	IDS	L	L	7	vdda csi21[(23)]	Yes [(19)]	NA	PU/ PD	PHY SubLVDS LVCMOS
		gpi_70	3	I								
		safe_mode	7									
U26	-	csi21_dx2	0	IDS	L	L	7	vdda csi21[(23)]	Yes [(19)]	NA	PU/ PD	PHY SubLVDS LVCMOS
		gpi_71	3	I								
		safe_mode	7									
U25	-	csi21_dy2	0	IDS	L	L	7	vdda csi21[(23)]	Yes [(19)]	NA	PU/ PD	PHY SubLVDS LVCMOS
		gpi_72	3	I								
		safe_mode	7									
V26	-	csi21_dx3	0	IDS	L	L	7	vdda csi21[(23)]	Yes [(19)]	NA	PU/ PD	PHY SubLVDS LVCMOS
		gpi_73	3	I								
		safe_mode	7									
V25	-	csi21_dy3	0	IDS	L	L	7	vdda csi21[(23)]	Yes [(19)]	NA	PU/ PD	PHY SubLVDS LVCMOS
		gpi_74	3	I								
		safe_mode	7									
W26	-	csi21_dx4	0	IDS	L	L	7	vdda csi21[(23)]	Yes [(19)]	NA	PU/ PD	PHY SubLVDS LVCMOS
		gpi_75	3	I								
		safe_mode	7									
W25	-	csi21_dy4	0	IDS	L	L	7	vdda csi21[(23)]	Yes [(19)]	NA	PU/ PD	PHY SubLVDS LVCMOS
		gpi_76	3	I								
		safe_mode	7									
M26	-	csi22_dx0	0	IDS	L	L	7	vdda csi22[(23)]	Yes [(19)]	NA	PU/ PD	PHY SubLVDS LVCMOS
		gpi_77	3	I								
		safe_mode	7									
M25	-	csi22_dy0	0	IDS	L	L	7	vdda csi22[(23)]	Yes [(19)]	NA	PU/ PD	PHY SubLVDS LVCMOS
		gpi_78	3	I								
		safe_mode	7									
N26	-	csi22_dx1	0	IDS	L	L	7	vdda csi22[(23)]	Yes [(19)]	NA	PU/ PD	PHY SubLVDS LVCMOS
		gpi_79	3	I								
		safe_mode	7									
N25	-	csi22_dy1	0	IDS	L	L	7	vdda csi22[(23)]	Yes [(19)]	NA	PU/ PD	PHY SubLVDS LVCMOS
		gpi_80	3	I								
		safe_mode	7									
T27	-	cam_shutter	0	O	L	L	7	vdds_ dv_cam	Yes	4	PU/ PD	LVCMOS Dual Voltage
		gpio_81	3	IO								
		safe_mode	7									
U27	-	cam_strobe	0	O	L	L	7	vdds_ dv_cam	Yes	4	PU/ PD	LVCMOS Dual Voltage
		gpio_82	3	IO								
		safe_mode	7									
V27	-	cam_ globalreset	0	IO	L	L	7	vdds_ dv_cam	Yes	4	PU/ PD	LVCMOS Dual Voltage
		gpio_83	3	IO								
		safe_mode	7									

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Table 2-1. Ball Characteristics(1) (continued)

BALL BOTTOM [1]	BALL TOP [2]	PIN NAME [3]	MODE [4]	TYPE [5]	BALL RESET STATE [6]	BALL RESET REL. STATE [7]	RESET REL. MODE [8]	POWER [9]	HYS [10]	BUFFER STRENGTH (mA) [11]	PULL U/D TYPE [12]	IO CELL [13]
AE18	-	usbb1_ulpitll_clk	0	O	L	L	7	vdds_dv_bank0	Yes (18)	4(17)	PU/PD	LVCMOS Dual Voltage
		hsi1_cawake	1	I								
		gpio_84	3	IO								
		usbb1_ulpiphy_clk	4	I								
		attila_hw_dbg20	6	O								
		safe_mode	7									
AG19	-	usbb1_ulpitll_stp	0	I	H	H	7	vdds_dv_bank0	Yes	8	PU/PD	LVCMOS Dual Voltage
		hsi1_cadata	1	I								
		mcbsp4_clkr	2	IO								
		gpio_85	3	IO								
		usbb1_ulpiphy_stp	4	O								
		usbb1_mm_rxdp	5	IO								
		attila_hw_dbg21	6	O								
		safe_mode	7									
AF19	-	usbb1_ulpitll_dir	0	O	L	L	7	vdds_dv_bank0	Yes	8	PU/PD	LVCMOS Dual Voltage
		hsi1_caflag	1	I								
		mcbsp4_fsr	2	IO								
		gpio_86	3	IO								
		usbb1_ulpiphy_dir	4	I								
		attila_hw_dbg22	6	O								
		safe_mode	7									
AE19	-	usbb1_ulpitll_nxt	0	O	L	L	7	vdds_dv_bank0	Yes	8	PU/PD	LVCMOS Dual Voltage
		hsi1_acready	1	O								
		mcbsp4_fsx	2	IO								
		gpio_87	3	IO								
		usbb1_ulpiphy_nxt	4	I								
		usbb1_mm_rxdm	5	IO								
		attila_hw_dbg23	6	O								
		safe_mode	7									

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Table 2-1. Ball Characteristics(1) (continued)

BALL BOTTOM [1]	BALL TOP [2]	PIN NAME [3]	MODE [4]	TYPE [5]	BALL RESET STATE [6]	BALL RESET REL. STATE [7]	RESET REL. MODE [8]	POWER [9]	HYS [10]	BUFFER STRENGTH (mA) [11]	PULL U/D TYPE [12]	IO CELL [13]
AF18	-	usbb1_ulpitll_dat0	0	IO	L	L	7	vdds_dv_bank0	Yes	8	PU/PD	LVCMOS Dual Voltage
		hsi1_acwake	1	O								
		mcbsp4_clkx	2	IO								
		gpio_88	3	IO								
		usbb1_ulpiphy_dat0	4	IO								
		usbb1_mm_txen	5	IO								
		attila_hw_dbg24	6	O								
		safe_mode	7									
AG18	-	usbb1_ulpitll_dat1	0	IO	L	L	7	vdds_dv_bank0	Yes	8	PU/PD	LVCMOS Dual Voltage
		hsi1_acdata	1	O								
		mcbsp4_dx	2	IO								
		gpio_89	3	IO								
		usbb1_ulpiphy_dat1	4	IO								
		usbb1_mm_txdat	5	IO								
		attila_hw_dbg25	6	O								
		safe_mode	7									
AE17	-	usbb1_ulpitll_dat2	0	IO	L	L	7	vdds_dv_bank0	Yes	8	PU/PD	LVCMOS Dual Voltage
		hsi1_acflag	1	O								
		mcbsp4_dr	2	I								
		gpio_90	3	IO								
		usbb1_ulpiphy_dat2	4	IO								
		usbb1_mm_txse0	5	IO								
		attila_hw_dbg26	6	O								
		safe_mode	7									
AF17	-	usbb1_ulpitll_dat3	0	IO	L	L	7	vdds_dv_bank0	Yes	8	PU/PD	LVCMOS Dual Voltage
		hsi1_caready	1	I								
		gpio_91	3	IO								
		usbb1_ulpiphy_dat3	4	IO								
		usbb1_mm_rxrcv	5	IO								
		attila_hw_dbg27	6	O								
		safe_mode	7									

Table 2-1. Ball Characteristics[(1)] (continued)

BALL BOTTOM [1]	BALL TOP [2]	PIN NAME [3]	MODE [4]	TYPE [5]	BALL RESET STATE [6]	BALL RESET REL. STATE [7]	RESET REL. MODE [8]	POWER [9]	HYS [10]	BUFFER STRENGTH (mA) [11]	PULL U/D TYPE [12]	IO CELL [13]
AH17	-	usbb1_ulpitll_dat4	0	IO	L	L	7	vdds_dv_bank0	Yes	8	PU/PD	LVCMOS Dual Voltage
		dmtimer8_pwm_evt	1	IO								
		abe_mcbsp3_dr	2	I								
		gpio_92	3	IO								
		usbb1_ulpiphy_dat4	4	IO								
		attila_hw_dbg28	6	O								
		safe_mode	7									
AE16	-	usbb1_ulpitll_dat5	0	IO	L	L	7	vdds_dv_bank0	Yes	8	PU/PD	LVCMOS Dual Voltage
		dmtimer9_pwm_evt	1	IO								
		abe_mcbsp3_dx	2	IO								
		gpio_93	3	IO								
		usbb1_ulpiphy_dat5	4	IO								
		attila_hw_dbg29	6	O								
		safe_mode	7									
AF16	-	usbb1_ulpitll_dat6	0	IO	L	L	7	vdds_dv_bank0	Yes	8	PU/PD	LVCMOS Dual Voltage
		dmtimer10_pwm_evt	1	IO								
		abe_mcbsp3_clkx	2	IO								
		gpio_94	3	IO								
		usbb1_ulpiphy_dat6	4	IO								
		abe_dmic_din3	5	I								
		attila_hw_dbg30	6	O								
		safe_mode	7									
AG16	-	usbb1_ulpitll_dat7	0	IO	L	L	7	vdds_dv_bank0	Yes	8	PU/PD	LVCMOS Dual Voltage
		dmtimer11_pwm_evt	1	IO								
		abe_mcbsp3_fsx	2	IO								
		gpio_95	3	IO								
		usbb1_ulpiphy_dat7	4	IO								
		abe_dmic_clk3	5	O								
		attila_hw_dbg31	6	O								
		safe_mode	7									

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Table 2-1. Ball Characteristics(1) (continued)

BALL BOTTOM [1]	BALL TOP [2]	PIN NAME [3]	MODE [4]	TYPE [5]	BALL RESET STATE [6]	BALL RESET REL. STATE [7]	RESET REL. MODE [8]	POWER [9]	HYS [10]	BUFFER STRENGTH (mA) [11]	PULL U/D TYPE [12]	IO CELL [13]
AF14	-	usbb1_hsic_data	0	IO	L	L	7	vdds_1p2v	NA	0.1	PUy/PDy(2)	LVCMOS
		gpio_96	3	IO								
		safe_mode	7									
AE14	-	usbb1_hsic_strobe	0	IO	L	L	7	vdds_1p2v	NA	0.1	PUy/PDy(2)	LVCMOS
		gpio_97	3	IO								
		safe_mode	7									
H4	-	sim_io	0	IO	L	L	7	vdds_usim(28)	Yes (16)	1	PUy/PDy (10)	LVCMOS Dual Voltage
		gpio_wk0	3	IO								
		attila_hw_dbg1	6	O								
		safe_mode	7									
J2	-	sim_clk	0	O	L	L	7	vdds_usim(28)	Yes (16)	1	PUy/PDy (10)	LVCMOS Dual Voltage
		gpio_wk1	3	IO								
		attila_hw_dbg2	6	O								
		safe_mode	7									
G2	-	sim_reset	0	O	L	L	7	vdds_usim(28)	Yes (16)	1	PUy/PDy (10)	LVCMOS Dual Voltage
		gpio_wk2	3	IO								
		attila_hw_dbg3	6	O								
		safe_mode	7									
J1	-	sim_cd	0	I	H	H	7	vdds_1p8v	Yes	4	PU/PD	LVCMOS
		gpio_wk3	3	IO								
		attila_hw_dbg4	6	O								
		safe_mode	7									
K1	-	sim_pwrctrl	0	O	L	L	7	vdds_1p8v	Yes	4	PU/PD	LVCMOS
		gpio_wk4	3	IO								
		attila_hw_dbg5	6	O								
		safe_mode	7									
H2	-	usbc1_icusb_dp	0	IODS	L	L	7	vdds_usim(28)	Yes (16)	1	PUy/PDy	LVCMOS Dual Voltage SubLVDS
		gpio_98	3	IO								
		safe_mode	7									
H3	-	usbc1_icusb_dm	0	IODS	L	L	7	vdds_usim(28)	Yes (16)	1	PUy/PDy	LVCMOS Dual Voltage SubLVDS
		gpio_99	3	IO								
		safe_mode	7									
D2	-	sdmmc1_clk	0	O	L	L	7	vdds_sdmmc1(27)	Yes (16)	1	PUy/PDy	LVCMOS Dual Voltage
		dpm_emu19	2	O								
		gpio_100	3	IO								
		safe_mode	7									

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Table 2-1. Ball Characteristics[(1)] (continued)

BALL BOTTOM [1]	BALL TOP [2]	PIN NAME [3]	MODE [4]	TYPE [5]	BALL RESET STATE [6]	BALL RESET REL. STATE [7]	RESET REL. MODE [8]	POWER [9]	HYS [10]	BUFFER STRENGTH (mA) [11]	PULL U/D TYPE [12]	IO CELL [13]
E3	-	sdmmc1_cmd	0	IO	L	L	7	vdds_sdmmc1(27)	Yes (16)	1	PUy/PDy	LVCMOS Dual Voltage
		uart1_rx	2	I								
		gpio_101	3	IO								
		safe_mode	7									
E4	-	sdmmc1_dat0	0	IO	L	L	7	vdds_sdmmc1(27)	Yes (16)	1	PUy/PDy	LVCMOS Dual Voltage
		dpm_emu18	2	O								
		gpio_102	3	IO								
		safe_mode	7									
E2	-	sdmmc1_dat1	0	IO	L	L	7	vdds_sdmmc1(27)	Yes (16)	1	PUy/PDy	LVCMOS Dual Voltage
		dpm_emu17	2	O								
		gpio_103	3	IO								
		safe_mode	7									
E1	-	sdmmc1_dat2	0	IO	L	L	7	vdds_sdmmc1(27)	Yes (16)	1	PUy/PDy	LVCMOS Dual Voltage
		dpm_emu16	2	O								
		gpio_104	3	IO								
		jtag_tms_tmsc	4	IO								
		safe_mode	7									
F4	-	sdmmc1_dat3	0	IO	L	L	7	vdds_sdmmc1(27)	Yes (16)	1	PUy/PDy	LVCMOS Dual Voltage
		dpm_emu15	2	O								
		gpio_105	3	IO								
		jtag_tck	4	I								
		safe_mode	7									
F3	-	sdmmc1_dat4	0	IO	L	L	7	vdds_sdmmc1(27)	Yes (16)	1	PUy/PDy	LVCMOS Dual Voltage
		gpio_106	3	IO								
		safe_mode	7									
F1	-	sdmmc1_dat5	0	IO	L	L	7	vdds_sdmmc1(27)	Yes (16)	1	PUy/PDy	LVCMOS Dual Voltage
		gpio_107	3	IO								
		safe_mode	7									
G4	-	sdmmc1_dat6	0	IO	L	L	7	vdds_sdmmc1(27)	Yes (16)	1	PUy/PDy	LVCMOS Dual Voltage
		gpio_108	3	IO								
		safe_mode	7									
G3	-	sdmmc1_dat7	0	IO	L	L	7	vdds_sdmmc1(27)	Yes (16)	1	PUy/PDy	LVCMOS Dual Voltage
		gpio_109	3	IO								
		safe_mode	7									

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Table 2-1. Ball Characteristics(1) (continued)

BALL BOTTOM [1]	BALL TOP [2]	PIN NAME [3]	MODE [4]	TYPE [5]	BALL RESET STATE [6]	BALL RESET REL. STATE [7]	RESET REL. MODE [8]	POWER [9]	HYS [10]	BUFFER STRENGTH (mA) [11]	PULL U/D TYPE [12]	IO CELL [13]
AD27	-	abe_mcbsp2_clkx	0	IO	L	L	7	vdds_dv_bank1	Yes	4	PU/PD	LVCMOS Dual Voltage
		mcspi2_clk	1	IO								
		abe_mcasp_ahclkx	2	O								
		gpio_110	3	IO								
		usbb2_mm_rxdm	4	IO								
		safe_mode	7									
AD26	-	abe_mcbsp2_dr	0	I	L	L	7	vdds_dv_bank1	Yes	4	PU/PD	LVCMOS Dual Voltage
		mcspi2_somi	1	IO								
		abe_mcasp_axr	2	IO								
		gpio_111	3	IO								
		usbb2_mm_rxdp	4	IO								
		safe_mode	7									
AD25	-	abe_mcbsp2_dx	0	IO	L	L	7	vdds_dv_bank1	Yes	4	PU/PD	LVCMOS Dual Voltage
		mcspi2_simo	1	IO								
		abe_mcasp_amute	2	O								
		gpio_112	3	IO								
		usbb2_mm_rxrcv	4	IO								
		safe_mode	7									
AC28	-	abe_mcbsp2_fsx	0	IO	L	L	7	vdds_dv_bank1	Yes	4	PU/PD	LVCMOS Dual Voltage
		mcspi2_cs0	1	IO								
		abe_mcasp_afsx	2	O								
		gpio_113	3	IO								
		usbb2_mm_txen	4	IO								
		safe_mode	7									
AC26	-	abe_mcbsp1_clkx	0	IO	L	L	7	vdds_dv_bank1	Yes	4	PU/PD	LVCMOS Dual Voltage
		abe_slimbus1_clock	1	IO								
		gpio_114	3	IO								
		safe_mode	7									
AC25	-	abe_mcbsp1_dr	0	I	L	L	7	vdds_dv_bank1	Yes	4	PU/PD	LVCMOS Dual Voltage
		abe_slimbus1_data	1	IO								
		gpio_115	3	IO								
		safe_mode	7									

Table 2-1. Ball Characteristics(1) (continued)

BALL BOTTOM [1]	BALL TOP [2]	PIN NAME [3]	MODE [4]	TYPE [5]	BALL RESET STATE [6]	BALL RESET REL. STATE [7]	RESET REL. MODE [8]	POWER [9]	HYS [10]	BUFFER STRENGTH (mA) [11]	PULL U/D TYPE [12]	IO CELL [13]
AB25	-	abe_mcbsp1_dx	0	IO	L	L	7	vdds_dv_bank1	Yes	4	PU/PD	LVCMOS Dual Voltage
		sdmmc3_dat2	1	IO								
		abe_mcasp_aclkx	2	O								
		gpio_116	3	IO								
		safe_mode	7									
AC27	-	abe_mcbsp1_fsx	0	IO	L	L	7	vdds_dv_bank1	Yes	4	PU/PD	LVCMOS Dual Voltage
		sdmmc3_dat3	1	IO								
		abe_mcasp_amutein	2	I								
		gpio_117	3	IO								
		safe_mode	7									
AG25	-	abe_pdm_ul_data	0	I	L	L	7	vdds_dv_bank2	Yes	4	PU/PD	LVCMOS Dual Voltage
		abe_mcbsp3_dr	1	I								
		safe_mode	7									
AF25	-	abe_pdm_dl_data	0	O	L	L	7	vdds_dv_bank2	Yes	4	PU/PD	LVCMOS Dual Voltage
		abe_mcbsp3_dx	1	IO								
		safe_mode	7									
AE25	-	abe_pdm_frame	0	IO	L	L	7	vdds_dv_bank2	Yes	4	PU/PD	LVCMOS Dual Voltage
		abe_mcbsp3_clkx	1	IO								
		safe_mode	7									
AF26	-	abe_pdm_lb_clk	0	O	L	L	7	vdds_dv_bank2	Yes	4	PU/PD	LVCMOS Dual Voltage
		abe_mcbsp3_fsx	1	IO								
		safe_mode	7									
AH26	-	abe_clks	0	I	L	L	7	vdds_dv_bank2	Yes	4	PU/PD	LVCMOS Dual Voltage
		gpio_118	3	IO								
		safe_mode	7									
AE24	-	abe_dmic_clk1	0	O	L	L	7	vdds_dv_bank2	Yes	4	PU/PD	LVCMOS Dual Voltage
		gpio_119	3	IO								
		usbb2_mm_txse0	4	IO								
		uart4_cts	5	I								
		safe_mode	7									

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Table 2-1. Ball Characteristics(1) (continued)

BALL BOTTOM [1]	BALL TOP [2]	PIN NAME [3]	MODE [4]	TYPE [5]	BALL RESET STATE [6]	BALL RESET REL. STATE [7]	RESET REL. MODE [8]	POWER [9]	HYS [10]	BUFFER STRENGTH (mA) [11]	PULL U/D TYPE [12]	IO CELL [13]
AF24	-	abe_dmic_din1	0	I	L	L	7	vdds_dv_bank2	Yes	4	PU/PD	LVCMOS Dual Voltage
		gpio_120	3	IO								
		usbb2_mm_txdat	4	IO								
		uart4_rts	5	O								
		safe_mode	7									
AG24	-	abe_dmic_din2	0	I	L	L	7	vdds_dv_bank2	Yes	4	PU/PD	LVCMOS Dual Voltage
		slimbus2_clock	1	IO								
		abe_mcasp_axr	2									
		gpio_121	3	IO								
		dmtimer11_pwm_evt	5	IO								
		safe_mode	7									
AH24	-	abe_dmic_din3	0	I	L	L	7	vdds_dv_bank2	Yes	4	PU/PD	LVCMOS Dual Voltage
		slimbus2_data	1	IO								
		abe_dmic_clk2	2	O								
		gpio_122	3	IO								
		dmtimer9_pwm_evt	5	IO								
		safe_mode	7									
AB26	-	uart2_cts	0	I	H	H	7	vdds_dv_bank1	Yes	4	PU/PD	LVCMOS Dual Voltage
		sdmmc3_clk	1	O								
		gpio_123	3	IO								
		safe_mode	7									
AB27	-	uart2_rts	0	O	H	H	7	vdds_dv_bank1	Yes	4	PU/PD	LVCMOS Dual Voltage
		sdmmc3_cmd	1	IO								
		gpio_124	3	IO								
		safe_mode	7									
AA25	-	uart2_rx	0	I	H	H	7	vdds_dv_bank1	Yes	4	PU/PD	LVCMOS Dual Voltage
		sdmmc3_dat0	1	IO								
		gpio_125	3	IO								
		safe_mode	7									
AA26	-	uart2_tx	0	O	H	H	7	vdds_dv_bank1	Yes	4	PU/PD	LVCMOS Dual Voltage
		sdmmc3_dat1	1	IO								
		gpio_126	3	IO								
		safe_mode	7									

Table 2-1. Ball Characteristics(1) (continued)

BALL BOTTOM [1]	BALL TOP [2]	PIN NAME [3]	MODE [4]	TYPE [5]	BALL RESET STATE [6]	BALL RESET REL. STATE [7]	RESET REL. MODE [8]	POWER [9]	HYS [10]	BUFFER STRENGTH (mA) [11]	PULL U/D TYPE [12]	IO CELL [13]
AA27	-	hdq_sio	0	IOD	Z	Z	7	vdds_ 1p8v	Yes	4	PU/ PD	LVCMOS Open Drain
		i2c3_sccb	1	OD								
		i2c2_sccb	2	OD								
		gpio_127	3	IO								
		safe_mode	7									
AE28	-	i2c1_scl	0	OD	H	H	0	vdds_ dv_ bank2	Yes	3	PUx/ PDy- OD (6)	LVCMOS Open Drain Dual Voltage
AE26	-	i2c1_sda	0	IOD	H	H(5)	0	vdds_ dv_ bank2	Yes	3	PUx/ PDy- OD (6)	LVCMOS Open Drain Dual Voltage
C26	-	i2c2_scl	0	OD	H	H	7	vdds_ 1p8v	Yes	3	PUx/ PDy- GPIO (6)	LVCMOS Open Drain
		uart1_rx	1	I						4		
		gpio_128	3	IO						4		
		safe_mode	7							4		
D26	-	i2c2_sda	0	IOD	H	H	7	vdds_ 1p8v	Yes	3	PUx/ PDy- GPIO (6)	LVCMOS Open Drain
		uart1_tx	1	O						4		
		gpio_129	3	IO						4		
		safe_mode	7							4		
W27	-	i2c3_scl	0	OD	H	H	7	vdds_ dv_cam	Yes	3	PUx/ PDy- GPIO (6)	LVCMOS Open Drain Dual Voltage
		gpio_130	3	IO						4		
		safe_mode	7							4		
Y27	-	i2c3_sda	0	IOD	H	H	7	vdds_ dv_cam	Yes	3	PUx/ PDy- GPIO (6)	LVCMOS Open Drain Dual Voltage
		gpio_131	3	IO						4		
		safe_mode	7							4		
AG21	-	i2c4_scl	0	OD	H	H	7	vdds_ dv_ bank5	Yes	3	PUx/ PDy- GPIO (6)	LVCMOS Open Drain Dual Voltage
		gpio_132	3	IO						4		
		safe_mode	7							4		
AH22	-	i2c4_sda	0	IOD	H	H	7	vdds_ dv_ bank5	Yes	3	PUx/ PDy- GPIO (6)	LVCMOS Open Drain Dual Voltage
		gpio_133	3	IO						4		
		safe_mode	7							4		
AG9	-	sr_scl	0	OD	H	H	0	vdds_ dv_ bank2	Yes	3	PUx/ PDy- OD (6)	LVCMOS Open Drain Dual Voltage
AF9	-	sr_sda	0	IOD	H	H	0	vdds_ dv_ bank2	Yes	3	PUx/ PDy- OD (6)	LVCMOS Open Drain Dual Voltage
AF22	-	mcspi1_clk	0	IO	L	L	7	vdds_ dv_ bank3	Yes	4	PU/ PD	LVCMOS Dual Voltage
		gpio_134	3	IO								
		safe_mode	7									
AE22	-	mcspi1_somi	0	IO	L	L	7	vdds_ dv_ bank3	Yes	4	PU/ PD	LVCMOS Dual Voltage
		gpio_135	3	IO								
		safe_mode	7									

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Table 2-1. Ball Characteristics(1) (continued)

BALL BOTTOM [1]	BALL TOP [2]	PIN NAME [3]	MODE [4]	TYPE [5]	BALL RESET STATE [6]	BALL RESET REL. STATE [7]	RESET REL. MODE [8]	POWER [9]	HYS [10]	BUFFER STRENGTH (mA) [11]	PULL U/D TYPE [12]	IO CELL [13]
AG22	-	mcspi1_simo	0	IO	L	L	7	vdds_dv_bank3	Yes	4	PU/PD	LVCMOS Dual Voltage
		gpio_136	3	IO								
		safe_mode	7									
AE23	-	mcspi1_cs0	0	IO	L	L	7	vdds_dv_bank3	Yes	4	PU/PD	LVCMOS Dual Voltage
		gpio_137	3	IO								
		safe_mode	7									
AF23	-	mcspi1_cs1	0	O	L	L	7	vdds_dv_bank3	Yes	4	PU/PD	LVCMOS Dual Voltage
		uart1_rx	1	I								
		gpio_138	3	IO								
		safe_mode	7									
AG23	-	mcspi1_cs2	0	O	H	H	7	vdds_dv_bank3	Yes	4	PU/PD	LVCMOS Dual Voltage
		uart1_cts	1	I								
		slimbus2_clock	2	IO								
		gpio_139	3	IO								
		safe_mode	7									
AH23	-	mcspi1_cs3	0	O	H	H	7	vdds_dv_bank3	Yes (17)	4	PU/PD	LVCMOS Dual Voltage
		uart1_rts	1	O								
		slimbus2_data	2	IO								
		gpio_140	3	IO								
		safe_mode	7									
F27	-	uart3_cts_rctx	0	IO	H	H	7	vdds_1p8v	Yes	4	PU/PD	LVCMOS
		uart1_tx	1	O								
		gpio_141	3	IO								
		safe_mode	7									
F28	-	uart3_rts_sd	0	O	H	H	7	vdds_1p8v	Yes	4	PU/PD	LVCMOS
		gpio_142	3	IO								
		safe_mode	7									
G27	-	uart3_rx_irrx	0	I	H	H	7	vdds_1p8v	Yes	4	PU/PD	LVCMOS
		dmtimer8_pwm_evt	1	IO								
		gpio_143	3	IO								
		safe_mode	7									
G28	-	uart3_tx_irtx	0	O	H	H	7	vdds_1p8v	Yes	4	PU/PD	LVCMOS
		dmtimer9_pwm_evt	1	IO								
		gpio_144	3	IO								
		safe_mode	7									
AE5	-	sdmmc5_clk	0	O	L	L	7	vdds_dv_bank4	Yes	4	PU/PD	LVCMOS Dual Voltage SubLVDS
		mcspi2_clk	1	IO								
		usbc1_icusb_dp	2	IODS								
		gpio_145	3	IO								
		sdmmc2_clk	5	O								
		safe_mode	7									

Table 2-1. Ball Characteristics(1) (continued)

BALL BOTTOM [1]	BALL TOP [2]	PIN NAME [3]	MODE [4]	TYPE [5]	BALL RESET STATE [6]	BALL RESET REL. STATE [7]	RESET REL. MODE [8]	POWER [9]	HYS [10]	BUFFER STRENGTH (mA) [11]	PULL U/D TYPE [12]	IO CELL [13]
AF5	-	sdmmc5_cmd	0	IO	H	H	7	vdds_dv_bank4	Yes	4	PU/PD	LVCMOS Dual Voltage SubLVDS
		mcspi2_simo	1	IO								
		usbc1_icusb_dm	2	IODS								
		gpio_146	3	IO								
		sdmmc2_cmd	5	IO								
		safe_mode	7									
AE4	-	sdmmc5_dat0	0	IO	H	H	7	vdds_dv_bank4	Yes	4	PU/PD	LVCMOS Dual Voltage
		mcspi2_somi	1	IO								
		usbc1_icusb_rcv	2	I								
		gpio_147	3	IO								
		sdmmc2_dat0	5	IO								
		safe_mode	7									
AF4	-	sdmmc5_dat1	0	IO	H	H	7	vdds_dv_bank4	Yes	4	PU/PD	LVCMOS Dual Voltage
		usbc1_icusb_txen	2	O								
		gpio_148	3	IO								
		sdmmc2_dat1	5	IO								
		safe_mode	7									
AG3	-	sdmmc5_dat2	0	IO	H	H	7	vdds_dv_bank4	Yes	4	PU/PD	LVCMOS Dual Voltage
		mcspi2_cs1	1	O								
		gpio_149	3	IO								
		sdmmc2_dat2	5	IO								
		safe_mode	7									
AF3	-	sdmmc5_dat3	0	IO	H	H	7	vdds_dv_bank4	Yes	4	PU/PD	LVCMOS Dual Voltage
		mcspi2_cs0	1	IO								
		gpio_150	3	IO								
		sdmmc2_dat3	5	IO								
		safe_mode	7									
AE21	-	mcspi4_clk	0	IO	L	L	7	vdds_dv_bank5	Yes	4	PU/PD	LVCMOS Dual Voltage Open Drain
		sdmmc4_clk	1	O								
		kpd_col6	2	OD								
		gpio_151	3	IO								
		safe_mode	7									

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Table 2-1. Ball Characteristics(1) (continued)

BALL BOTTOM [1]	BALL TOP [2]	PIN NAME [3]	MODE [4]	TYPE [5]	BALL RESET STATE [6]	BALL RESET REL. STATE [7]	RESET REL. MODE [8]	POWER [9]	HYS [10]	BUFFER STRENGTH (mA) [11]	PULL U/D TYPE [12]	IO CELL [13]
AF20	-	mcspi4_simo	0	IO	H	H	7	vdds_dv_bank5	Yes	4	PU/PD	LVCMOS Dual Voltage Open Drain
		sdmmc4_cmd	1	IO								
		kpd_col7	2	OD								
		gpio_152	3	IO								
		safe_mode	7									
AF21	-	mcspi4_somi	0	IO	H	H	7	vdds_dv_bank5	Yes	4	PU/PD	LVCMOS Dual Voltage
		sdmmc4_dat0	1	IO								
		kpd_row6	2	I								
		gpio_153	3	IO								
		safe_mode	7									
AE20	-	mcspi4_cs0	0	IO	H	H	7	vdds_dv_bank5	Yes	4	PU/PD	LVCMOS Dual Voltage
		sdmmc4_dat3	1	IO								
		kpd_row7	2	I								
		gpio_154	3	IO								
		safe_mode	7									
AG20	-	uart4_rx	0	I	H	H	7	vdds_dv_bank5	Yes	4	PU/PD	LVCMOS Dual Voltage
		sdmmc4_dat2	1	IO								
		kpd_row8	2	I								
		gpio_155	3	IO								
		safe_mode	7									
AH19	-	uart4_tx	0	O	H	H	7	vdds_dv_bank5	Yes	4	PU/PD	LVCMOS Dual Voltage Open Drain
		sdmmc4_dat1	1	IO								
		kpd_col8	2	OD								
		gpio_156	3	IO								
		safe_mode	7									
AG12	-	usbb2_ulpitll_clk	0	O	L	L	7	vdds_dv_bank6	Yes (18)	4(17)	PU/PD	LVCMOS Dual Voltage
		usbb2_ulpiphy_clk	1	I								
		sdmmc4_cmd	2	IO								
		gpio_157	3	IO								
		hsi2_cawake	4	I								
		safe_mode	7									
AF12	-	usbb2_ulpitll_stp	0	I	H	H	7	vdds_dv_bank6	Yes	4(17)	PU/PD	LVCMOS Dual Voltage
		usbb2_ulpiphy_stp	1	O								
		sdmmc4_clk	2	O								
		gpio_158	3	IO								
		hsi2_cadata	4	I								
		dispc2_data23	5	O								
		safe_mode	7									

Table 2-1. Ball Characteristics(1) (continued)

BALL BOTTOM [1]	BALL TOP [2]	PIN NAME [3]	MODE [4]	TYPE [5]	BALL RESET STATE [6]	BALL RESET REL. STATE [7]	RESET REL. MODE [8]	POWER [9]	HYS [10]	BUFFER STRENGTH (mA) [11]	PULL U/D TYPE [12]	IO CELL [13]
AE12	-	usbb2_ulpitll_dir	0	O	H	H	7	vdds_dv_bank6	Yes	4(17)	PU/PD	LVCMOS Dual Voltage
		usbb2_ulpiphy_dir	1	I								
		sdmmc4_dat0	2	IO								
		gpio_159	3	IO								
		hsi2_caflag	4	I								
		dispc2_data22	5	O								
		safe_mode	7									
AG13	-	usbb2_ulpitll_nxt	0	O	H	H	7	vdds_dv_bank6	Yes	4(17)	PU/PD	LVCMOS Dual Voltage
		usbb2_ulpiphy_nxt	1	I								
		sdmmc4_dat1	2	IO								
		gpio_160	3	IO								
		hsi2_acready	4	O								
		dispc2_data21	5	O								
		safe_mode	7									
AE11	-	usbb2_ulpitll_dat0	0	IO	H	H	7	vdds_dv_bank6	Yes	4(17)	PU/PD	LVCMOS Dual Voltage
		usbb2_ulpiphy_dat0	1	IO								
		sdmmc4_dat2	2	IO								
		gpio_161	3	IO								
		hsi2_acwake	4	O								
		dispc2_data20	5	O								
		usbb2_mm_txen	6	IO								
		safe_mode	7									
AF11	-	usbb2_ulpitll_dat1	0	IO	H	H	7	vdds_dv_bank6	Yes	4(17)	PU/PD	LVCMOS Dual Voltage
		usbb2_ulpiphy_dat1	1	IO								
		sdmmc4_dat3	2	IO								
		gpio_162	3	IO								
		hsi2_acdata	4	O								
		dispc2_data19	5	O								
		usbb2_mm_txdat	6	IO								
		safe_mode	7									

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Table 2-1. Ball Characteristics(1) (continued)

BALL BOTTOM [1]	BALL TOP [2]	PIN NAME [3]	MODE [4]	TYPE [5]	BALL RESET STATE [6]	BALL RESET REL. STATE [7]	RESET REL. MODE [8]	POWER [9]	HYS [10]	BUFFER STRENGTH (mA) [11]	PULL U/D TYPE [12]	IO CELL [13]
AG11	-	usbb2_ulpitll_dat2	0	IO	L	L	7	vdds_dv_bank6	Yes	4(17)	PU/PD	LVCMOS Dual Voltage
		usbb2_ulpiphy_dat2	1	IO								
		sdmmc3_dat2	2	IO								
		gpio_163	3	IO								
		hsi2_acflag	4	O								
		dispc2_data18	5	O								
		usbb2_mm_txse0	6	IO								
		safe_mode	7									
AH11	-	usbb2_ulpitll_dat3	0	IO	H	H	7	vdds_dv_bank6	Yes	4(17)	PU/PD	LVCMOS Dual Voltage
		usbb2_ulpiphy_dat3	1	IO								
		sdmmc3_dat1	2	IO								
		gpio_164	3	IO								
		hsi2_caready	4	I								
		dispc2_data15	5	O								
		rfbi_data15	6	IO								
		safe_mode	7									
AE10	-	usbb2_ulpitll_dat4	0	IO	H	H	7	vdds_dv_bank6	Yes	4(17)	PU/PD	LVCMOS Dual Voltage
		usbb2_ulpiphy_dat4	1	IO								
		sdmmc3_dat0	2	IO								
		gpio_165	3	IO								
		mcspi3_somi	4	IO								
		dispc2_data14	5	O								
		rfbi_data14	6	IO								
		safe_mode	7									
AF10	-	usbb2_ulpitll_dat5	0	IO	H	H	7	vdds_dv_bank6	Yes	4(17)	PU/PD	LVCMOS Dual Voltage
		usbb2_ulpiphy_dat5	1	IO								
		sdmmc3_dat3	2	IO								
		gpio_166	3	IO								
		mcspi3_cs0	4	IO								
		dispc2_data13	5	O								
		rfbi_data13	6	IO								
		safe_mode	7									

Table 2-1. Ball Characteristics(1) (continued)

BALL BOTTOM [1]	BALL TOP [2]	PIN NAME [3]	MODE [4]	TYPE [5]	BALL RESET STATE [6]	BALL RESET REL. STATE [7]	RESET REL. MODE [8]	POWER [9]	HYS [10]	BUFFER STRENGTH (mA) [11]	PULL U/D TYPE [12]	IO CELL [13]
AG10	-	usbb2_ulpitll_dat6	0	IO	H	H	7	vdds_dv_bank6	Yes	4(17)	PU/PD	LVCMOS Dual Voltage
		usbb2_ulpiphy_dat6	1	IO								
		sdmmc3_cmd	2	IO								
		gpio_167	3	IO								
		mcspi3_simo	4	IO								
		dispc2_data12	5	O								
		rfbi_data12	6	IO								
		safe_mode	7									
AE9	-	usbb2_ulpitll_dat7	0	IO	H	H	7	vdds_dv_bank6	Yes	4(17)	PU/PD	LVCMOS Dual Voltage
		usbb2_ulpiphy_dat7	1	IO								
		sdmmc3_clk	2	O								
		gpio_168	3	IO								
		mcspi3_clk	4	IO								
		dispc2_data11	5	O								
		rfbi_data11	6	IO								
		safe_mode	7									
AF13	-	usbb2_hsic_data	0	IO	L	L	7	vdds_1p2v	NA	0.1	PUy/PDy(2)	LVCMOS
		gpio_169	3	IO								
		safe_mode	7									
AE13	-	usbb2_hsic_strobe	0	IO	L	L	7	vdds_1p2v	NA	0.1	PUy/PDy(2)	LVCMOS
		gpio_170	3	IO								
		safe_mode	7									
G26	-	kpd_col3	0	OD	L	L	7	vdds_dv_bank7	Yes	4	PU/PD	LVCMOS Dual Voltage Open Drain
		kpd_col0	1	OD								
		gpio_171	3	IO								
		safe_mode	7									
G25	-	kpd_col4	0	OD	L	L	7	vdds_dv_bank7	Yes	4	PU/PD	LVCMOS Dual Voltage Open Drain
		kpd_col1	1	OD								
		gpio_172	3	IO								
		safe_mode	7									
H26	-	kpd_col5	0	OD	L	L	7	vdds_dv_bank7	Yes	4	PU/PD	LVCMOS Dual Voltage Open Drain
		kpd_col2	1	OD								
		gpio_173	3	IO								
		safe_mode	7									
H25	-	kpd_col0	0	OD	L	L	7	vdds_dv_bank7	Yes	4	PU/PD	LVCMOS Dual Voltage Open Drain
		kpd_col3	1	OD								
		gpio_174	3	IO								
		safe_mode	7									

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Table 2-1. Ball Characteristics[1] (continued)

BALL BOTTOM [1]	BALL TOP [2]	PIN NAME [3]	MODE [4]	TYPE [5]	BALL RESET STATE [6]	BALL RESET REL. STATE [7]	RESET REL. MODE [8]	POWER [9]	HYS [10]	BUFFER STRENGTH (mA) [11]	PULL U/D TYPE [12]	IO CELL [13]
J27	-	kpd_col1	0	OD	L	L	7	vdds_dv _bank7	Yes	4	PU/ PD	LVCMOS Dual Voltage Open Drain
		kpd_col4	1	OD								
		gpio_0	3	IO								
		safe_mode	7									
H27	-	kpd_col2	0	OD	L	L	7	vdds_dv _bank7	Yes	4	PU/ PD	LVCMOS Dual Voltage Open Drain
		kpd_col5	1	OD								
		gpio_1	3	IO								
		safe_mode	7									
J26	-	kpd_row3	0	I	L	H	7	vdds_dv _bank7	Yes	4	PU/ PD	LVCMOS Dual Voltage
		kpd_row0	1	I								
		gpio_175	3	IO								
		safe_mode	7									
J25	-	kpd_row4	0	I	L	H	7	vdds_dv _bank7	Yes	4	PU/ PD	LVCMOS Dual Voltage
		kpd_row1	1	I								
		gpio_176	3	IO								
		safe_mode	7									
K26	-	kpd_row5	0	I	L	H	7	vdds_dv _bank7	Yes	4	PU/ PD	LVCMOS Dual Voltage
		kpd_row2	1	I								
		gpio_177	3	IO								
		safe_mode	7									
K25	-	kpd_row0	0	I	L	H	7	vdds_dv _bank7	Yes	4	PU/ PD	LVCMOS Dual Voltage
		kpd_row3	1	I								
		gpio_178	3	IO								
		safe_mode	7									
L27	-	kpd_row1	0	I	L	H	7	vdds_dv _bank7	Yes	4	PU/ PD	LVCMOS Dual Voltage
		kpd_row4	1	I								
		gpio_2	3	IO								
		safe_mode	7									
K27	-	kpd_row2	0	I	L	H	7	vdds_dv _bank7	Yes	4	PU/ PD	LVCMOS Dual Voltage
		kpd_row5	1	I								
		gpio_3	3	IO								
		safe_mode	7									
C3	-	usba0_otg_ ce	0	O	0	0	0	vdda_ usba0otg _3p3v[26]	NA	See[22]	NA	PHY
B5	-	usba0_otg_ dp	0	IODS	0	Z	7	vdda_ usba0otg _3p3v[26]	Yes [20]	See[14]	PUx/ PDy [15]	LVCMOS SubLVDS
		uart3_rx_irrx	1	I								
		uart2_rx	2	I								
		safe_mode	7									
B4	-	usba0_otg_ dm	0	IODS	0	Z	7	vdda_ usba0otg _3p3v[26]	Yes [20]	See[14]	PUx/ PDy [15]	LVCMOS SubLVDS
		uart3_tx_irtx	1	O								
		uart2_tx	2	O								
		safe_mode	7									
AH6	-	fref_xtal_in	0	AI-I	Z	Z	0	vdds_ 1p8_fref	Yes	NA	NA	LVCMOS Analog

Table 2-1. Ball Characteristics[(1)] (continued)

BALL BOTTOM [1]	BALL TOP [2]	PIN NAME [3]	MODE [4]	TYPE [5]	BALL RESET STATE [6]	BALL RESET REL. STATE [7]	RESET REL. MODE [8]	POWER [9]	HYS [10]	BUFFER STRENGTH (mA) [11]	PULL U/D TYPE [12]	IO CELL [13]
AH5	-	fref_xtal_out	0	AO	Z	NA	0	vdds_ 1p8_fref	NA	NA	NA	OSC
AG5	-	fref_xtal_ vssosc	0	NA	NA	NA	NA	NA	NA	NA	NA	NA
AG8	-	fref_slicer_in	0	AI-I	Z	Z	0	vdds_ 1p8_fref	NA	NA	NA	LVCMOS Analog
		gpi_wk5	3	I								
		safe_mode	7									
AD1	-	fref_clk_ioreq	0	O	L	L	0	vdds_ 1p8_fref	Yes	4	PU/ PD	LVCMOS
AD2	-	fref_clk0_out	0	O	L	L	7	vdds_ 1p8_fref	Yes	4	PU/ PD	LVCMOS
		fref_clk1_req	1	I								
		sys_drm_ msecure	2	O								
		gpio_wk6	3	IO								
		sdmmc2_ dat7	5	IO								
		attila_hw_ dbg6	6	O								
		safe_mode	7									
AA28	-	fref_clk1_out	0	O	L	L	7	vdds_ dv_cam	Yes	4	PU/ PD	LVCMOS Dual Voltage
		gpio_181	3	IO								
		safe_mode	7									
Y28	-	fref_clk2_out	0	O	L	L	7	vdds_ dv_cam	Yes	4	PU/ PD	LVCMOS Dual Voltage
		gpio_182	3	IO								
		safe_mode	7									
AD3	-	fref_clk3_req	0	I	L	L	7	vdds_ dv_ fref	Yes	4	PU/ PD	LVCMOS Dual Voltage
		fref_clk1_req	1	I								
		sys_drm_ msecure	2	O								
		gpio_wk30	3	IO								
		sdmmc2_ dat4	5	IO								
		attila_hw_ dbg7	6	O								
		safe_mode	7									
AD4	-	fref_clk3_out	0	O	L	L	7	vdds_ dv_ fref	Yes	4	PU/ PD	LVCMOS Dual Voltage
		fref_clk2_req	1	I								
		sys_secure_ indicator	2	O								
		gpio_wk31	3	IO								
		sdmmc2_ dat5	5	IO								
		attila_hw_ dbg8	6	O								
		safe_mode	7									

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Table 2-1. Ball Characteristics[(1)] (continued)

BALL BOTTOM [1]	BALL TOP [2]	PIN NAME [3]	MODE [4]	TYPE [5]	BALL RESET STATE [6]	BALL RESET REL. STATE [7]	RESET REL. MODE [8]	POWER [9]	HYS [10]	BUFFER STRENGTH (mA) [11]	PULL U/D TYPE [12]	IO CELL [13]
AC2	-	fref_clk4_req	0	I	L	L	0	vdds_ dv_ fref	Yes	4	PU/ PD	LVCMOS Dual Voltage
		fref_clk5_out	1	O								
		gpio_wk7	3	IO								
		sdmmc2_ dat6	5	IO								
		attila_hw_ dbg9	6	O								
AC3	-	fref_clk4_out	0	O	L	0	0	vdds_ dv_ fref	Yes	4	PU/ PD	LVCMOS Dual Voltage
		gpio_wk8	3	IO								
		attila_hw_ dbg10	6	O								
AG7	-	sys_32k	0	I	Z	Z	0	vdds_ 1p8v	Yes	4	PU/ PD	LVCMOS
AE7	-	sys_ nrespwron	0	I	Z	Z	0	vdds_ 1p8v	Yes	4	PUx/ PDy (11)	LVCMOS
AF7	-	sys_ nreswarm	0	IOD	0	H	0	vdds_ 1p8v	Yes	4	PUx/ PDy (11)	LVCMOS Open Drain
AH7	-	sys_pwr_req	0	O	H	1	0	vdds_ 1p8v	Yes	4	PU/ PD	LVCMOS
AG6	-	sys_pwron_ reset_out	0	O	L	0	0	vdds_ 1p8v	Yes	4	PU/ PD	LVCMOS
		gpio_wk29	3	IO								
		attila_hw_ dbg11	6	O								
AE6	-	sys_nirq1	0	I	H	H	7	vdds_ 1p8v	Yes	4	PU/ PD	LVCMOS
		safe_mode	7									
AF6	-	sys_nirq2	0	I	H	H	7	vdds_ 1p8v	Yes	4	PU/ PD	LVCMOS
		gpio_183	3	IO								
		safe_mode	7									
F26	-	sys_boot0	0	I	L	L	0	vdds_ 1p8v	Yes	4	PU/ PD	LVCMOS
		gpio_184	3	IO								
		safe_mode	7									
E27	-	sys_boot1	0	I	L	L	0	vdds_ 1p8v	Yes	4	PU/ PD	LVCMOS
		gpio_185	3	IO								
		safe_mode	7									
E26	-	sys_boot2	0	I	L	L	0	vdds_ 1p8v	Yes	4	PU/ PD	LVCMOS
		gpio_186	3	IO								
		safe_mode	7									
E25	-	sys_boot3	0	I	L	L	0	vdds_ 1p8v	Yes	4	PU/ PD	LVCMOS
		gpio_187	3	IO								
		safe_mode	7									
D28	-	sys_boot4	0	I	L	L	0	vdds_ 1p8v	Yes	4	PU/ PD	LVCMOS
		gpio_188	3	IO								
		safe_mode	7									
D27	-	sys_boot5	0	I	L	L	0	vdds_ 1p8v	Yes	4	PU/ PD	LVCMOS
		gpio_189	3	IO								
		safe_mode	7									

Table 2-1. Ball Characteristics(1) (continued)

BALL BOTTOM [1]	BALL TOP [2]	PIN NAME [3]	MODE [4]	TYPE [5]	BALL RESET STATE [6]	BALL RESET REL. STATE [7]	RESET REL. MODE [8]	POWER [9]	HYS [10]	BUFFER STRENGTH (mA) [11]	PULL U/D TYPE [12]	IO CELL [13]
AF8	-	sys_boot6	0	I	Z	Z	0	vdds_1p8v	Yes	4	PU/PD	LVCMOS
		dpm_emu18	1	O								
		gpio_wk9	3	IO								
		attila_hw_dbg12	6	O								
		safe_mode	7									
AE8	-	sys_boot7	0	I	Z	Z	0	vdds_1p8v	Yes	4	PU/PD	LVCMOS
		dpm_emu19	1	O								
		gpio_wk10	3	IO								
		attila_hw_dbg13	6	O								
		safe_mode	7									
AH2	-	jtag_ntrst	0	I	L	L	0	vdds_1p8v	Yes	4	PU/PD	LVCMOS
AG1	-	jtag_tck	0	I	L	L	0	vdds_1p8v	Yes	4	PU/PD	LVCMOS
		safe_mode	7									
AE3	-	jtag_rtck	0	O	L	0	0	vdds_1p8v	Yes	4	PU/PD	LVCMOS
AH1	-	jtag_tms_tmsc	0	IO	H	H	0	vdds_1p8v	Yes	4	PU/PD	LVCMOS
		safe_mode	7									
AE1	-	jtag_tdi	0	I	H	H	0	vdds_1p8v	Yes	4	PU/PD	LVCMOS
AE2	-	jtag_tdo	0	O	H	H	0	vdds_1p8v	Yes	4	PU/PD	LVCMOS
M2	-	dpm_emu0	0	IO	H	H	0	vdds_1p8v	Yes	4(17)	PU/PD	LVCMOS
		gpio_11	3	IO								
		attila_hw_dbg0	6	O								
		safe_mode	7									
N2	-	dpm_emu1	0	O	H	H	0	vdds_1p8v	Yes	4(17)	PU/PD	LVCMOS
		gpio_12	3	IO								
		attila_hw_dbg1	6	O								
		safe_mode	7									
P2	-	dpm_emu2	0	O	L	L	7	vdds_1p8v	Yes(18)	4(17)	PU/PD	LVCMOS
		usba0_ulpiphy_clk	1	I								
		gpio_13	3	IO								
		dispc2_fid	5	O								
		attila_hw_dbg2	6	O								
		safe_mode	7									

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Table 2-1. Ball Characteristics(1) (continued)

BALL BOTTOM [1]	BALL TOP [2]	PIN NAME [3]	MODE [4]	TYPE [5]	BALL RESET STATE [6]	BALL RESET REL. STATE [7]	RESET REL. MODE [8]	POWER [9]	HYS [10]	BUFFER STRENGTH (mA) [11]	PULL U/D TYPE [12]	IO CELL [13]
V1	-	dpm_emu3	0	O	L	L	7	vdds_1p8v	Yes	4(17)	PU/PD	LVCMOS
		usba0_ulpiphy_stp	1	O								
		gpio_14	3	IO								
		rfbi_data10	4	IO								
		dispc2_data10	5	O								
		attila_hw_dbg3	6	O								
		safe_mode	7									
V2	-	dpm_emu4	0	O	L	L	7	vdds_1p8v	Yes(18)	4(17)	PU/PD	LVCMOS
		usba0_ulpiphy_dir	1	I								
		gpio_15	3	IO								
		rfbi_data9	4	IO								
		dispc2_data9	5	O								
		attila_hw_dbg4	6	O								
		safe_mode	7									
W1	-	dpm_emu5	0	O	L	L	7	vdds_1p8v	Yes	4(17)	PU/PD	LVCMOS
		usba0_ulpiphy_nxt	1	I								
		gpio_16	3	IO								
		rfbi_te_vsync0	4	I								
		dispc2_data16	5	O								
		attila_hw_dbg5	6	O								
		safe_mode	7									
W2	-	dpm_emu6	0	O	L	L	7	vdds_1p8v	Yes	4(17)	PU/PD	LVCMOS
		usba0_ulpiphy_dat0	1	IO								
		uart3_tx_irtx	2	O								
		gpio_17	3	IO								
		rfbi_hsync0	4	I								
		dispc2_data17	5	O								
		attila_hw_dbg6	6	O								
		safe_mode	7									

Table 2-1. Ball Characteristics(1) (continued)

BALL BOTTOM [1]	BALL TOP [2]	PIN NAME [3]	MODE [4]	TYPE [5]	BALL RESET STATE [6]	BALL RESET REL. STATE [7]	RESET REL. MODE [8]	POWER [9]	HYS [10]	BUFFER STRENGTH (mA) [11]	PULL U/D TYPE [12]	IO CELL [13]
W3	-	dpm_emu7	0	O	L	L	7	vdds_ 1p8v	Yes	4(17)	PU/ PD	LVCMOS
		usba0_ ulpiphy_dat1	1	IO								
		uart3_rx_irrx	2	I								
		gpio_18	3	IO								
		rfbi_cs0	4	O								
		dispc2_hsync	5	O								
		attila_hw_ dbg7	6	O								
		safe_mode	7									
W4	-	dpm_emu8	0	O	L	L	7	vdds_ 1p8v	Yes	4(17)	PU/ PD	LVCMOS
		usba0_ ulpiphy_dat2	1	IO								
		uart3_rts_sd	2	O								
		gpio_19	3	IO								
		rfbi_re	4	O								
		dispc2_pclk	5	O								
		attila_hw_ dbg8	6	O								
		safe_mode	7									
Y2	-	dpm_emu9	0	O	L	L	7	vdds_ 1p8v	Yes	4(17)	PU/ PD	LVCMOS
		usba0_ ulpiphy_dat3	1	IO								
		uart3_cts_ rctx	2	IO								
		gpio_20	3	IO								
		rfbi_we	4	O								
		dispc2_vsync	5	O								
		attila_hw_ dbg9	6	O								
		safe_mode	7									
Y3	-	dpm_emu10	0	O	L	L	7	vdds_ 1p8v	Yes	4(17)	PU/ PD	LVCMOS
		usba0_ ulpiphy_dat4	1	IO								
		gpio_21	3	IO								
		rfbi_a0	4	O								
		dispc2_de	5	O								
		attila_hw_ dbg10	6	O								
		safe_mode	7									
Y4	-	dpm_emu11	0	O	L	L	7	vdds_ 1p8v	Yes	4(17)	PU/ PD	LVCMOS
		usba0_ ulpiphy_dat5	1	IO								
		gpio_22	3	IO								
		rfbi_data8	4	IO								
		dispc2_data8	5	O								
		attila_hw_ dbg11	6	O								
		safe_mode	7									

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Table 2-1. Ball Characteristics[(1)] (continued)

BALL BOTTOM [1]	BALL TOP [2]	PIN NAME [3]	MODE [4]	TYPE [5]	BALL RESET STATE [6]	BALL RESET REL. STATE [7]	RESET REL. MODE [8]	POWER [9]	HYS [10]	BUFFER STRENGTH (mA) [11]	PULL U/D TYPE [12]	IO CELL [13]
AA1	-	dpm_emu12	0	O	L	L	7	vdds_ 1p8v	Yes	4[(17)]	PU/ PD	LVCMOS
		usba0_ ulpiphy_dat6	1	IO								
		gpio_23	3	IO								
		rfbi_data7	4	IO								
		dispc2_data7	5	O								
		attila_hw_ dbg12	6	O								
		safe_mode	7									
AA2	-	dpm_emu13	0	O	L	L	7	vdds_ 1p8v	Yes	4[(17)]	PU/ PD	LVCMOS
		usba0_ ulpiphy_dat7	1	O								
		gpio_24	3	IO								
		rfbi_data6	4	IO								
		dispc2_data6	5	O								
		attila_hw_ dbg13	6	O								
		safe_mode	7									
AA3	-	dpm_emu14	0	O	L	L	7	vdds_ 1p8v	Yes	4[(17)]	PU/ PD	LVCMOS
		sys_drm_ msecure	1	O								
		uart1_rx	2	I								
		gpio_25	3	IO								
		rfbi_data5	4	IO								
		dispc2_data5	5	O								
		attila_hw_ dbg14	6	O								
		safe_mode	7									
AA4	-	dpm_emu15	0	O	L	L	7	vdds_ 1p8v	Yes	4[(17)]	PU/ PD	LVCMOS
		sys_secure_ indicator	1	O								
		gpio_26	3	IO								
		rfbi_data4	4	IO								
		dispc2_data4	5	O								
		attila_hw_ dbg15	6	O								
		safe_mode	7									
AB2	-	dpm_emu16	0	O	L	L	7	vdds_ 1p8v	Yes	4[(17)]	PU/ PD	LVCMOS Dual Voltage SubLVDS
		dmtimer8_ pwm_evt	1	IO								
		dsi1_te0	2	IDS								
		gpio_27	3	IO								
		rfbi_data3	4	IO								
		dispc2_data3	5	O								
		attila_hw_ dbg16	6	O								
		safe_mode	7									

Table 2-1. Ball Characteristics[(1)] (continued)

BALL BOTTOM [1]	BALL TOP [2]	PIN NAME [3]	MODE [4]	TYPE [5]	BALL RESET STATE [6]	BALL RESET REL. STATE [7]	RESET REL. MODE [8]	POWER [9]	HYS [10]	BUFFER STRENGTH (mA) [11]	PULL U/D TYPE [12]	IO CELL [13]
AB3	-	dpm_emu17	0	O	L	L	7	vdds_ 1p8v	Yes	4[(17)]	PU/ PD	LVCMOS Dual Voltage SubLVDS
		dmtimer9_ pwm_evt	1	IO								
		dsi1_te1	2	IDS								
		gpio_28	3	IO								
		rfbi_data2	4	IO								
		dispc2_data2	5	O								
		attila_hw_ dbg17	6	O								
		safe_mode	7									
AB4	-	dpm_emu18	0	O	L	L	7	vdds_ 1p8v	Yes	4[(17)]	PU/ PD	LVCMOS Dual Voltage SubLVDS
		dmtimer10_ pwm_evt	1	IO								
		dsi2_te0	2	IDS								
		gpio_190	3	IO								
		rfbi_data1	4	IO								
		dispc2_data1	5	O								
		attila_hw_ dbg18	6	O								
		safe_mode	7									
AC4	-	dpm_emu19	0	O	L	L	7	vdds_ 1p8v	Yes	4[(17)]	PU/ PD	LVCMOS Dual Voltage SubLVDS
		dmtimer11_ pwm_evt	1	IO								
		dsi2_te1	2	IDS								
		gpio_191	3	IO								
		rfbi_data0	4	IO								
		dispc2_data0	5	O								
		attila_hw_ dbg19	6	O								
		safe_mode	7									

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Table 2-1. Ball Characteristics(1) (continued)

BALL BOTTOM [1]	BALL TOP [2]	PIN NAME [3]	MODE [4]	TYPE [5]	BALL RESET STATE [6]	BALL RESET REL. STATE [7]	RESET REL. MODE [8]	POWER [9]	HYS [10]	BUFFER STRENGTH (mA) [11]	PULL U/D TYPE [12]	IO CELL [13]
H1 / M1 / AB1 / C2 / F2 / K2 / U2 / AF2 / B3 / J3 / J4 / AG4 / B6 / K8 / U8 / AH8 / N9 / A10 / AH10 / H11 / AA11 / N12 / P12 / R12 / T12 / U12 / AA12 / B13 / H13 / M13 / N13 / P13 / R13 / T13 / U13 / AH13 / M14 / N14 / P14 / R14 / T14 / U14 / M15 / N15 / P15 / R15 / T15 / U15 / M16 / N16 / P16 / R16 / T16 / U16 / H17 / M17 / N17 / P17 / R17 / T17 / U17 / Y17 / AG17 / H19 / A20 / AA20 / J21 / L21 / M21 / U21 / AH21 / M22 / A23 / F25 / L25 / Y25 / L26 / Y26 / AG26 / B27 / AE27 / H28 / K28 / U28	A2 / A6 / A9 / A11 / A14 / A28 / B1 / B14 / B21 / B24 / B29 / E28 / F1 / H28 / J1 / L29 / M2 / P1 / P2 / R28 / V2 / V28 / AA28 / AB2 / AE2 / AF28 / AH1 / AH5 / AH14 / AH18 / AH29 / AJ2 / AJ7 / AJ11 / AJ16 / AJ22 / AJ28	vss	-	GND	NA	NA	NA	NA	NA	NA	NA	NA
Y22	-	vpp(21)	-	PWR	NA	NA	NA	NA	NA	NA	NA	NA
J8	-	vpp_cust(21)	-	PWR	NA	NA	NA	NA	NA	NA	NA	NA

Table 2-1. Ball Characteristics(1) (continued)

BALL BOTTOM [1]	BALL TOP [2]	PIN NAME [3]	MODE [4]	TYPE [5]	BALL RESET STATE [6]	BALL RESET REL. STATE [7]	RESET REL. MODE [8]	POWER [9]	HYS [10]	BUFFER STRENGTH (mA) [11]	PULL U/D TYPE [12]	IO CELL [13]
J9 / K9 / L9 / M9 / T9 / J10 / J11 / Y11 / H12 / J12 / Y12 / J13 / Y13 / AA13 / J15 / J16 / J17 / H18 / J18 / J19 / J20 / K20 / L20 / M20 / N20 / R20 / T20 / U20 / V20	-	vdd_core	-	PWR	NA	NA	NA	NA	NA	NA	NA	NA
V8 / W8 / Y8 / U9 / V9 / W9 / Y9 / Y10 / AA10	-	vdd_mpu	-	PWR	NA	NA	NA	NA	NA	NA	NA	NA
AA17 / Y18 / AA18 / Y19 / AA19 / W20 / Y20 / V21 / W21 / Y21	-	vdd_iva_audio	-	PWR	NA	NA	NA	NA	NA	NA	NA	NA
AA16	-	vdds_1p2v	-	PWR	NA	NA	NA	NA	NA	NA	NA	NA
AB7 / U7 / V7 / K7 / H22 / J22 / W22	-	vdds_1p8v	-	PWR	NA	NA	NA	NA	NA	NA	NA	NA
Y7	-	vdds_1p8_fref	-	PWR	NA	NA	NA	NA	NA	NA	NA	NA
D1 / G1 / U1 / Y1 / AC1 / AF1 / A4 / AH4 / A6 / L7 / G8 / H8 / L8 / M8 / AA8 / A9 / H9 / AA9 / AB9 / AH9 / A12 / AH12 / A17 / H20 / G21 / H21 / A22 / A25 / E28 / J28 / L28	A22 / B4 / B7 / B9 / B13 / B18 / B25 / D2 / D29 / F29 / G2 / J2 / J28 / M28 / U1 / Y1 / AC1 / AF2 / AH9 / AH12 / AJ4 / AJ6	vddq_lpddr2	-	PWR	NA	NA	NA	NA	NA	NA	NA	NA
G15	-	vddq_vref_lpddr21	-	PWR	NA	NA	NA	NA	NA	NA	NA	NA

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Table 2-1. Ball Characteristics(1) (continued)

BALL BOTTOM [1]	BALL TOP [2]	PIN NAME [3]	MODE [4]	TYPE [5]	BALL RESET STATE [6]	BALL RESET REL. STATE [7]	RESET REL. MODE [8]	POWER [9]	HYS [10]	BUFFER STRENGTH (mA) [11]	PULL U/D TYPE [12]	IO CELL [13]
T8	-	vddq_vref_ lpddr22	-	PWR	NA	NA	NA	NA	NA	NA	NA	NA
AH18 / AH20 / AA21 / AB21 / AA22 / AB22 / AH25 / T28 / AB28 / AD28	T28 / AC28 / AE29 / AH22 / AJ19 / AJ26	vddca_lpddr2	-	PWR	NA	NA	NA	NA	NA	NA	NA	NA
Y14	-	vddca_vref_ lpddr21	-	PWR	NA	NA	NA	NA	NA	NA	NA	NA
R27	-	vddca_vref_ lpddr22	-	PWR	NA	NA	NA	NA	NA	NA	NA	NA
G22	-	vdda_dll0_ lpddr21	-	PWR	NA	NA	NA	NA	NA	NA	NA	NA
G9	-	vdda_dll1_ lpddr21	-	PWR	NA	NA	NA	NA	NA	NA	NA	NA
M7	-	vdda_dll0_ lpddr22	-	PWR	NA	NA	NA	NA	NA	NA	NA	NA
AB10	-	vdda_dll1_ lpddr22	-	PWR	NA	NA	NA	NA	NA	NA	NA	NA
L1	-	vdda_dsi1	-	PWR	NA	NA	NA	NA	NA	NA	NA	PHY
N8 / P8	-	vssa_dsi	-	GND	NA	NA	NA	NA	NA	NA	NA	PHY
L2	-	vdda_dsi2	-	PWR	NA	NA	NA	NA	NA	NA	NA	PHY
W28	-	vdda_csi21	-	PWR	NA	NA	NA	NA	NA	NA	NA	PHY
R22	-	vssa_csi2	-	GND	NA	NA	NA	NA	NA	NA	NA	PHY
V28	-	vdda_csi22	-	PWR	NA	NA	NA	NA	NA	NA	NA	PHY
A11 / G12	-	vdda_hdmi_ vdac	-	PWR	NA	NA	NA	NA	NA	NA	NA	PHY
G11	-	vssa_hdmi_ vdac	-	GND	NA	NA	NA	NA	NA	NA	NA	PHY
A5	-	vdda_ usba0otg_ 3p3v	-	PWR	NA	NA	NA	NA	NA	NA	NA	PHY
G10	-	vssa_ usba0otg_ 3p3v	-	GND	NA	NA	NA	NA	NA	NA	NA	PHY
A7	-	vdda_ usba0otg_ 1p8v	-	PWR	NA	NA	NA	NA	NA	NA	NA	PHY
H10	-	vssa_ usba0otg	-	GND	NA	NA	NA	NA	NA	NA	NA	PHY
J7	-	vdds_usim	-	PWR	NA	NA	NA	NA	NA	NA	NA	NA
A2	-	pbias_sim	-	PWR	NA	NA	NA	NA	NA	NA	NA	NA
G7 / H7	-	vdds_ sdmmc1	-	PWR	NA	NA	NA	NA	NA	NA	NA	NA
A1	-	pbias_mmc1	-	PWR	NA	NA	NA	NA	NA	NA	NA	NA
P9	-	vdda_dpll_ mpu	-	PWR	NA	NA	NA	NA	NA	NA	NA	NA
G13	-	vdda_dpll_ core_audio	-	PWR	NA	NA	NA	NA	NA	NA	NA	NA

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Table 2-1. Ball Characteristics(1) (continued)

BALL BOTTOM [1]	BALL TOP [2]	PIN NAME [3]	MODE [4]	TYPE [5]	BALL RESET STATE [6]	BALL RESET REL. STATE [7]	RESET REL. MODE [8]	POWER [9]	HYS [10]	BUFFER STRENGTH (mA) [11]	PULL U/D TYPE [12]	IO CELL [13]
Y16	-	vdda_dpll_ iva_per	-	PWR	NA	NA	NA	NA	NA	NA	NA	NA
G20	-	vdds_dv_ gpmc	-	PWR	NA	NA	NA	NA	NA	NA	NA	NA
G16 / H16	-	vdds_dv_ sdmmc2	-	PWR	NA	NA	NA	NA	NA	NA	NA	NA
G17 / G18 / G19	-	vdds_dv_c2c	-	PWR	NA	NA	NA	NA	NA	NA	NA	NA
V22	-	vdds_dv_cam	-	PWR	NA	NA	NA	NA	NA	NA	NA	NA
AB16	-	vdds_dv_ bank0	-	PWR	NA	NA	NA	NA	NA	NA	NA	NA
AB20	-	vdds_dv_ bank1	-	PWR	NA	NA	NA	NA	NA	NA	NA	NA
AB8 / AB19	-	vdds_dv_ bank2	-	PWR	NA	NA	NA	NA	NA	NA	NA	NA
AB18	-	vdds_dv_ bank3	-	PWR	NA	NA	NA	NA	NA	NA	NA	NA
AA7	-	vdds_dv_ bank4	-	PWR	NA	NA	NA	NA	NA	NA	NA	NA
AB17	-	vdds_dv_ bank5	-	PWR	NA	NA	NA	NA	NA	NA	NA	NA
AA14	-	vdds_dv_ bank6	-	PWR	NA	NA	NA	NA	NA	NA	NA	NA
M28	-	vdds_dv_ bank7	-	PWR	NA	NA	NA	NA	NA	NA	NA	NA
W7	-	vdds_dv_fref	-	PWR	NA	NA	NA	NA	NA	NA	NA	NA
AB14	-	vdda_ldo_ sram_mpu	-	PWR	NA	NA	NA	NA	NA	NA	NA	NA
N22	-	vdda_ldo_ sram_iva_ audio	-	PWR	NA	NA	NA	NA	NA	NA	NA	NA
T22	-	vdda_ldo_ sram_core	-	PWR	NA	NA	NA	NA	NA	NA	NA	NA
P7	-	vdda_ldo_ emu_wkup	-	PWR	NA	NA	NA	NA	NA	NA	NA	NA
AB12	-	vdda_bdgp_ vbb	-	PWR	NA	NA	NA	NA	NA	NA	NA	NA
AB13	-	cap_vbb_ldo _mpu	-	PWR	NA	NA	NA	NA	NA	NA	NA	NA
R21	-	cap_vbb_ldo _iva_audio	-	PWR	NA	NA	NA	NA	NA	NA	NA	NA
AB11	-	cap_vdd_ldo _sram_mpu	-	PWR	NA	NA	NA	NA	NA	NA	NA	NA
N21	-	cap_vdd_ldo _sram_iva_ audio	-	PWR	NA	NA	NA	NA	NA	NA	NA	NA
U22	-	cap_vdd_ldo _sram_core	-	PWR	NA	NA	NA	NA	NA	NA	NA	NA
T7	-	cap_vdd_ldo _emu_wkup	-	PWR	NA	NA	NA	NA	NA	NA	NA	NA
A27	-	atestv	-	AO	Z	NA	0	vdds_ 1p8v	NA	NA	NA	Analog
AG28	-	vsense	-	AO	Z	NA	0	NA	NA	NA	NA	Analog

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Table 2-1. Ball Characteristics(1) (continued)

BALL BOTTOM [1]	BALL TOP [2]	PIN NAME [3]	MODE [4]	TYPE [5]	BALL RESET STATE [6]	BALL RESET REL. STATE [7]	RESET REL. MODE [8]	POWER [9]	HYS [10]	BUFFER STRENGTH (mA) [11]	PULL U/D TYPE [12]	IO CELL [13]
AH27	-	iforce	-	AI	Z	NA	0	NA	No	NA	No	Analog
AH16	AJ17	pop_lpddr21_zq	-	FEED	NA	NA	NA	NA	NA	NA	NA	NA
AF28	AG29	pop_lpddr22_zq	-	FEED	NA	NA	NA	NA	NA	NA	NA	NA
A26 / B2	B2 / B28	pop_vacc_lpddr2	-	PWR	NA	NA	NA	NA	NA	NA	NA	NA
AG27 / C1 / AG2	C1 / AH2 / AH28	pop_vdd1_lpddr2_shared	-	PWR	NA	NA	NA	NA	NA	NA	NA	NA
A13 / C27 / AH14	A15 / C28 / AJ15	pop_vdd1_lpddr21	-	PWR	NA	NA	NA	NA	NA	NA	NA	NA
N1 / P1 / R28	N2 / P29 / R1	pop_vdd1_lpddr22	-	PWR	NA	NA	NA	NA	NA	NA	NA	NA
AH3 / A3 / C28 / AF27	A3 / C29 / AG28 / AH3	pop_vdd2_lpddr2_shared	-	PWR	NA	NA	NA	NA	NA	NA	NA	NA
AG14 / A15 / B15	A16 / B16 / AH15	pop_vdd2_lpddr21	-	PWR	NA	NA	NA	NA	NA	NA	NA	NA
N28 / T1 / T2	P28 / T1 / T2	pop_vdd2_lpddr22	-	PWR	NA	NA	NA	NA	NA	NA	NA	NA

(1) NA stands for Not Applicable.

(2) x and y = 20 to 70 µA

(3) x and y = 40 to 70 µA

(4) The cell is provided with the flexibility of selecting optimal voltage level based on the current load requirement among 2 µA, 4 µA, 6 µA, or 8 µA.

(5) From ES2.2, BALL RESET RELEASE STATE = H.
Before ES2.2 (that is, for ES2.0 and ES2.1), BALL RESET RELEASE STATE = Z.

(6) The pullup or pulldown can be either the standard LVCMOS 100-µA drive strength or the configurable I^2C internal pullup resistances. The default buffer configuration is the following:
- PUx/PDy-OD is specified: the default buffer configuration is High-Speed I^2C point-to-point mode using internal pullup resistance.
- PUx/PDy-GPIO is specified: the default buffer configuration is standard LVCMOS mode (non-I^2C). The internal pullup resistance programming does not apply in this mode.

In I^2C mode configuration, for a full description of the internal pullup resistance programming according to the load range, see the CONTROL_I2C_0 and CONTROL_I2C_2 registers in the Control Module / Control Module Functional Description / Functional Register Description / Signal Integrity Parameter Control Registers With Pad Group Assignment section of the OMAP4430 TRM.
In standard LVCMOS mode configuration (non-I^2C mode), for a full description of the pullup or pulldown programming, see the CONTROL_CORE_PADX registers in the Control Module / Control Module Functional Description / Pad Functional Multiplexing and Configuration section of the OMAP4430 TRM.

(7) The drive strength is fixed regardless of the load. The driver is designed to drive 75 Ω for video applications.

(8) In buffer mode, the drive strength is fixed regardless of the load. The driver is designed to drive 75 Ω for video applications. In bypass mode, the drive strength is 0.47 mA.

(9) PAD can be driven low or high impedance by the driver. External pullup is required and can vary between 1 kΩ and 10 kΩ. The circuitry pulling up or pulling down the pad must be able to provide at least 100 µA of current without collapsing.

(10) PD: 30 kΩ to 150 kΩ. PU: 50 kΩ to 110 kΩ

(11) Nominal impedance:
- 1.8-V mode: PU = 48 Ω / PD = 45 Ω
- 1.2-V mode: PU = 51 Ω / PD = 51 Ω

Impedance spread:
- 1.8-V mode: PU = 30 to 92 Ω / PD = 30 to 83 Ω
- 1.2-V mode: PU = 35 to 86 Ω / PD = 36 to 74 Ω

(12) The maximum capacitive load for the DSI low-power mode is equal to 60 pF. See Chapter 8 of the MIPI D-PHY standard v1.0 for complete specification on the electrical characteristics.
No specific capacitive load is needed in DSI high-speed mode.
The PCB interconnect must be 50-Ω transmission line on DSI dsi_dx[2;0] and DSI dsi_dy[2;0]. DSI dsi_dx[2;0] and DSI dsi_dy[2;0] lines must be well matched. See Chapter 7 of the MIPI D-PHY standard v1.0 for complete specification of the interconnect.

(13) The buffer strength of this IO cell is programmable (2.5, 5, 7.5, or 10 mA); the default value is described in the table above.

(14) IO drive strength for D+ (usba0_otg_dp) and D– (usba0_otg_dm): minimum 18.3 mA, maximum 89 mA (for a power supply vdda_usba0otg_3p3v = 3.6 V).
Ball characteristics are compliant with USB2.0.

(15) PU = minimum 900 Ω, maximum 3.090 kΩ and PD = minimum 14.25 kΩ, maximum 24.8 kΩ. Note that:
– PU is typically connected for D+ (usba0_otg_dp) in Full Speed mode and for D– (usba0_otg_dm) in Low Speed mode.
– PD is typically connected for D+ (usba0_otg_dp) and D– (usba0_otg_dm) whatever the modes. PD is connected to both D+ and D– only if OMAP4 is used as HOST.
Ball characteristics are compliant with USB2.0.

(16) For H2 / H3 / H4 / D2 / E3 / E4 / E2 / E1 / F4 / F3 / F1 / G2 / G4 / G3 / J2 balls, the hysteresis value is equal to 100 mV minimum for 1.8 V (vdds_mmc1 or vdds_usim following the interface used), or 50 mV minimum for 3.0 V (vdds_mmc1 or vdds_usim following the interface used).

(17) The buffer drive strength is configurable by software programming:
– Mode 2: DS0 = 0, impedance = 50 Ω (buffer drive strength = 4 mA, IO_L = IO_H = 4 mA)
– Mode 1: DS0 = 1, impedance = 25 Ω (buffer drive strength = 8 mA, IO_L = IO_H = 8 mA)
In the BUFFER STRENGTH (mA) [11] column is defined the value by default.
For more information regarding the DS0 programming, see the CONTROL_SMART2IO_PADCONF_2 register in the Control Module / Control Module Functional Description / Functional Register Description / Signal Integrity Parameter Control Registers With Pad Group Assignment section of the OMAP4430 TRM.
For more information regarding the load, rise / fall times vs frequency depending the modes (DS0 = 0 or 1) or the supply voltage value (1.2 V or 1.8 V), see Table 3-5, *GPMC DC Electrical Characteristics*.

(18) For AE18 / AG12 balls, the hysteresis value is equal to 70 mV minimum for 1.8 V and 60 mV minimum for 1.2 V. For P2 / V2 balls, the hysteresis value is equal to 70 mV minimum for 1.8 V.

(19) For more information regarding the MIPI D-PHY hysteresis, see Section 3.3.3, *Camera DC Electrical Characteristics*, Section 3.3.4, *Display DC Electrical Characteristics*.

(20) For B5 / B4 balls, the hysteresis is:
– In low-speed and full-speed single-ended receiver modes: minimum 20 mV, typical 50 mV, maximum 80 mV
– In differential receiver modes, no hysteresis feature is present.

(21) vpp must be unconnected. vpp_cust is only powered when programming CPFROM eFuses. Otherwise, it is recommended to leave vpp_cust turned off (floating). Note that if the TWL6030 PMIC is used then the vpp pulldown resistor inside the TWL6030 must be disabled when the vpp_cust is turned off.

(22) IO drive strength for usba0_otg_ce pin: minimum 100 µA, maximum 20 mA.

(23) If a CSI2 serial PHY is enabled, vdda_csi2 must be supplied by a dedicated 1.8-V low-noise power source.
If a CSI2 serial PHY is definitively disabled, other multiplexed 1.8-V CMOS signals of the interface can be enabled, the interface can be supplied by the same power source as vdds_1p8v: the vdds_1p8v power source supplies vdda_csi2 ball.
If CSI2 serial PHY and CMOS signals are definitively disabled, the interface balls are left unconnected with its associated power supply (vdda/vssa) grounded (for circuit reliability reasons).

(24) If a DSI serial PHY is enabled, vdda_dsi must be supplied by a dedicated 1.8-V low-noise power source.
If a DSI serial PHY is definitively disabled, the interface balls are left unconnected and in that case the associated power supply (vdda/vssa) can be grounded (for circuit reliability reasons) only if the corresponding DSI DPLL is never used to generate the functional clock to the DISPC.

(25) If the HDMI serial PHY or DAC are definitively disabled, the interface balls are left unconnected with its associated power supply (vdda/vssa) grounded (for circuit reliability reasons).

(26) If the HS USB OTG PHY is enabled, vdda_usba0otg_3p3v and vdda_usba0otg_1p8v must be supplied by dedicated 3.3-V and 1.8-V low-noise power sources.
If the USB OTG PHY is definitively disabled, other multiplexed 3.3-V CMOS signals of the interface can be enabled, vdda_usba0otg_3p3v must be supplied by a dedicated 3.3-V power source and vdda_usba0otg_1p8v can be supplied by the same power source as vdds_1p8v.
If the USB OTG PHY and CMOS signals are definitively disabled, vdda_usba0otg_3p3v and vdda_usba0otg_1p8v are grounded for power saving and there is a forward-biased diode from usba0_otg_dp, usba0_otg_dm, usba0_otg_ce pins to vdda_usba0otg_3p3v pin.

(27) If the SDMMC1 functional signals are enabled, vdds_sdmmc1 must be supplied by either dedicated 1.8-V or 3.0-V power source.
If the SDMMC1 functional signals are definitively disabled, other multiplexed 1.8-V CMOS signals of the interface can be enabled, the interface can be supplied by the same power source as vdds_1p8v: the vdds_1p8v power source supplies vdds_sdmmc1.
If the SDMMC1 functional balls and CMOS signals are definitively disabled, the interface balls are left unconnected with its associated power supply (vdds_sdmmc1) grounded (for circuit reliability reasons).
For the corresponding setting of the MMC1_PWRDNZ bit (MMC1_IO_PWRDNZ signal) and the MMC1_PBIASLITE_PWRDNZ bit (MMC1_PBIAS_PWRDNZ signal), see the Control Module / Control Module Functional Description / Extended-Drain I/O and PBIAS Cell section and the Control Module / Control Module Programming Guide section of the OMAP4430 TRM.

(28) If USIM, USBC1 functional signals are enabled, vdds_usim must be supplied by either dedicated 1.8-V or 3.0-V power source.
If USIM, USBC1 functional signals are definitively disabled, other multiplexed 1.8-V CMOS signals of the interface can be enabled, the

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interface can be supplied by the same power source as vdds_1p8v: the vdds_1p8v power source supplies vdds_usim ball.
If the USIM, USBC1 functional balls and CMOS signals are definitively disabled, the interface balls are left unconnected with its associated power supply (vdds_usim) grounded (for circuit reliability reasons).
For the corresponding setting of the GPIOWK_IO_PWRDNZ bit (GPIOWK_IO_PWRDNZ signal), the USBC1_ICUSB_PWRDNZ bit (USBC1_ICUSB_IO_PWRDNZ signal) and the PBIASLITE1_PWRDNZ bit (PBIAS1_PWRDNZ signal), see the Control Module / Control Module Functional Description / Extended-Drain I/O and PBIAS Cell section and the Control Module / Control Module Programming Guide section of the OMAP4430 TRM.

(29) The function (data or clock) supported on each lane is programmable. For more information on HDMI, please contact your TI representative.

(30) The HDMI pulldown resistor is only enabled when the HDMI supply is either ramping or off. Hence, this pulldown resistor is not linked to the HDMI standard protocol.

2.3 Multiplexing Characteristics

Table 2-2 describes the device multiplexing (no characteristics are available in this table).

NOTE

This table doesn't take into account subsystem multiplexing signals. Subsystem multiplexing signals are described in Section 2.4, *Signal Descriptions*.

NOTE

For more information, see the Control Module / Control Module Functional Description / PAD Functional Multiplexing and Configuration section of the OMAP4430 TRM.

NOTE

Configuring two pins to the same input signal is not supported as it can yield unexpected results. This can be easily prevented with the proper software configuration. (safe_mode is not an input signal.)

NOTE

When a pad is set into a multiplexing mode which is not defined by pin multiplexing, this pad is actually set undriven (HiZ) with potential pullup / pulldown. Pulls need to be disabled to have a pure HiZ.

NOTE

All balls not described in Table 2-1 and Table 2-2 are not connected.

Table 2-2. Multiplexing Characteristics(1)

BALL BOTTOM	BALL TOP	Mode 0	Mode 1	Mode 2	Mode 3	Mode 4	Mode 5	Mode 6	Mode 7
C12	-	gpmc_ad0	sdmmc2_dat0	-	-	-	-	-	-
D12	-	gpmc_ad1	sdmmc2_dat1	-	-	-	-	-	-
C13	-	gpmc_ad2	sdmmc2_dat2	-	-	-	-	-	-
D13	-	gpmc_ad3	sdmmc2_dat3	-	-	-	-	-	-
C15	-	gpmc_ad4	sdmmc2_dat4	sdmmc2_dir_dat0	-	-	-	-	-
D15	-	gpmc_ad5	sdmmc2_dat5	sdmmc2_dir_dat1	-	-	-	-	-

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Table 2-2. Multiplexing Characteristics[(1)] (continued)

BALL BOTTOM	BALL TOP	Mode 0	Mode 1	Mode 2	Mode 3	Mode 4	Mode 5	Mode 6	Mode 7
A16	-	gpmc_ad6	sdmmc2_dat6	sdmmc2_dir_cmd	-	-	-	-	-
B16	-	gpmc_ad7	sdmmc2_dat7	sdmmc2_clk_fdbk	-	-	-	-	-
C16	-	gpmc_ad8	kpd_row0	-	gpio_32	-	sdmmc1_dat0	-	-
D16	-	gpmc_ad9	kpd_row1	-	gpio_33	-	sdmmc1_dat1	-	-
C17	-	gpmc_ad10	kpd_row2	-	gpio_34	-	sdmmc1_dat2	-	-
D17	-	gpmc_ad11	kpd_row3	-	gpio_35	-	sdmmc1_dat3	-	-
C18	-	gpmc_ad12	kpd_col0	-	gpio_36	-	sdmmc1_dat4	-	-
D18	-	gpmc_ad13	kpd_col1	-	gpio_37	-	sdmmc1_dat5	-	-
C19	-	gpmc_ad14	kpd_col2	-	gpio_38	-	sdmmc1_dat6	-	-
D19	-	gpmc_ad15	kpd_col3	-	gpio_39	-	sdmmc1_dat7	-	-
B17	-	gpmc_a16	kpd_row4	-	gpio_40	venc_656_data0	-	-	safe_mode
A18	-	gpmc_a17	kpd_row5	-	gpio_41	venc_656_data1	-	-	safe_mode
B18	-	gpmc_a18	kpd_row6	-	gpio_42	venc_656_data2	-	-	safe_mode
A19	-	gpmc_a19	kpd_row7	-	gpio_43	venc_656_data3	-	-	safe_mode
B19	-	gpmc_a20	kpd_col4	-	gpio_44	venc_656_data4	-	-	safe_mode
B20	-	gpmc_a21	kpd_col5	-	gpio_45	venc_656_data5	-	-	safe_mode
A21	-	gpmc_a22	kpd_col6	-	gpio_46	venc_656_data6	-	-	safe_mode
B21	-	gpmc_a23	kpd_col7	-	gpio_47	venc_656_data7	-	-	safe_mode
C20	-	gpmc_a24	kpd_col8	-	gpio_48	-	-	-	safe_mode
D20	-	gpmc_a25	-	-	gpio_49	-	-	-	safe_mode
B25	-	gpmc_ncs0	-	-	gpio_50	sys_ndmareq0	-	-	-
C21	-	gpmc_ncs1	-	-	gpio_51	-	-	-	safe_mode
D21	-	gpmc_ncs2	kpd_row8	-	gpio_52	-	-	-	safe_mode
C22	-	gpmc_ncs3	gpmc_dir	-	gpio_53	-	-	-	safe_mode
C25	-	gpmc_nwp	dsi1_te0	-	gpio_54	sys_ndmareq1	-	-	-
B22	-	gpmc_clk	-	-	gpio_55	sys_ndmareq2	sdmmc1_cmd	-	-
D25	-	gpmc_nadv_ale	dsi1_te1	-	gpio_56	sys_ndmareq3	sdmmc1_clk	-	-
B11	-	gpmc_noe	sdmmc2_clk	-	-	-	-	-	-
B12	-	gpmc_nwe	sdmmc2_cmd	-	-	-	-	-	-
C23	-	gpmc_nbe0_cle	dsi2_te0	-	gpio_59	-	-	-	-

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Table 2-2. Multiplexing Characteristics[(1)] (continued)

BALL BOTTOM	BALL TOP	Mode 0	Mode 1	Mode 2	Mode 3	Mode 4	Mode 5	Mode 6	Mode 7
D22	-	gpmc_nbe1	-	-	gpio_60	-	-	-	safe_mode
B26	-	gpmc_wait0	dsi2_te1	-	gpio_61	-	-	-	-
B23	-	gpmc_wait1	-	-	gpio_62	-	-	-	safe_mode
D23	-	gpmc_wait2	usbc1_icusb_txen	-	gpio_100	sys_ndmareq0	-	-	safe_mode
A24	-	gpmc_ncs4	dsi1_te0	-	gpio_101	sys_ndmareq1	-	-	safe_mode
B24	-	gpmc_ncs5	dsi1_te1	-	gpio_102	sys_ndmareq2	-	-	safe_mode
C24	-	gpmc_ncs6	dsi2_te0	-	gpio_103	sys_ndmareq3	-	-	safe_mode
D24	-	gpmc_ncs7	dsi2_te1	-	gpio_104	-	-	-	safe_mode
-	E29	lpddr21_dq0	-	-	-	-	-	-	-
-	D28	lpddr21_dq1	-	-	-	-	-	-	-
-	B27	lpddr21_dq2	-	-	-	-	-	-	-
-	A27	lpddr21_dq3	-	-	-	-	-	-	-
-	A26	lpddr21_dq4	-	-	-	-	-	-	-
-	B26	lpddr21_dq5	-	-	-	-	-	-	-
-	A25	lpddr21_dq6	-	-	-	-	-	-	-
-	A24	lpddr21_dq7	-	-	-	-	-	-	-
-	B19	lpddr21_dq8	-	-	-	-	-	-	-
-	A19	lpddr21_dq9	-	-	-	-	-	-	-
-	A18	lpddr21_dq10	-	-	-	-	-	-	-
-	A17	lpddr21_dq11	-	-	-	-	-	-	-
-	B17	lpddr21_dq12	-	-	-	-	-	-	-
-	A13	lpddr21_dq13	-	-	-	-	-	-	-
-	A12	lpddr21_dq14	-	-	-	-	-	-	-
-	B12	lpddr21_dq15	-	-	-	-	-	-	-
-	N28	lpddr21_dq16	-	-	-	-	-	-	-
-	N29	lpddr21_dq17	-	-	-	-	-	-	-
-	M29	lpddr21_dq18	-	-	-	-	-	-	-
-	L28	lpddr21_dq19	-	-	-	-	-	-	-
-	K28	lpddr21_dq20	-	-	-	-	-	-	-
-	K29	lpddr21_dq21	-	-	-	-	-	-	-
-	J29	lpddr21_dq22	-	-	-	-	-	-	-
-	H29	lpddr21_dq23	-	-	-	-	-	-	-
-	B8	lpddr21_dq24	-	-	-	-	-	-	-

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Table 2-2. Multiplexing Characteristics(1) (continued)

BALL BOTTOM	BALL TOP	Mode 0	Mode 1	Mode 2	Mode 3	Mode 4	Mode 5	Mode 6	Mode 7
-	A8	lpddr21_dq25	-	-	-	-	-	-	-
-	A7	lpddr21_dq26	-	-	-	-	-	-	-
-	B6	lpddr21_dq27	-	-	-	-	-	-	-
-	B5	lpddr21_dq28	-	-	-	-	-	-	-
-	A5	lpddr21_dq29	-	-	-	-	-	-	-
-	A4	lpddr21_dq30	-	-	-	-	-	-	-
-	B3	lpddr21_dq31	-	-	-	-	-	-	-
-	AJ27	lpddr21_ca0	-	-	-	-	-	-	-
-	AH27	lpddr21_ca1	-	-	-	-	-	-	-
-	AH26	lpddr21_ca2	-	-	-	-	-	-	-
-	AH25	lpddr21_ca3	-	-	-	-	-	-	-
-	AJ25	lpddr21_ca4	-	-	-	-	-	-	-
-	AJ20	lpddr21_ca5	-	-	-	-	-	-	-
-	AH20	lpddr21_ca6	-	-	-	-	-	-	-
-	AH19	lpddr21_ca7	-	-	-	-	-	-	-
-	AJ18	lpddr21_ca8	-	-	-	-	-	-	-
-	AH17	lpddr21_ca9	-	-	-	-	-	-	-
-	A23	lpddr21_dqs0	-	-	-	-	-	-	-
-	B23	lpddr21_ndqs0	-	-	-	-	-	-	-
-	A20	lpddr21_dqs1	-	-	-	-	-	-	-
-	B20	lpddr21_ndqs1	-	-	-	-	-	-	-
-	G28	lpddr21_dqs2	-	-	-	-	-	-	-
-	G29	lpddr21_ndqs2	-	-	-	-	-	-	-
-	B10	lpddr21_dqs3	-	-	-	-	-	-	-
-	A10	lpddr21_ndqs3	-	-	-	-	-	-	-
-	B22	lpddr21_dm0	-	-	-	-	-	-	-
-	A21	lpddr21_dm1	-	-	-	-	-	-	-
-	F28	lpddr21_dm2	-	-	-	-	-	-	-
-	B11	lpddr21_dm3	-	-	-	-	-	-	-
-	AJ21	lpddr21_ck	-	-	-	-	-	-	-
-	AH21	lpddr21_nck	-	-	-	-	-	-	-
AH28	AH24	lpddr21_ncs0	-	-	-	-	-	-	-
-	AJ24	lpddr21_ncs1	-	-	-	-	-	-	-
-	AH23	lpddr21_cke0	-	-	-	-	-	-	-

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Table 2-2. Multiplexing Characteristics[(1)] (continued)

BALL BOTTOM	BALL TOP	Mode 0	Mode 1	Mode 2	Mode 3	Mode 4	Mode 5	Mode 6	Mode 7
-	AJ23	lpddr21_cke1	-	-	-	-	-	-	-
-	AH16	lpddr21_vref_ca	-	-	-	-	-	-	-
-	B15	lpddr21_vref_dq	-	-	-	-	-	-	-
-	L2	lpddr22_dq0	-	-	-	-	-	-	-
-	M1	lpddr22_dq1	-	-	-	-	-	-	-
-	N1	lpddr22_dq2	-	-	-	-	-	-	-
-	U2	lpddr22_dq3	-	-	-	-	-	-	-
-	V1	lpddr22_dq4	-	-	-	-	-	-	-
-	W2	lpddr22_dq5	-	-	-	-	-	-	-
-	W1	lpddr22_dq6	-	-	-	-	-	-	-
-	Y2	lpddr22_dq7	-	-	-	-	-	-	-
-	AE1	lpddr22_dq8	-	-	-	-	-	-	-
-	AF1	lpddr22_dq9	-	-	-	-	-	-	-
-	AG1	lpddr22_dq10	-	-	-	-	-	-	-
-	AG2	lpddr22_dq11	-	-	-	-	-	-	-
-	AJ3	lpddr22_dq12	-	-	-	-	-	-	-
-	AH4	lpddr22_dq13	-	-	-	-	-	-	-
-	AJ5	lpddr22_dq14	-	-	-	-	-	-	-
-	AH6	lpddr22_dq15	-	-	-	-	-	-	-
-	C2	lpddr22_dq16	-	-	-	-	-	-	-
-	D1	lpddr22_dq17	-	-	-	-	-	-	-
-	E1	lpddr22_dq18	-	-	-	-	-	-	-
-	E2	lpddr22_dq19	-	-	-	-	-	-	-
-	F2	lpddr22_dq20	-	-	-	-	-	-	-
-	G1	lpddr22_dq21	-	-	-	-	-	-	-
-	H1	lpddr22_dq22	-	-	-	-	-	-	-
-	H2	lpddr22_dq23	-	-	-	-	-	-	-
-	AJ9	lpddr22_dq24	-	-	-	-	-	-	-
-	AJ10	lpddr22_dq25	-	-	-	-	-	-	-
-	AH10	lpddr22_dq26	-	-	-	-	-	-	-
-	AH11	lpddr22_dq27	-	-	-	-	-	-	-
-	AJ12	lpddr22_dq28	-	-	-	-	-	-	-

Table 2-2. Multiplexing Characteristics[(1)] (continued)

BALL BOTTOM	BALL TOP	Mode 0	Mode 1	Mode 2	Mode 3	Mode 4	Mode 5	Mode 6	Mode 7
-	AJ13	lpddr22_dq29	-	-	-	-	-	-	-
-	AH13	lpddr22_dq30	-	-	-	-	-	-	-
-	AJ14	lpddr22_dq31	-	-	-	-	-	-	-
-	R29	lpddr22_ca0	-	-	-	-	-	-	-
-	T29	lpddr22_ca1	-	-	-	-	-	-	-
-	U29	lpddr22_ca2	-	-	-	-	-	-	-
-	V29	lpddr22_ca3	-	-	-	-	-	-	-
-	W28	lpddr22_ca4	-	-	-	-	-	-	-
-	AC29	lpddr22_ca5	-	-	-	-	-	-	-
-	AD29	lpddr22_ca6	-	-	-	-	-	-	-
-	AD28	lpddr22_ca7	-	-	-	-	-	-	-
-	AE28	lpddr22_ca8	-	-	-	-	-	-	-
-	AF29	lpddr22_ca9	-	-	-	-	-	-	-
-	AA1	lpddr22_dqs0	-	-	-	-	-	-	-
-	AA2	lpddr22_ndqs0	-	-	-	-	-	-	-
-	AD2	lpddr22_dqs1	-	-	-	-	-	-	-
-	AD1	lpddr22_ndqs1	-	-	-	-	-	-	-
-	K2	lpddr22_dqs2	-	-	-	-	-	-	-
-	K1	lpddr22_ndqs2	-	-	-	-	-	-	-
-	AH8	lpddr22_dqs3	-	-	-	-	-	-	-
-	AJ8	lpddr22_ndqs3	-	-	-	-	-	-	-
-	AB1	lpddr22_dm0	-	-	-	-	-	-	-
-	AC2	lpddr22_dm1	-	-	-	-	-	-	-
-	L1	lpddr22_dm2	-	-	-	-	-	-	-
-	AH7	lpddr22_dm3	-	-	-	-	-	-	-
-	AB28	lpddr22_ck	-	-	-	-	-	-	-
-	AB29	lpddr22_nck	-	-	-	-	-	-	-
-	Y28	lpddr22_ncs0	-	-	-	-	-	-	-
-	W29	lpddr22_ncs1	-	-	-	-	-	-	-
-	AA29	lpddr22_cke0	-	-	-	-	-	-	-
-	Y29	lpddr22_cke1	-	-	-	-	-	-	-
-	U28	lpddr22_vref_ca	-	-	-	-	-	-	-
-	R2	lpddr22_vref_dq	-	-	-	-	-	-	-
P3	-	dsi1_dx0	-	-	-	-	-	-	-
P4	-	dsi1_dy0	-	-	-	-	-	-	-

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Table 2-2. Multiplexing Characteristics[(1)] (continued)

BALL BOTTOM	BALL TOP	Mode 0	Mode 1	Mode 2	Mode 3	Mode 4	Mode 5	Mode 6	Mode 7
N3	-	dsi1_dx1	-	-	-	-	-	-	-
N4	-	dsi1_dy1	-	-	-	-	-	-	-
M3	-	dsi1_dx2	-	-	-	-	-	-	-
M4	-	dsi1_dy2	-	-	-	-	-	-	-
L3	-	dsi1_dx3	-	-	-	-	-	-	-
L4	-	dsi1_dy3	-	-	-	-	-	-	-
K3	-	dsi1_dx4	-	-	-	-	-	-	-
K4	-	dsi1_dy4	-	-	-	-	-	-	-
T3	-	dsi2_dx0	-	-	-	-	-	-	-
T4	-	dsi2_dy0	-	-	-	-	-	-	-
U3	-	dsi2_dx1	-	-	-	-	-	-	-
U4	-	dsi2_dy1	-	-	-	-	-	-	-
V3	-	dsi2_dx2	-	-	-	-	-	-	-
V4	-	dsi2_dy2	-	-	-	-	-	-	-
B7	-	cvideo_tvout	-	-	-	-	-	-	-
C7	-	cvideo_vfb	-	-	-	-	-	-	-
D7	-	cvideo_rset	-	-	-	-	-	-	-
B9	-	hdmi_hpd	-	-	gpio_63	-	-	-	safe_mode
B10	-	hdmi_cec	-	-	gpio_64	-	-	-	safe_mode
A8	-	hdmi_ddc_ scl	-	-	gpio_65	-	-	-	safe_mode
B8	-	hdmi_ddc_ sda	-	-	gpio_66	-	-	-	safe_mode
C8	-	hdmi_data2x	-	-	-	-	-	-	-
D8	-	hdmi_data2y	-	-	-	-	-	-	-
C9	-	hdmi_data1x	-	-	-	-	-	-	-
D9	-	hdmi_data1y	-	-	-	-	-	-	-
C10	-	hdmi_data0x	-	-	-	-	-	-	-
D10	-	hdmi_data0y	-	-	-	-	-	-	-
C11	-	hdmi_clockx	-	-	-	-	-	-	-
D11	-	hdmi_clocky	-	-	-	-	-	-	-
R26	-	csi21_dx0	-	-	gpi_67	-	-	-	safe_mode
R25	-	csi21_dy0	-	-	gpi_68	-	-	-	safe_mode
T26	-	csi21_dx1	-	-	gpi_69	-	-	-	safe_mode
T25	-	csi21_dy1	-	-	gpi_70	-	-	-	safe_mode
U26	-	csi21_dx2	-	-	gpi_71	-	-	-	safe_mode
U25	-	csi21_dy2	-	-	gpi_72	-	-	-	safe_mode
V26	-	csi21_dx3	-	-	gpi_73	-	-	-	safe_mode
V25	-	csi21_dy3	-	-	gpi_74	-	-	-	safe_mode
W26	-	csi21_dx4	-	-	gpi_75	-	-	-	safe_mode
W25	-	csi21_dy4	-	-	gpi_76	-	-	-	safe_mode
M26	-	csi22_dx0	-	-	gpi_77	-	-	-	safe_mode
M25	-	csi22_dy0	-	-	gpi_78	-	-	-	safe_mode
N26	-	csi22_dx1	-	-	gpi_79	-	-	-	safe_mode
N25	-	csi22_dy1	-	-	gpi_80	-	-	-	safe_mode
T27	-	cam_shutter	-	-	gpio_81	-	-	-	safe_mode
U27	-	cam_strobe	-	-	gpio_82	-	-	-	safe_mode

Table 2-2. Multiplexing Characteristics[(1)] (continued)

BALL BOTTOM	BALL TOP	Mode 0	Mode 1	Mode 2	Mode 3	Mode 4	Mode 5	Mode 6	Mode 7
V27	-	cam_ globalreset	-	-	gpio_83	-	-	-	safe_mode
AE18	-	usbb1_ulpitll _clk	hsi1_cawake	-	gpio_84	usbb1_ ulpiphy_clk	-	attila_hw_ dbg20	safe_mode
AG19	-	usbb1_ulpitll _stp	hsi1_cadata	mcbsp4_clkr	gpio_85	usbb1_ ulpiphy_stp	usbb1_mm_ rxdp	attila_hw_ dbg21	safe_mode
AF19	-	usbb1_ulpitll _dir	hsi1_caflag	mcbsp4_fsr	gpio_86	usbb1_ ulpiphy_dir	-	attila_hw_ dbg22	safe_mode
AE19	-	usbb1_ulpitll _nxt	hsi1_acready	mcbsp4_fsx	gpio_87	usbb1_ ulpiphy_nxt	usbb1_mm_ rxdm	attila_hw_ dbg23	safe_mode
AF18	-	usbb1_ulpitll _dat0	hsi1_acwake	mcbsp4_clkx	gpio_88	usbb1_ ulpiphy_dat0	usbb1_mm_ txen	attila_hw_ dbg24	safe_mode
AG18	-	usbb1_ulpitll _dat1	hsi1_acdata	mcbsp4_dx	gpio_89	usbb1_ ulpiphy_dat1	usbb1_mm_ txdat	attila_hw_ dbg25	safe_mode
AE17	-	usbb1_ulpitll _dat2	hsi1_acflag	mcbsp4_dr	gpio_90	usbb1_ ulpiphy_dat2	usbb1_mm_ txse0	attila_hw_ dbg26	safe_mode
AF17	-	usbb1_ulpitll _dat3	hsi1_caready	-	gpio_91	usbb1_ ulpiphy_dat3	usbb1_mm_ rxrcv	attila_hw_ dbg27	safe_mode
AH17	-	usbb1_ulpitll _dat4	dmtimer8_ pwm_evt	abe_mcbsp3 _dr	gpio_92	usbb1_ ulpiphy_dat4	-	attila_hw_ dbg28	safe_mode
AE16	-	usbb1_ulpitll _dat5	dmtimer9_ pwm_evt	abe_mcbsp3 _dx	gpio_93	usbb1_ ulpiphy_dat5	-	attila_hw_ dbg29	safe_mode
AF16	-	usbb1_ulpitll _dat6	dmtimer10_ pwm_evt	abe_mcbsp3 _clkx	gpio_94	usbb1_ ulpiphy_dat6	abe_dmic_ din3	attila_hw_ dbg30	safe_mode
AG16	-	usbb1_ulpitll _dat7	dmtimer11_ pwm_evt	abe_mcbsp3 _fsx	gpio_95	usbb1_ ulpiphy_dat7	abe_dmic_ clk3	attila_hw_ dbg31	safe_mode
AF14	-	usbb1_hsic_ data	-	-	gpio_96	-	-	-	safe_mode
AE14	-	usbb1_hsic_ strobe	-	-	gpio_97	-	-	-	safe_mode
H4	-	sim_io	-	-	gpio_wk0	-	-	attila_hw_ dbg1	safe_mode
J2	-	sim_clk	-	-	gpio_wk1	-	-	attila_hw_ dbg2	safe_mode
G2	-	sim_reset	-	-	gpio_wk2	-	-	attila_hw_ dbg3	safe_mode
J1	-	sim_cd	-	-	gpio_wk3	-	-	attila_hw_ dbg4	safe_mode
K1	-	sim_pwrctrl	-	-	gpio_wk4	-	-	attila_hw_ dbg5	safe_mode
H2	-	usbc1_icusb _dp	-	-	gpio_98	-	-	-	safe_mode
H3	-	usbc1_icusb _dm	-	-	gpio_99	-	-	-	safe_mode
D2	-	sdmmc1_clk	-	dpm_emu19	gpio_100	-	-	-	safe_mode
E3	-	sdmmc1_ cmd	-	uart1_rx	gpio_101	-	-	-	safe_mode
E4	-	sdmmc1_ dat0	-	dpm_emu18	gpio_102	-	-	-	safe_mode
E2	-	sdmmc1_ dat1	-	dpm_emu17	gpio_103	-	-	-	safe_mode
E1	-	sdmmc1_ dat2	-	dpm_emu16	gpio_104	jtag_tms_ tmsc	-	-	safe_mode
F4	-	sdmmc1_ dat3	-	dpm_emu15	gpio_105	jtag_tck	-	-	safe_mode

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Table 2-2. Multiplexing Characteristics[(1)] (continued)

BALL BOTTOM	BALL TOP	Mode 0	Mode 1	Mode 2	Mode 3	Mode 4	Mode 5	Mode 6	Mode 7
F3	-	sdmmc1_ dat4	-	-	gpio_106	-	-	-	safe_mode
F1	-	sdmmc1_ dat5	-	-	gpio_107	-	-	-	safe_mode
G4	-	sdmmc1_ dat6	-	-	gpio_108	-	-	-	safe_mode
G3	-	sdmmc1_ dat7	-	-	gpio_109	-	-	-	safe_mode
AD27	-	abe_mcbsp2 _clkx	mcspi2_clk	abe_mcasp_ ahclkx	gpio_110	usbb2_mm_ rxdm	-	-	safe_mode
AD26	-	abe_mcbsp2 _dr	mcspi2_somi	abe_mcasp_ axr	gpio_111	usbb2_mm_ rxdp	-	-	safe_mode
AD25	-	abe_mcbsp2 _dx	mcspi2_simo	abe_mcasp_ amute	gpio_112	usbb2_mm_ rxrcv	-	-	safe_mode
AC28	-	abe_mcbsp2 _fsx	mcspi2_cs0	abe_mcasp_ afsx	gpio_113	usbb2_mm_ txen	-	-	safe_mode
AC26	-	abe_mcbsp1 _clkx	abe_slimbus 1_clock	-	gpio_114	-	-	-	safe_mode
AC25	-	abe_mcbsp1 _dr	abe_slimbus 1_data	-	gpio_115	-	-	-	safe_mode
AB25	-	abe_mcbsp1 _dx	sdmmc3_ dat2	abe_mcasp_ aclkx	gpio_116	-	-	-	safe_mode
AC27	-	abe_mcbsp1 _fsx	sdmmc3_ dat3	abe_mcasp_ amutein	gpio_117	-	-	-	safe_mode
AG25	-	abe_pdm_ul _data	abe_mcbsp3 _dr	-	-	-	-	-	safe_mode
AF25	-	abe_pdm_dl _data	abe_mcbsp3 _dx	-	-	-	-	-	safe_mode
AE25	-	abe_pdm_ frame	abe_mcbsp3 _clkx	-	-	-	-	-	safe_mode
AF26	-	abe_pdm_lb _clk	abe_mcbsp3 _fsx	-	-	-	-	-	safe_mode
AH26	-	abe_clks	-	-	gpio_118	-	-	-	safe_mode
AE24	-	abe_dmic_ clk1	-	-	gpio_119	usbb2_mm_ txse0	uart4_cts	-	safe_mode
AF24	-	abe_dmic_ din1	-	-	gpio_120	usbb2_mm_ txdat	uart4_rts	-	safe_mode
AG24	-	abe_dmic_ din2	slimbus2_ clock	abe_mcasp_ axr	gpio_121	-	dmtimer11_ pwm_evt	-	safe_mode
AH24	-	abe_dmic_ din3	slimbus2_ data	abe_dmic_ clk2	gpio_122	-	dmtimer9_ pwm_evt	-	safe_mode
AB26	-	uart2_cts	sdmmc3_clk	-	gpio_123	-	-	-	safe_mode
AB27	-	uart2_rts	sdmmc3_ cmd	-	gpio_124	-	-	-	safe_mode
AA25	-	uart2_rx	sdmmc3_ dat0	-	gpio_125	-	-	-	safe_mode
AA26	-	uart2_tx	sdmmc3_ dat1	-	gpio_126	-	-	-	safe_mode
AA27	-	hdq_sio	i2c3_sccb	i2c2_sccb	gpio_127	-	-	-	safe_mode
AE28	-	i2c1_scl	-	-	-	-	-	-	-
AE26	-	i2c1_sda	-	-	-	-	-	-	-
C26	-	i2c2_scl	uart1_rx	-	gpio_128	-	-	-	safe_mode
D26	-	i2c2_sda	uart1_tx	-	gpio_129	-	-	-	safe_mode
W27	-	i2c3_scl	-	-	gpio_130	-	-	-	safe_mode

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Table 2-2. Multiplexing Characteristics(1) (continued)

BALL BOTTOM	BALL TOP	Mode 0	Mode 1	Mode 2	Mode 3	Mode 4	Mode 5	Mode 6	Mode 7
Y27	-	i2c3_sda	-	-	gpio_131	-	-	-	safe_mode
AG21	-	i2c4_scl	-	-	gpio_132	-	-	-	safe_mode
AH22	-	i2c4_sda	-	-	gpio_133	-	-	-	safe_mode
AG9	-	sr_scl	-	-	-	-	-	-	-
AF9	-	sr_sda	-	-	-	-	-	-	-
AF22	-	mcspi1_clk	-	-	gpio_134	-	-	-	safe_mode
AE22	-	mcspi1_somi	-	-	gpio_135	-	-	-	safe_mode
AG22	-	mcspi1_simo	-	-	gpio_136	-	-	-	safe_mode
AE23	-	mcspi1_cs0	-	-	gpio_137	-	-	-	safe_mode
AF23	-	mcspi1_cs1	uart1_rx	-	gpio_138	-	-	-	safe_mode
AG23	-	mcspi1_cs2	uart1_cts	slimbus2_clock	gpio_139	-	-	-	safe_mode
AH23	-	mcspi1_cs3	uart1_rts	slimbus2_data	gpio_140	-	-	-	safe_mode
F27	-	uart3_cts_rctx	uart1_tx	-	gpio_141	-	-	-	safe_mode
F28	-	uart3_rts_sd	-	-	gpio_142	-	-	-	safe_mode
G27	-	uart3_rx_irrx	dmtimer8_pwm_evt	-	gpio_143	-	-	-	safe_mode
G28	-	uart3_tx_irtx	dmtimer9_pwm_evt	-	gpio_144	-	-	-	safe_mode
AE5	-	sdmmc5_clk	mcspi2_clk	usbc1_icusb_dp	gpio_145	-	sdmmc2_clk	-	safe_mode
AF5	-	sdmmc5_cmd	mcspi2_simo	usbc1_icusb_dm	gpio_146	-	sdmmc2_cmd	-	safe_mode
AE4	-	sdmmc5_dat0	mcspi2_somi	usbc1_icusb_rcv	gpio_147	-	sdmmc2_dat0	-	safe_mode
AF4	-	sdmmc5_dat1	-	usbc1_icusb_txen	gpio_148	-	sdmmc2_dat1	-	safe_mode
AG3	-	sdmmc5_dat2	mcspi2_cs1	-	gpio_149	-	sdmmc2_dat2	-	safe_mode
AF3	-	sdmmc5_dat3	mcspi2_cs0	-	gpio_150	-	sdmmc2_dat3	-	safe_mode
AE21	-	mcspi4_clk	sdmmc4_clk	kpd_col6	gpio_151	-	-	-	safe_mode
AF20	-	mcspi4_simo	sdmmc4_cmd	kpd_col7	gpio_152	-	-	-	safe_mode
AF21	-	mcspi4_somi	sdmmc4_dat0	kpd_row6	gpio_153	-	-	-	safe_mode
AE20	-	mcspi4_cs0	sdmmc4_dat3	kpd_row7	gpio_154	-	-	-	safe_mode
AG20	-	uart4_rx	sdmmc4_dat2	kpd_row8	gpio_155	-	-	-	safe_mode
AH19	-	uart4_tx	sdmmc4_dat1	kpd_col8	gpio_156	-	-	-	safe_mode
AG12	-	usbb2_ulpitll_clk	usbb2_ulpiphy_clk	sdmmc4_cmd	gpio_157	hsi2_cawake	-	-	safe_mode
AF12	-	usbb2_ulpitll_stp	usbb2_ulpiphy_stp	sdmmc4_clk	gpio_158	hsi2_cadata	dispc2_data23	-	safe_mode
AE12	-	usbb2_ulpitll_dir	usbb2_ulpiphy_dir	sdmmc4_dat0	gpio_159	hsi2_caflag	dispc2_data22	-	safe_mode
AG13	-	usbb2_ulpitll_nxt	usbb2_ulpiphy_nxt	sdmmc4_dat1	gpio_160	hsi2_acready	dispc2_data21	-	safe_mode

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Table 2-2. Multiplexing Characteristics(1) (continued)

BALL BOTTOM	BALL TOP	Mode 0	Mode 1	Mode 2	Mode 3	Mode 4	Mode 5	Mode 6	Mode 7
AE11	-	usbb2_ulpitll_dat0	usbb2_ulpiphy_dat0	sdmmc4_dat2	gpio_161	hsi2_acwake	dispc2_data20	usbb2_mm_txen	safe_mode
AF11	-	usbb2_ulpitll_dat1	usbb2_ulpiphy_dat1	sdmmc4_dat3	gpio_162	hsi2_acdata	dispc2_data19	usbb2_mm_txdat	safe_mode
AG11	-	usbb2_ulpitll_dat2	usbb2_ulpiphy_dat2	sdmmc3_dat2	gpio_163	hsi2_acflag	dispc2_data18	usbb2_mm_txse0	safe_mode
AH11	-	usbb2_ulpitll_dat3	usbb2_ulpiphy_dat3	sdmmc3_dat1	gpio_164	hsi2_caready	dispc2_data15	rfbi_data15	safe_mode
AE10	-	usbb2_ulpitll_dat4	usbb2_ulpiphy_dat4	sdmmc3_dat0	gpio_165	mcspi3_somi	dispc2_data14	rfbi_data14	safe_mode
AF10	-	usbb2_ulpitll_dat5	usbb2_ulpiphy_dat5	sdmmc3_dat3	gpio_166	mcspi3_cs0	dispc2_data13	rfbi_data13	safe_mode
AG10	-	usbb2_ulpitll_dat6	usbb2_ulpiphy_dat6	sdmmc3_cmd	gpio_167	mcspi3_simo	dispc2_data12	rfbi_data12	safe_mode
AE9	-	usbb2_ulpitll_dat7	usbb2_ulpiphy_dat7	sdmmc3_clk	gpio_168	mcspi3_clk	dispc2_data11	rfbi_data11	safe_mode
AF13	-	usbb2_hsic_data	-	-	gpio_169	-	-	-	safe_mode
AE13	-	usbb2_hsic_strobe	-	-	gpio_170	-	-	-	safe_mode
G26	-	kpd_col3	kpd_col0	-	gpio_171	-	-	-	safe_mode
G25	-	kpd_col4	kpd_col1	-	gpio_172	-	-	-	safe_mode
H26	-	kpd_col5	kpd_col2	-	gpio_173	-	-	-	safe_mode
H25	-	kpd_col0	kpd_col3	-	gpio_174	-	-	-	safe_mode
J27	-	kpd_col1	kpd_col4	-	gpio_0	-	-	-	safe_mode
H27	-	kpd_col2	kpd_col5	-	gpio_1	-	-	-	safe_mode
J26	-	kpd_row3	kpd_row0	-	gpio_175	-	-	-	safe_mode
J25	-	kpd_row4	kpd_row1	-	gpio_176	-	-	-	safe_mode
K26	-	kpd_row5	kpd_row2	-	gpio_177	-	-	-	safe_mode
K25	-	kpd_row0	kpd_row3	-	gpio_178	-	-	-	safe_mode
L27	-	kpd_row1	kpd_row4	-	gpio_2	-	-	-	safe_mode
K27	-	kpd_row2	kpd_row5	-	gpio_3	-	-	-	safe_mode
C3	-	usba0_otg_ce	-	-	-	-	-	-	-
B5	-	usba0_otg_dp	uart3_rx_irrx	uart2_rx	-	-	-	-	safe_mode
B4	-	usba0_otg_dm	uart3_tx_irtx	uart2_tx	-	-	-	-	safe_mode
AH6	-	fref_xtal_in	-	-	-	-	-	-	-
AH5	-	fref_xtal_out	-	-	-	-	-	-	-
AG5	-	fref_xtal_vssosc	-	-	-	-	-	-	-
AG8	-	fref_slicer_in	-	-	gpi_wk5	-	-	-	safe_mode
AD1	-	fref_clk_ioreq	-	-	-	-	-	-	-
AD2	-	fref_clk0_out	fref_clk1_req	sys_drm_msecure	gpio_wk6	-	sdmmc2_dat7	attila_hw_dbg6	safe_mode
AA28	-	fref_clk1_out	-	-	gpio_181	-	-	-	safe_mode
Y28	-	fref_clk2_out	-	-	gpio_182	-	-	-	safe_mode
AD3	-	fref_clk3_req	fref_clk1_req	sys_drm_msecure	gpio_wk30	-	sdmmc2_dat4	attila_hw_dbg7	safe_mode

Table 2-2. Multiplexing Characteristics(1) (continued)

BALL BOTTOM	BALL TOP	Mode 0	Mode 1	Mode 2	Mode 3	Mode 4	Mode 5	Mode 6	Mode 7
AD4	-	fref_clk3_out	fref_clk2_req	sys_secure_ indicator	gpio_ wk31	-	sdmmc2_ dat5	attila_hw_ dbg8	safe_mode
AC2	-	fref_clk4_req	fref_clk5_out	-	gpio_wk7	-	sdmmc2_ dat6	attila_hw_ dbg9	-
AC3	-	fref_clk4_out	-	-	gpio_wk8	-	-	attila_hw_ dbg10	-
AG7	-	sys_32k	-	-	-	-	-	-	-
AE7	-	sys_ nrespwron	-	-	-	-	-	-	-
AF7	-	sys_ nreswarm	-	-	-	-	-	-	-
AH7	-	sys_pwr_req	-	-	-	-	-	-	-
AG6	-	sys_pwron_ reset_out	-	-	gpio_ wk29	-	-	attila_hw_ dbg11	-
AE6	-	sys_nirq1	-	-	-	-	-	-	safe_mode
AF6	-	sys_nirq2	-	-	gpio_183	-	-	-	safe_mode
F26	-	sys_boot0	-	-	gpio_184	-	-	-	safe_mode
E27	-	sys_boot1	-	-	gpio_185	-	-	-	safe_mode
E26	-	sys_boot2	-	-	gpio_186	-	-	-	safe_mode
E25	-	sys_boot3	-	-	gpio_187	-	-	-	safe_mode
D28	-	sys_boot4	-	-	gpio_188	-	-	-	safe_mode
D27	-	sys_boot5	-	-	gpio_189	-	-	-	safe_mode
AF8	-	sys_boot6	dpm_emu18	-	gpio_wk9	-	-	attila_hw_ dbg12	safe_mode
AE8	-	sys_boot7	dpm_emu19	-	gpio_ wk10	-	-	attila_hw_ dbg13	safe_mode
AH2	-	jtag_ntrst	-	-	-	-	-	-	-
AG1	-	jtag_tck	-	-	-	-	-	-	safe_mode
AE3	-	jtag_rtck	-	-	-	-	-	-	-
AH1	-	jtag_tms_ tmsc	-	-	-	-	-	-	safe_mode
AE1	-	jtag_tdi	-	-	-	-	-	-	-
AE2	-	jtag_tdo	-	-	-	-	-	-	-
M2	-	dpm_emu0	-	-	gpio_11	-	-	attila_hw_ dbg0	safe_mode
N2	-	dpm_emu1	-	-	gpio_12	-	-	attila_hw_ dbg1	safe_mode
P2	-	dpm_emu2	usba0_ ulpiphy_clk	-	gpio_13	-	dispc2_fid	attila_hw_ dbg2	safe_mode
V1	-	dpm_emu3	usba0_ ulpiphy_stp	-	gpio_14	rfbi_data10	dispc2_ data10	attila_hw_ dbg3	safe_mode
V2	-	dpm_emu4	usba0_ ulpiphy_dir	-	gpio_15	rfbi_data9	dispc2_data9	attila_hw_ dbg4	safe_mode
W1	-	dpm_emu5	usba0_ ulpiphy_nxt	-	gpio_16	rfbi_te_ vsync0	dispc2_ data16	attila_hw_ dbg5	safe_mode
W2	-	dpm_emu6	usba0_ ulpiphy_dat0	uart3_tx_irtx	gpio_17	rfbi_hsync0	dispc2_ data17	attila_hw_ dbg6	safe_mode
W3	-	dpm_emu7	usba0_ ulpiphy_dat1	uart3_rx_irrx	gpio_18	rfbi_cs0	dispc2_ hsync	attila_hw_ dbg7	safe_mode
W4	-	dpm_emu8	usba0_ ulpiphy_dat2	uart3_rts_sd	gpio_19	rfbi_re	dispc2_pclk	attila_hw_ dbg8	safe_mode
Y2	-	dpm_emu9	usba0_ ulpiphy_dat3	uart3_cts_ rctx	gpio_20	rfbi_we	dispc2_ vsync	attila_hw_ dbg9	safe_mode

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Table 2-2. Multiplexing Characteristics[(1)] (continued)

BALL BOTTOM	BALL TOP	Mode 0	Mode 1	Mode 2	Mode 3	Mode 4	Mode 5	Mode 6	Mode 7
Y3	-	dpm_emu10	usba0_ ulpiphy_dat4	-	gpio_21	rfbi_a0	dispc2_de	attila_hw_ dbg10	safe_mode
Y4	-	dpm_emu11	usba0_ ulpiphy_dat5	-	gpio_22	rfbi_data8	dispc2_data8	attila_hw_ dbg11	safe_mode
AA1	-	dpm_emu12	usba0_ ulpiphy_dat6	-	gpio_23	rfbi_data7	dispc2_data7	attila_hw_ dbg12	safe_mode
AA2	-	dpm_emu13	usba0_ ulpiphy_dat7	-	gpio_24	rfbi_data6	dispc2_data6	attila_hw_ dbg13	safe_mode
AA3	-	dpm_emu14	sys_drm_ msecure	uart1_rx	gpio_25	rfbi_data5	dispc2_data5	attila_hw_ dbg14	safe_mode
AA4	-	dpm_emu15	sys_secure_ indicator	-	gpio_26	rfbi_data4	dispc2_data4	attila_hw_ dbg15	safe_mode
AB2	-	dpm_emu16	dmtimer8_ pwm_evt	dsi1_te0	gpio_27	rfbi_data3	dispc2_data3	attila_hw_ dbg16	safe_mode
AB3	-	dpm_emu17	dmtimer9_ pwm_evt	dsi1_te1	gpio_28	rfbi_data2	dispc2_data2	attila_hw_ dbg17	safe_mode
AB4	-	dpm_emu18	dmtimer10_ pwm_evt	dsi2_te0	gpio_190	rfbi_data1	dispc2_data1	attila_hw_ dbg18	safe_mode
AC4	-	dpm_emu19	dmtimer11_ pwm_evt	dsi2_te1	gpio_191	rfbi_data0	dispc2_data0	attila_hw_ dbg19	safe_mode

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Table 2-2. Multiplexing Characteristics(1) (continued)

BALL BOTTOM	BALL TOP	Mode 0	Mode 1	Mode 2	Mode 3	Mode 4	Mode 5	Mode 6	Mode 7
H1 / M1 / AB1 / C2 / F2 / K2 / U2 / AF2 / B3 / J3 / J4 / AG4 / B6 / K8 / U8 / AH8 / N9 / A10 / AH10 / H11 / AA11 / N12 / P12 / R12 / T12 / U12 / AA12 / B13 / H13 / M13 / N13 / P13 / R13 / T13 / U13 / AH13 / M14 / N14 / P14 / R14 / T14 / U14 / M15 / N15 / P15 / R15 / T15 / U15 / M16 / N16 / P16 / R16 / T16 / U16 / H17 / M17 / N17 / P17 / R17 / T17 / U17 / Y17 / AG17 / H19 / A20 / AA20 / J21 / L21 / M21 / U21 / AH21 / M22 / A23 / F25 / L25 / Y25 / L26 / Y26 / AG26 / B27 / AE27 / H28 / K28 / U28	A2 / A6 / A9 / A11 / A14 / A28 / B1 / B14 / B21 / B24 / B29 / E28 / F1 / H28 / J1 / L29 / M2 / P1 / P2 / R28 / V2 / V28 / AA28 / AB2 / AE2 / AF28 / AH1 / AH5 / AH14 / AH18 / AH29 / AJ2 / AJ7 / AJ11 / AJ16 / AJ22 / AJ28	vss	-	-	-	-	-	-	-
Y22	-	vpp(2)	-	-	-	-	-	-	-
J8	-	vpp_cust(2)	-	-	-	-	-	-	-
J9 / K9 / L9 / M9 / T9 / J10 / J11 / Y11 / H12 / J12 / Y12 / J13 / Y13 / AA13 / J15 / J16 / J17 / H18 / J18 / J19 / J20 / K20 / L20 / M20 / N20 / R20 / T20 / U20 / V20	-	vdd_core	-	-	-	-	-	-	-
V8 / W8 / Y8 / U9 / V9 / W9 / Y9 / Y10 / AA10	-	vdd_mpu	-	-	-	-	-	-	-

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Table 2-2. Multiplexing Characteristics(1) (continued)

BALL BOTTOM	BALL TOP	Mode 0	Mode 1	Mode 2	Mode 3	Mode 4	Mode 5	Mode 6	Mode 7
AA17 / Y18 / AA18 / Y19 / AA19 / W20 / Y20 / V21 / W21 / Y21	-	vdd_iva_audio	-	-	-	-	-	-	-
AA16	-	vdds_1p2v	-	-	-	-	-	-	-
AB7 / U7 / V7 / K7 / H22 / J22 / W22	-	vdds_1p8v	-	-	-	-	-	-	-
Y7	-	vdds_1p8_fref	-	-	-	-	-	-	-
D1 / G1 / U1 / Y1 / AC1 / AF1 / A4 / AH4 / A6 / L7 / G8 / H8 / L8 / M8 / AA8 / A9 / H9 / AA9 / AB9 / AH9 / A12 / AH12 / A17 / H20 / G21 / H21 / A22 / A25 / E28 / J28 / L28	A22 / B4 / B7 / B9 / B13 / B18 / B25 / D2 / D29 / F29 / G2 / J2 / J28 / M28 / U1 / Y1 / AC1 / AF2 / AH9 / AH12 / AJ4 / AJ6	vddq_lpddr2	-	-	-	-	-	-	-
G15	-	vddq_vref_lpddr21	-	-	-	-	-	-	-
T8	-	vddq_vref_lpddr22	-	-	-	-	-	-	-
AH18 / AH20 / AA21 / AB21 / AA22 / AB22 / AH25 / T28 / AB28 / AD28	T28 / AC28 / AE29 / AH22 / AJ19 / AJ26	vddca_lpddr2	-	-	-	-	-	-	-
Y14	-	vddca_vref_lpddr21	-	-	-	-	-	-	-
R27	-	vddca_vref_lpddr22	-	-	-	-	-	-	-
G22	-	vdda_dll0_lpddr21	-	-	-	-	-	-	-
G9	-	vdda_dll1_lpddr21	-	-	-	-	-	-	-
M7	-	vdda_dll0_lpddr22	-	-	-	-	-	-	-
AB10	-	vdda_dll1_lpddr22	-	-	-	-	-	-	-
L1	-	vdda_dsi1	-	-	-	-	-	-	-
N8 / P8	-	vssa_dsi	-	-	-	-	-	-	-
L2	-	vdda_dsi2	-	-	-	-	-	-	-
W28	-	vdda_csi21	-	-	-	-	-	-	-
R22	-	vssa_csi2	-	-	-	-	-	-	-

Table 2-2. Multiplexing Characteristics[(1)] (continued)

BALL BOTTOM	BALL TOP	Mode 0	Mode 1	Mode 2	Mode 3	Mode 4	Mode 5	Mode 6	Mode 7
V28	-	vdda_csi22	-	-	-	-	-	-	-
A11 / G12	-	vdda_hdmi_vdac	-	-	-	-	-	-	-
G11	-	vssa_hdmi_vdac	-	-	-	-	-	-	-
A5	-	vdda_usba0otg_3p3v	-	-	-	-	-	-	-
G10	-	vssa_usba0otg_3p3v	-	-	-	-	-	-	-
A7	-	vdda_usba0otg_1p8v	-	-	-	-	-	-	-
H10	-	vssa_usba0otg	-	-	-	-	-	-	-
J7	-	vdds_usim	-	-	-	-	-	-	-
A2	-	pbias_sim	-	-	-	-	-	-	-
G7 / H7	-	vdds_sdmmc1	-	-	-	-	-	-	-
A1	-	pbias_mmc1	-	-	-	-	-	-	-
P9	-	vdda_dpll_mpu	-	-	-	-	-	-	-
G13	-	vdda_dpll_core_audio	-	-	-	-	-	-	-
Y16	-	vdda_dpll_iva_per	-	-	-	-	-	-	-
G20	-	vdds_dv_gpmc	-	-	-	-	-	-	-
G16 / H16	-	vdds_dv_sdmmc2	-	-	-	-	-	-	-
G17 / G18 / G19	-	vdds_dv_c2c	-	-	-	-	-	-	-
V22	-	vdds_dv_cam	-	-	-	-	-	-	-
AB16	-	vdds_dv_bank0	-	-	-	-	-	-	-
AB20	-	vdds_dv_bank1	-	-	-	-	-	-	-
AB8 / AB19	-	vdds_dv_bank2	-	-	-	-	-	-	-
AB18	-	vdds_dv_bank3	-	-	-	-	-	-	-
AA7	-	vdds_dv_bank4	-	-	-	-	-	-	-
AB17	-	vdds_dv_bank5	-	-	-	-	-	-	-
AA14	-	vdds_dv_bank6	-	-	-	-	-	-	-
M28	-	vdds_dv_bank7	-	-	-	-	-	-	-
W7	-	vdds_dv_fref	-	-	-	-	-	-	-
AB14	-	vdda_ldo_sram_mpu	-	-	-	-	-	-	-

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Table 2-2. Multiplexing Characteristics(1) (continued)

BALL BOTTOM	BALL TOP	Mode 0	Mode 1	Mode 2	Mode 3	Mode 4	Mode 5	Mode 6	Mode 7
N22	-	vdda_ldo_sram_iva_audio	-	-	-	-	-	-	-
T22	-	vdda_ldo_sram_core	-	-	-	-	-	-	-
P7	-	vdda_ldo_emu_wkup	-	-	-	-	-	-	-
AB12	-	vdda_bdgp_vbb	-	-	-	-	-	-	-
AB13	-	cap_vbb_ldo_mpu	-	-	-	-	-	-	-
R21	-	cap_vbb_ldo_iva_audio	-	-	-	-	-	-	-
AB11	-	cap_vdd_ldo_sram_mpu	-	-	-	-	-	-	-
N21	-	cap_vdd_ldo_sram_iva_audio	-	-	-	-	-	-	-
U22	-	cap_vdd_ldo_sram_core	-	-	-	-	-	-	-
T7	-	cap_vdd_ldo_emu_wkup	-	-	-	-	-	-	-
A27	-	atestv(3)	-	-	-	-	-	-	-
AG28	-	vsense(3)	-	-	-	-	-	-	-
AH27	-	iforce(3)	-	-	-	-	-	-	-
AH16	AJ17	pop_lpddr21_zq	-	-	-	-	-	-	-
AF28	AG29	pop_lpddr22_zq	-	-	-	-	-	-	-
A26 / B2	B2 / B28	pop_vacc_lpddr2	-	-	-	-	-	-	-
AG27 / C1 / AG2	C1 / AH2 / AH28	pop_vdd1_lpddr2_shared	-	-	-	-	-	-	-
A13 / C27 / AH14	A15 / C28 / AJ15	pop_vdd1_lpddr21	-	-	-	-	-	-	-
N1 / P1 / R28	N2 / P29 / R1	pop_vdd1_lpddr22	-	-	-	-	-	-	-
AH3 / A3 / C28 / AF27	A3 / C29 / AG28 / AH3	pop_vdd2_lpddr2_shared	-	-	-	-	-	-	-
AG14 / A15 / B15	A16 / B16 / AH15	pop_vdd2_lpddr21	-	-	-	-	-	-	-
N28 / T1 / T2	P28 / T1 / T2	pop_vdd2_lpddr22	-	-	-	-	-	-	-

(1) In safe_mode the ball is configured as a high impedance input; the ball is also floating (unconnected to modules).

(2) vpp must be unconnected. vpp_cust is only powered when programming CPFROM eFuses. Otherwise, it is recommended to leave vpp_cust turned off (floating). Note that if the TWL6030 PMIC is used then the vpp pulldown resistor inside the TWL6030 must be disabled when the vpp_cust is turned off.

(3) atestv, iforce, and vsense pins must be left unconnected.
The following bottom balls are reserved: C4 / C5 / C6 / D3 / D4 / D5 / D6 / L22 / N7. These balls must be left unconnected.

2.4 Signal Descriptions

Many signals are available on multiple pins, according to the software configuration of the pin multiplexing options.

1. **SIGNAL NAME:** The name of the signal passing through the pin.

NOTE

The subsystem multiplexing signals are not described in Table 2-1 and Table 2-2.

2. **DESCRIPTION:** Description of the signal
3. **TYPE:** Type = Signal direction and type:
   – I = Input
   – O = Output
   – IO = Input / output
   – D = Open Drain
   – DS = Differential
   – A = Analog
   – PWR = Power
   – GND = Ground
4. **BALL BOTTOM:** Associated ball(s) bottom
5. **BALL TOP:** Associated ball(s) top
6. **PIN NAME:** This is the name of the pin the signal is passing through.

2.4.1 External Memory Interfaces

2.4.1.1 GPMC

NOTE

For more information, see the Memory Subsystem / General-Purpose Memory Controller section of the OMAP4430 TRM.

Table 2-3. GPMC Signal Descriptions

SIGNAL NAME [1]	PIN NAME [6]	DESCRIPTION [2]	TYPE [3]	BALL BOTTOM [4]	BALL TOP [5]
Multiplexed GPMC Mode					
gpmc_a1/gpmc_d0	gpmc_ad0	GPMC address bit 1 / data bit 0	IO	C12	-
gpmc_a2/gpmc_d1	gpmc_ad1	GPMC address bit 2 / data bit 1	IO	D12	-
gpmc_a3/gpmc_d2	gpmc_ad2	GPMC address bit 3 / data bit 2	IO	C13	-
gpmc_a4/gpmc_d3	gpmc_ad3	GPMC address bit 4 / data bit 3	IO	D13	-
gpmc_a5/gpmc_d4	gpmc_ad4	GPMC address bit 5 / data bit 4	IO	C15	-
gpmc_a6/gpmc_d5	gpmc_ad5	GPMC address bit 6 / data bit 5	IO	D15	-
gpmc_a7/gpmc_d6	gpmc_ad6	GPMC address bit 7 / data bit 6	IO	A16	-
gpmc_a8/gpmc_d7	gpmc_ad7	GPMC address bit 8 / data bit 7	IO	B16	-
gpmc_a9/gpmc_d8	gpmc_ad8	GPMC address bit 9 / data bit 8	IO	C16	-
gpmc_a10/gpmc_d9	gpmc_ad9	GPMC address bit 10 / data bit 9	IO	D16	-
gpmc_a11/gpmc_d10	gpmc_ad10	GPMC address bit 11 / data bit 10	IO	C17	-
gpmc_a12/gpmc_d11	gpmc_ad11	GPMC address bit 12 / data bit 11	IO	D17	-
gpmc_a13/gpmc_d12	gpmc_ad12	GPMC address bit 13 / data bit 12	IO	C18	-
gpmc_a14/gpmc_d13	gpmc_ad13	GPMC address bit 14 / data bit 13	IO	D18	-
gpmc_a15/gpmc_d14	gpmc_ad14	GPMC address bit 15 / data bit 14	IO	C19	-

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Table 2-3. GPMC Signal Descriptions (continued)

SIGNAL NAME [1]	PIN NAME [6]	DESCRIPTION [2]	TYPE [3]	BALL BOTTOM [4]	BALL TOP [5]
gpmc_a16/gpmc_d15	gpmc_ad15	GPMC address bit 16 / data bit 15	IO	D19	-
gpmc_a17	gpmc_a16	GPMC address bit 17	O	B17	-
gpmc_a18	gpmc_a17	GPMC address bit 18	O	A18	-
gpmc_a19	gpmc_a18	GPMC address bit 19	O	B18	-
gpmc_a20	gpmc_a19	GPMC address bit 20	O	A19	-
gpmc_a21	gpmc_a20	GPMC address bit 21	O	B19	-
gpmc_a22	gpmc_a21	GPMC address bit 22	O	B20	-
gpmc_a23	gpmc_a22	GPMC address bit 23	O	A21	-
gpmc_a24	gpmc_a23	GPMC address bit 24	O	B21	-
gpmc_a25	gpmc_a24	GPMC address bit 25	O	C20	-
gpmc_a26	gpmc_a25	GPMC address bit 26	O	D20	-
Nonmultiplexed GPMC Mode					
gpmc_d0	gpmc_ad0	GPMC data bit 0	IO	C12	-
gpmc_d1	gpmc_ad1	GPMC data bit 1	IO	D12	-
gpmc_d2	gpmc_ad2	GPMC data bit 2	IO	C13	-
gpmc_d3	gpmc_ad3	GPMC data bit 3	IO	D13	-
gpmc_d4	gpmc_ad4	GPMC data bit 4	IO	C15	-
gpmc_d5	gpmc_ad5	GPMC data bit 5	IO	D15	-
gpmc_d6	gpmc_ad6	GPMC data bit 6	IO	A16	-
gpmc_d7	gpmc_ad7	GPMC data bit 7	IO	B16	-
gpmc_d8	gpmc_ad8	GPMC data bit 8	IO	C16	-
gpmc_d9	gpmc_ad9	GPMC data bit 9	IO	D16	-
gpmc_d10	gpmc_ad10	GPMC data bit 10	IO	C17	-
gpmc_d11	gpmc_ad11	GPMC data bit 11	IO	D17	-
gpmc_d12	gpmc_ad12	GPMC data bit 12	IO	C18	-
gpmc_d13	gpmc_ad13	GPMC data bit 13	IO	D18	-
gpmc_d14	gpmc_ad14	GPMC data bit 14	IO	C19	-
gpmc_d15	gpmc_ad15	GPMC data bit 15	IO	D19	-
gpmc_a1	gpmc_a16	GPMC address bit 1	O	B17	-
gpmc_a2	gpmc_a17	GPMC address bit 2	O	A18	-
gpmc_a3	gpmc_a18	GPMC address bit 3	O	B18	-
gpmc_a4	gpmc_a19	GPMC address bit 4	O	A19	-
gpmc_a5	gpmc_a20	GPMC address bit 5	O	B19	-
gpmc_a6	gpmc_a21	GPMC address bit 6	O	B20	-
gpmc_a7	gpmc_a22	GPMC address bit 7	O	A21	-
gpmc_a8	gpmc_a23	GPMC address bit 8	O	B21	-
gpmc_a9	gpmc_a24	GPMC address bit 9	O	C20	-
gpmc_a10	gpmc_a25	GPMC address bit 10	O	D20	-
Common GPMC Signals					
gpmc_ncs0	gpmc_ncs0	GPMC chip select 0 invert	O	B25	-
gpmc_ncs1	gpmc_ncs1	GPMC chip select 1 invert	O	C21	-
gpmc_ncs2	gpmc_ncs2	GPMC chip select 2 invert	O	D21	-
gpmc_ncs3	gpmc_ncs3	GPMC chip select 3 invert	O	C22	-
gpmc_ncs4	gpmc_ncs4	GPMC chip select 4 invert	O	A24	-
gpmc_ncs5	gpmc_ncs5	GPMC chip select 5 invert	O	B24	-
gpmc_ncs6	gpmc_ncs6	GPMC chip select 6 invert	O	C24	-
gpmc_ncs7	gpmc_ncs7	GPMC chip select 7 invert	O	D24	-

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Table 2-3. GPMC Signal Descriptions (continued)

SIGNAL NAME [1]	PIN NAME [6]	DESCRIPTION [2]	TYPE [3]	BALL BOTTOM [4]	BALL TOP [5]
gpmc_nwp	gpmc_nwp	GPMC flash write protect invert	O	C25	-
gpmc_clk	gpmc_clk	GPMC clock	O	B22	-
gpmc_nadv_ale	gpmc_nadv_ale	GPMC address valid invert or address latch enable	O	D25	-
gpmc_noe	gpmc_noe	GPMC output enable invert	O	B11	-
gpmc_nwe	gpmc_nwe	GPMC write enable invert	O	B12	-
gpmc_nbe0_cle	gpmc_nbe0_cle	GPMC lower-byte enable invert(1)	O	C23	-
gpmc_nbe1	gpmc_nbe1	GPMC upper-byte enable invert	O	D22	-
gpmc_wait0	gpmc_wait0	GPMC external indication of wait 0	I	B26	-
gpmc_wait1	gpmc_wait1	GPMC external indication of wait 1	I	B23	-
gpmc_wait2	gpmc_wait2	GPMC external indication of wait 2	I	D23	-
gpmc_dir	gpmc_dir	GPMC ad[15:0] signal direction control	O	C22	-

(1) Also used as command latch enable for NAND protocol memories.

2.4.1.2 LPDDR2

NOTE

For more information, see the Memory Subsystem / EMIF Controller section of the OMAP4430 TRM.

Table 2-4. LPDDR2 Signal Descriptions

SIGNAL NAME [1]	DESCRIPTION [2]	TYPE [3]	BALL BOTTOM [4]	BALL TOP [5]
lpddr21_dq0	LPDDR21 data bit 0	IO	-	E29
lpddr21_dq1	LPDDR21 data bit 1	IO	-	D28
lpddr21_dq2	LPDDR21 data bit 2	IO	-	B27
lpddr21_dq3	LPDDR21 data bit 3	IO	-	A27
lpddr21_dq4	LPDDR21 data bit 4	IO	-	A26
lpddr21_dq5	LPDDR21 data bit 5	IO	-	B26
lpddr21_dq6	LPDDR21 data bit 6	IO	-	A25
lpddr21_dq7	LPDDR21 data bit 7	IO	-	A24
lpddr21_dq8	LPDDR21 data bit 8	IO	-	B19
lpddr21_dq9	LPDDR21 data bit 9	IO	-	A19
lpddr21_dq10	LPDDR21 data bit 10	IO	-	A18
lpddr21_dq11	LPDDR21 data bit 11	IO	-	A17
lpddr21_dq12	LPDDR21 data bit 12	IO	-	B17
lpddr21_dq13	LPDDR21 data bit 13	IO	-	A13
lpddr21_dq14	LPDDR21 data bit 14	IO	-	A12
lpddr21_dq15	LPDDR21 data bit 15	IO	-	B12
lpddr21_dq16	LPDDR21 data bit 16	IO	-	N28
lpddr21_dq17	LPDDR21 data bit 17	IO	-	N29
lpddr21_dq18	LPDDR21 data bit 18	IO	-	M29
lpddr21_dq19	LPDDR21 data bit 19	IO	-	L28
lpddr21_dq20	LPDDR21 data bit 20	IO	-	K28
lpddr21_dq21	LPDDR21 data bit 21	IO	-	K29
lpddr21_dq22	LPDDR21 data bit 22	IO	-	J29
lpddr21_dq23	LPDDR21 data bit 23	IO	-	H29

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Table 2-4. LPDDR2 Signal Descriptions (continued)

SIGNAL NAME [1]	DESCRIPTION [2]	TYPE [3]	BALL BOTTOM [4]	BALL TOP [5]
lpddr21_dq24	LPDDR21 data bit 24	IO	-	B8
lpddr21_dq25	LPDDR21 data bit 25	IO	-	A8
lpddr21_dq26	LPDDR21 data bit 26	IO	-	A7
lpddr21_dq27	LPDDR21 data bit 27	IO	-	B6
lpddr21_dq28	LPDDR21 data bit 28	IO	-	B5
lpddr21_dq29	LPDDR21 data bit 29	IO	-	A5
lpddr21_dq30	LPDDR21 data bit 30	IO	-	A4
lpddr21_dq31	LPDDR21 data bit 31	IO	-	B3
lpddr21_ca0	LPDDR21 command / address bit 0	O	-	AJ27
lpddr21_ca1	LPDDR21 command / address bit 1	O	-	AH27
lpddr21_ca2	LPDDR21 command / address bit 2	O	-	AH26
lpddr21_ca3	LPDDR21 command / address bit 3	O	-	AH25
lpddr21_ca4	LPDDR21 command / address bit 4	O	-	AJ25
lpddr21_ca5	LPDDR21 command / address bit 5	O	-	AJ20
lpddr21_ca6	LPDDR21 command / address bit 6	O	-	AH20
lpddr21_ca7	LPDDR21 command / address bit 7	O	-	AH19
lpddr21_ca8	LPDDR21 command / address bit 8	O	-	AJ18
lpddr21_ca9	LPDDR21 command / address bit 9	O	-	AH17
lpddr21_dqs0	LPDDR21 data strobe 0	IO	-	A23
lpddr21_ndqs0	LPDDR21 data nstrobe 0	IO	-	B23
lpddr21_dqs1	LPDDR21 data strobe 1	IO	-	A20
lpddr21_ndqs1	LPDDR21 data nstrobe 1	IO	-	B20
lpddr21_dqs2	LPDDR21 data strobe 2	IO	-	G28
lpddr21_ndqs2	LPDDR21 data nstrobe 2	IO	-	G29
lpddr21_dqs3	LPDDR21 data strobe 3	IO	-	B10
lpddr21_ndqs3	LPDDR21 data nstrobe 3	IO	-	A10
lpddr21_dm0	LPDDR21 data mask 0	IO	-	B22
lpddr21_dm1	LPDDR21 data mask 1	IO	-	A21
lpddr21_dm2	LPDDR21 data mask 2	IO	-	F28
lpddr21_dm3	LPDDR21 data mask 3	IO	-	B11
lpddr21_ck	LPDDR21 clock	O	-	AJ21
lpddr21_nck	LPDDR21 clock invert	O	-	AH21
lpddr21_ncs0	LPDDR21 chip 1 select invert	O	-	AH24
lpddr21_ncs1	LPDDR21 chip 2 select invert	O	-	AJ24
lpddr21_cke0	LPDDR21 clock 1 enable	O	-	AH23
lpddr21_cke1	LPDDR21 clock 2 enable	O	-	AJ23
lpddr22_dq0	LPDDR22 data bit 0	IO	-	L2
lpddr22_dq1	LPDDR22 data bit 1	IO	-	M1
lpddr22_dq2	LPDDR22 data bit 2	IO	-	N1
lpddr22_dq3	LPDDR22 data bit 3	IO	-	U2
lpddr22_dq4	LPDDR22 data bit 4	IO	-	V1
lpddr22_dq5	LPDDR22 data bit 5	IO	-	W2
lpddr22_dq6	LPDDR22 data bit 6	IO	-	W1
lpddr22_dq7	LPDDR22 data bit 7	IO	-	Y2
lpddr22_dq8	LPDDR22 data bit 8	IO	-	AE1
lpddr22_dq9	LPDDR22 data bit 9	IO	-	AF1
lpddr22_dq10	LPDDR22 data bit 10	IO	-	AG1

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Table 2-4. LPDDR2 Signal Descriptions (continued)

SIGNAL NAME [1]	DESCRIPTION [2]	TYPE [3]	BALL BOTTOM [4]	BALL TOP [5]
lpddr22_dq11	LPDDR22 data bit 11	IO	-	AG2
lpddr22_dq12	LPDDR22 data bit 12	IO	-	AJ3
lpddr22_dq13	LPDDR22 data bit 13	IO	-	AH4
lpddr22_dq14	LPDDR22 data bit 14	IO	-	AJ5
lpddr22_dq15	LPDDR22 data bit 15	IO	-	AH6
lpddr22_dq16	LPDDR22 data bit 16	IO	-	C2
lpddr22_dq17	LPDDR22 data bit 17	IO	-	D1
lpddr22_dq18	LPDDR22 data bit 18	IO	-	E1
lpddr22_dq19	LPDDR22 data bit 19	IO	-	E2
lpddr22_dq20	LPDDR22 data bit 20	IO	-	F2
lpddr22_dq21	LPDDR22 data bit 21	IO	-	G1
lpddr22_dq22	LPDDR22 data bit 22	IO	-	H1
lpddr22_dq23	LPDDR22 data bit 23	IO	-	H2
lpddr22_dq24	LPDDR22 data bit 24	IO	-	AJ9
lpddr22_dq25	LPDDR22 data bit 25	IO	-	AJ10
lpddr22_dq26	LPDDR22 data bit 26	IO	-	AH10
lpddr22_dq27	LPDDR22 data bit 27	IO	-	AH11
lpddr22_dq28	LPDDR22 data bit 28	IO	-	AJ12
lpddr22_dq29	LPDDR22 data bit 29	IO	-	AJ13
lpddr22_dq30	LPDDR22 data bit 30	IO	-	AH13
lpddr22_dq31	LPDDR22 data bit 31	IO	-	AJ14
lpddr22_ca0	LPDDR22 command / address bit 0	O	-	R29
lpddr22_ca1	LPDDR22 command / address bit 1	O	-	T29
lpddr22_ca2	LPDDR22 command / address bit 2	O	-	U29
lpddr22_ca3	LPDDR22 command / address bit 3	O	-	V29
lpddr22_ca4	LPDDR22 command / address bit 4	O	-	W28
lpddr22_ca5	LPDDR22 command / address bit 5	O	-	AC29
lpddr22_ca6	LPDDR22 command / address bit 6	O	-	AD29
lpddr22_ca7	LPDDR22 command / address bit 7	O	-	AD28
lpddr22_ca8	LPDDR22 command / address bit 8	O	-	AE28
lpddr22_ca9	LPDDR22 command / address bit 9	O	-	AF29
lpddr22_dqs0	LPDDR22 data strobe 0	O	-	AA1
lpddr22_ndqs0	LPDDR22 data nstrobe 0	O	-	AA2
lpddr22_dqs1	LPDDR22 data strobe 1	O	-	AD2
lpddr22_ndqs1	LPDDR22 data nstrobe 1	O	-	AD1
lpddr22_dqs2	LPDDR22 data strobe 2	O	-	K2
lpddr22_ndqs2	LPDDR22 data nstrobe 2	O	-	K1
lpddr22_dqs3	LPDDR22 data strobe 3	O	-	AH8
lpddr22_ndqs3	LPDDR22 data nstrobe 3	O	-	AJ8
lpddr22_dm0	LPDDR22 data mask 0	IO	-	AB1
lpddr22_dm1	LPDDR22 data mask 1	IO	-	AC2
lpddr22_dm2	LPDDR22 data mask 2	IO	-	L1
lpddr22_dm3	LPDDR22 data mask 3	IO	-	AH7
lpddr22_ck	LPDDR22 clock	O	-	AB28
lpddr22_nck	LPDDR22 clock invert	O	-	AB29
lpddr22_ncs0	LPDDR22 chip select 0 invert	O	-	Y28
lpddr22_ncs1	LPDDR22 chip select 1 invert	O	-	W29

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Table 2-4. LPDDR2 Signal Descriptions (continued)

SIGNAL NAME [1]	DESCRIPTION [2]	TYPE [3]	BALL BOTTOM [4]	BALL TOP [5]
lpddr22_cke0	LPDDR22 clock 0 enable	O	-	AA29
lpddr22_cke1	LPDDR22 clock 1 enable	O	-	Y29

2.4.2 Video Interfaces

2.4.2.1 Camera

NOTE

For more information, see the Imaging Subsystem / ISS Interfaces section of the OMAP4430 TRM.

2.4.2.1.1 Camera Control

Table 2-5. Camera Control Signal Descriptions

SIGNAL NAME [1]	DESCRIPTION [2]	TYPE [3]	BALL BOTTOM [4]	BALL TOP [5]
cam_shutter	Camera mechanical shutter control	O	T27	-
cam_strobe	Camera flash activation trigger	O	U27	-
cam_globalreset	Camera sensor reset	IO	V27	-

2.4.2.1.2 CSI21

Table 2-6. CSI21 Signal Descriptions

SIGNAL NAME [1]	DESCRIPTION [2]	TYPE [3]	BALL BOTTOM [4]	BALL TOP [5]
csi21_dx0	CSI2 (CSI21) camera lane 0 differential x	IDS	R26	-
csi21_dy0	CSI2 (CSI21) camera lane 0 differential y	IDS	R25	-
csi21_dx1	CSI2 (CSI21) camera lane 1 differential x	IDS	T26	-
csi21_dy1	CSI2 (CSI21) camera lane 1 differential y	IDS	T25	-
csi21_dx2	CSI2 (CSI21) camera lane 2 differential x	IDS	U26	-
csi21_dy2	CSI2 (CSI21) camera lane 2 differential y	IDS	U25	-
csi21_dx3	CSI2 (CSI21) camera lane 3 differential x	IDS	V26	-
csi21_dy3	CSI2 (CSI21) camera lane 3 differential y	IDS	V25	-
csi21_dx4	CSI2 (CSI21) camera lane 4 differential x	IDS	W26	-
csi21_dy4	CSI2 (CSI21) camera lane 4 differential y	IDS	W25	-

2.4.2.1.3 CSI22 (CCP2)

Table 2-7. CSI22 Signal Descriptions

SIGNAL NAME [1]	DESCRIPTION [2]	TYPE [3]	BALL BOTTOM [4]	BALL TOP [5]
csi22_dx0	CSI2 (CSI22) camera lane 0 differential x	IDS	M26	-
csi22_dy0	CSI2 (CSI22) camera lane 0 differential y	IDS	M25	-
csi22_dx1	CSI2 (CSI22) camera lane 1 differential x	IDS	N26	-
csi22_dy1	CSI2 (CSI22) camera lane 1 differential y	IDS	N25	-

2.4.2.2 Display

NOTE

For more information, see the Display Subsystem / Display Subsystem Overview / DSS Environment section of the OMAP4430 TRM.

2.4.2.2.1 RFBI

Table 2-8. RFBI Signal Descriptions

SIGNAL NAME [1]	DESCRIPTION [2]	TYPE [3]	BALL BOTTOM [4]	BALL TOP [5]
rfbi_data0	RFBI data bit 0	IO	AC4	-
rfbi_data1	RFBI data bit 1	IO	AB4	-
rfbi_data2	RFBI data bit 2	IO	AB3	-
rfbi_data3	RFBI data bit 3	IO	AB2	-
rfbi_data4	RFBI data bit 4	IO	AA4	-
rfbi_data5	RFBI data bit 5	IO	AA3	-
rfbi_data6	RFBI data bit 6	IO	AA2	-
rfbi_data7	RFBI data bit 7	IO	AA1	-
rfbi_data8	RFBI data bit 8	IO	Y4	-
rfbi_data9	RFBI data bit 9	IO	V2	-
rfbi_data10	RFBI data bit 10	IO	V1	-
rfbi_data11	RFBI data bit 11	IO	AE9	-
rfbi_data12	RFBI data bit 12	IO	AG10	-
rfbi_data13	RFBI data bit 13	IO	AF10	-
rfbi_data14	RFBI data bit 14	IO	AE10	-
rfbi_data15	RFBI data bit 15	IO	AH11	-
rfbi_a0	RFBI data / control selection	O	Y3	-
rfbi_we	RFBI write enable	O	Y2	-
rfbi_re	RFBI read enable	O	W4	-
rfbi_cs0	RFBI chip select	O	W3	-
rfbi_te_vsync0	RFBI vertical synchronization / tearing effect control signal	I	W1	-
rfbi_hsync0	RFBI horizontal synchronization / tearing effect control signal	I	W2	-

2.4.2.2.2 DSI1

Table 2-9. DSI1 Signal Descriptions

SIGNAL NAME [1]	DESCRIPTION [2]	TYPE [3]	BALL BOTTOM [4]	BALL TOP [5]
dsi1_dx0	DSI1 display lane 0 differential positive or negative	IODS	P3	-
dsi1_dy0	DSI1 display lane 0 differential positive or negative	IODS	P4	-
dsi1_dx1	DSI1 display lane 1 differential positive or negative	IODS	N3	-
dsi1_dy1	DSI1 display lane 1 differential positive or negative	IODS	N4	-
dsi1_dx2	DSI1 display lane 2 differential positive or negative	IODS	M3	-
dsi1_dy2	DSI1 display lane 2 differential positive or negative	IODS	M4	-
dsi1_dx3	DSI1 display lane 3 differential positive or negative	IODS	L3	-
dsi1_dy3	DSI1 display lane 3 differential positive or negative	IODS	L4	-
dsi1_dx4	DSI1 display lane 4 differential positive or negative	IODS	K3	-
dsi1_dy4	DSI1 display lane 4 differential positive or negative	IODS	K4	-

Table 2-9. DSI1 Signal Descriptions (continued)

SIGNAL NAME [1]	DESCRIPTION [2]	TYPE [3]	BALL BOTTOM [4]	BALL TOP [5]
dsi1_te0	DSI1 tearing effect input 0	IDS	C25 / A24 / AB2	-
dsi1_te1	DSI1 tearing effect input 1	IDS	D25 / B24 / AB3	-

2.4.2.2.3 DSI2

Table 2-10. DSI2 Signal Descriptions

SIGNAL NAME [1]	DESCRIPTION [2]	TYPE [3]	BALL BOTTOM [4]	BALL TOP [5]
dsi2_dx0	DSI2 display lane 0 differential positive or negative	IODS	T3	-
dsi2_dy0	DSI2 display lane 0 differential positive or negative	IODS	T4	-
dsi2_dx1	DSI2 display lane 1 differential positive or negative	IODS	U3	-
dsi2_dy1	DSI2 display lane 1 differential positive or negative	IODS	U4	-
dsi2_dx2	DSI2 display lane 2 differential positive or negative	IODS	V3	-
dsi2_dy2	DSI2 display lane 2 differential positive or negative	IODS	V4	-
dsi2_te0	DSI2 tearing effect input 0	IDS	C23 / C24 / AB4	-
dsi2_te1	DSI2 tearing effect input 1	IDS	B26 / D24 / AC4	-

2.4.2.2.4 CVIDEO

Table 2-11. CVIDEO Signal Descriptions

SIGNAL NAME [1]	DESCRIPTION [2]	TYPE [3]	BALL BOTTOM [4]	BALL TOP [5]
cvideo_tvout	CVIDEO TV analog composite output	AO	B7	-
cvideo_vfb	CVIDEO input feedback thru resistor to out	AO	C7	-
cvideo_rset	CVIDEO input reference current resistor setting	AIO	D7	-

2.4.2.2.5 HDMI

Table 2-12. HDMI Signal Descriptions

SIGNAL NAME [1]	DESCRIPTION [2]	TYPE [3]	BALL BOTTOM [4]	BALL TOP [5]
hdmi_cec	HDMI consumer electronic control	IO	B10	-
hdmi_hpd	HDMI display hot plug detect	I	B9	-
hdmi_ddc_scl	HDMI display data channel clock	IOD	A8	-
hdmi_ddc_sda	HDMI display data channel data	IOD	B8	-
hdmi_data0x(1)	HDMI data 0 differential positive or negative	ODS	C10	-
hdmi_data0y(1)	HDMI data 0 differential positive or negative	ODS	D10	-
hdmi_data1x(1)	HDMI data 1 differential positive or negative	ODS	C9	-
hdmi_data1y(1)	HDMI data 1 differential positive or negative	ODS	D9	-
hdmi_data2x(1)	HDMI data 2 differential positive or negative	ODS	C8	-
hdmi_data2y(1)	HDMI data 2 differential positive or negative	ODS	D8	-
hdmi_clockx(1)	HDMI clock differential positive or negative	ODS	C11	-
hdmi_clocky(1)	HDMI clock differential positive or negative	ODS	D11	-

(1) The function (data or clock) supported on each lane is programmable. For more information on HDMI, please contact your TI representative.

2.4.2.2.6 DISPC

Table 2-13. DISPC Signal Descriptions

SIGNAL NAME [1]	DESCRIPTION [2]	TYPE [3]	BALL BOTTOM [4]	BALL TOP [5]
dispc2_data0	DISPC data to LCD2 panel - data bit 0	O	AC4	-
dispc2_data1	DISPC data to LCD2 panel - data bit 1	O	AB4	-
dispc2_data2	DISPC data to LCD2 panel - data bit 2	O	AB3	-
dispc2_data3	DISPC data to LCD2 panel - data bit 3	O	AB2	-
dispc2_data4	DISPC data to LCD2 panel - data bit 4	O	AA4	-
dispc2_data5	DISPC data to LCD2 panel - data bit 5	O	AA3	-
dispc2_data6	DISPC data to LCD2 panel - data bit 6	O	AA2	-
dispc2_data7	DISPC data to LCD2 panel - data bit 7	O	AA1	-
dispc2_data8	DISPC data to LCD2 panel - data bit 8	O	Y4	-
dispc2_data9	DISPC data to LCD2 panel - data bit 9	O	V2	-
dispc2_data10	DISPC data to LCD2 panel - data bit 10	O	V1	-
dispc2_data11	DISPC data to LCD2 panel - data bit 11	O	AE9	-
dispc2_data12	DISPC data to LCD2 panel - data bit 12	O	AG10	-
dispc2_data13	DISPC data to LCD2 panel - data bit 13	O	AF10	-
dispc2_data14	DISPC data to LCD2 panel - data bit 14	O	AE10	-
dispc2_data15	DISPC data to LCD2 panel - data bit 15	O	AH11	-
dispc2_data16	DISPC data to LCD2 panel - data bit 16	O	W1	-
dispc2_data17	DISPC data to LCD2 panel - data bit 17	O	W2	-
dispc2_data18	DISPC data to LCD2 panel - data bit 18	O	AG11	-
dispc2_data19	DISPC data to LCD2 panel - data bit 19	O	AF11	-
dispc2_data20	DISPC data to LCD2 panel - data bit 20	O	AE11	-
dispc2_data21	DISPC data to LCD2 panel - data bit 21	O	AG13	-
dispc2_data22	DISPC data to LCD2 panel - data bit 22	O	AE12	-
dispc2_data23	DISPC data to LCD2 panel - data bit 23	O	AF12	-
dispc2_hsync	DISPC horizontal synchronization from dispc to LCD2	O	W3	-
dispc2_vsync	DISPC vertical synchronization from dispc to LCD2	O	Y2	-
dispc2_de	DISPC ac bias output enable or data enable to LCD2	O	Y3	-
dispc2_pclk	DISPC LCD pixel clock to LCD2	O	W4	-
dispc2_fid	DISPC field ID to LCD2	O	P2	-

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2.4.3 Serial Communication Interfaces

2.4.3.1 HDQ/1-Wire

NOTE

For more information, see the Serial Communication Interface / HDQ/1-Wire section of the OMAP4430 TRM.

Table 2-14. HDQ/1-Wire Signal Descriptions

SIGNAL NAME [1]	DESCRIPTION [2]	TYPE [3]	BALL BOTTOM [4]	BALL TOP [5]
hdq_sio	HDQ™ 1-Wire® control and data interface	IOD	AA27	-

2.4.3.2 I^{2}C

NOTE

For more information, see the Serial Communication Interface / Multimaster High-Speed I^{2}C Controller / HS I^{2}C Environment / HS I^{2}C in I^{2}C Mode section of the OMAP4430 TRM.

Table 2-15. I^{2}C Signal Descriptions

SIGNAL NAME [1]	DESCRIPTION [2]	TYPE [3]	BALL BOTTOM [4]	BALL TOP [5]
Inter-Integrated Circuit Interface (I2C1)				
i2c1_scl	I2C1 clock	OD	AE28	-
i2c1_sda	I2C1 data	IOD	AE26	-
Inter-Integrated Circuit Interface (I2C2)				
i2c2_scl	I2C2 clock	OD	C26	-
i2c2_sda	I2C2 data	IOD	D26	-
i2c2_sccb	I2C2 serial camera control bus	OD	AA27	-
Inter-Integrated Circuit Interface (I2C3)				
i2c3_scl	I2C3 clock	OD	W27	-
i2c3_sda	I2C3 data	IOD	Y27	-
i2c3_sccb	I2C3 serial camera control bus	OD	AA27	-
Inter-Integrated Circuit Interface (I2C4)				
i2c4_scl	I2C4 clock	OD	AG21	-
i2c4_sda	I2C4 data	IOD	AH22	-

2.4.3.3 SmartReflex™

NOTE

For more information, see:

- The Power, Reset and Clock Management / Device Power Management Introduction / Device Power-Management Architecture Building Blocks / Voltage Management / AVS Overview section or
- The Power, Reset and Clock Management / PRCM Subsystem Environment / External Power Control Signals section

of the OMAP4430 TRM.

Table 2-16. SmartReflex Signal Descriptions

SIGNAL NAME [1]	DESCRIPTION [2]	TYPE [3]	BALL BOTTOM [4]	BALL TOP [5]
sr_scl	Smart-Reflex clock	OD	AG9	-
sr_sda	Smart-Reflex data	IOD	AF9	-

2.4.3.4 McBSP

NOTE

For more information, see the Serial Communication Interface / Multichannel Buffered Serial Port (McBSP) section of the OMAP4430 TRM.

Table 2-17. McBSP1, 2, 3 Signal Descriptions

SIGNAL NAME [1]	DESCRIPTION [2]	TYPE [3]	BALL BOTTOM [4]	BALL TOP [5]
abe_clks	ABE clock input	I	AH26	-

Table 2-17. McBSP1, 2, 3 Signal Descriptions (continued)

SIGNAL NAME [1]	DESCRIPTION [2]	TYPE [3]	BALL BOTTOM [4]	BALL TOP [5]
Audio Backend Multichannel Buffered Serial Port (ABE McBSP1)				
abe_mcbsp1_dr	ABE McBSP1 received serial data	I	AC25	-
abe_mcbsp1_dx	ABE McBSP1 transmitted serial data	IO	AB25	-
abe_mcbsp1_clkx	ABE McBSP1 combined serial clock	IO	AC26	-
abe_mcbsp1_fsx	ABE McBSP1 combined frame synchronization	IO	AC27	-
Audio Backend Multichannel Buffered Serial Port (ABE McBSP2)				
abe_mcbsp2_dr	ABE McBSP2 received serial data	I	AD26	-
abe_mcbsp2_dx	ABE McBSP2 transmitted serial data	IO	AD25	-
abe_mcbsp2_clkx	ABE McBSP2 combined serial clock	IO	AD27	-
abe_mcbsp2_fsx	ABE McBSP2 combined frame synchronization	IO	AC28	-
Audio Backend Multichannel Buffered Serial Port (ABE McBSP3)				
abe_mcbsp3_dr	ABE McBSP3 received serial data	I	AH17 / AG25	-
abe_mcbsp3_dx	ABE McBSP3 transmitted serial data	IO	AE16 / AF25	-
abe_mcbsp3_clkx	ABE McBSP3 combined serial clock	IO	AF16 / AE25	-
abe_mcbsp3_fsx	ABE McBSP3 combined frame synchronization	IO	AG16 / AF26	-

Table 2-18. McBSP4 Signal Descriptions

SIGNAL NAME [1]	DESCRIPTION [2]	TYPE [3]	BALL BOTTOM [4]	BALL TOP [5]
abe_clks	ABE clock input	I	AH26	-
mcbsp4_dr	McBSP4 received serial data	I	AE17	-
mcbsp4_dx	McBSP4 transmitted serial data	IO	AG18	-
mcbsp4_clkx	McBSP4 transmitted serial clock	IO	AF18	-
mcbsp4_fsx	McBSP4 transmitted frame synchronization	IO	AE19	-
mcbsp4_clkr	McBSP4 received serial clock	IO	AG19	-
mcbsp4_fsr	McBSP4 received frame synchronization	IO	AF19	-

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2.4.3.5 PDM

NOTE

For more information, see the Serial Communication Interface / Multichannel PDM Controller section of the OMAP4430 TRM.

Table 2-19. ABE McPDM Signal Descriptions

SIGNAL NAME [1]	DESCRIPTION [2]	TYPE [3]	BALL BOTTOM [4]	BALL TOP [5]
abe_clks	ABE clock input	I	AH26	-
abe_pdm_ul_data	ABE PDM data stream from TWL6030 PMIC to OMAP4430	I	AG25	-
abe_pdm_dl_data	ABE PDM data stream from OMAP4430 to TWL6030 PMIC	O	AF25	-
abe_pdm_frame	ABE PDM Frame synchronization	IO	AE25	-
abe_pdm_lb_clk	ABE PDM loop back clock	O	AF26	-

2.4.3.6 DMIC

NOTE

For more information, see the Serial Communication Interface / Digital Microphone Module section of the OMAP4430 TRM.

Table 2-20. ABE DMIC Signal Descriptions

SIGNAL NAME [1]	DESCRIPTION [2]	TYPE [3]	BALL BOTTOM [4]	BALL TOP [5]
abe_clks	ABE clock input	I	AH26	-
abe_dmic_clk1	ABE digital microphone clock output 1	O	AE24	-
abe_dmic_clk2	ABE digital microphone clock output 2	O	AH24	-
abe_dmic_clk3	ABE digital microphone clock output 3	O	AG16	-
abe_dmic_din1	ABE digital microphone data input 1	I	AF24	-
abe_dmic_din2	ABE digital microphone data input 2	I	AG24	-
abe_dmic_din3	ABE digital microphone data input 3	I	AF16 / AH24	-

2.4.3.7 McASP

NOTE

For more information, see the Serial Communication Interface / Multichannel Audio Serial Port section of the OMAP4430 TRM.

Table 2-21. ABE McASP Signal Descriptions

SIGNAL NAME [1]	DESCRIPTION [2]	TYPE [3]	BALL BOTTOM [4]	BALL TOP [5]
abe_clks	ABE clock input	I	AH26	-
abe_mcasp_axr	ABE McASP serial data IO	IO	AD26 / AG24	-
abe_mcasp_aclkx	ABE McASP clock transmit	O	AB25	-
abe_mcasp_afsx	ABE McASP frame synchonization transmit	O	AC28	-
abe_mcasp_ahclkx	ABE McASP high frequency clock output	O	AD27	-
abe_mcasp_amutein	ABE McASP auto mute input	I	AC27	-
abe_mcasp_amute	ABE McASP auto mute output	O	AD25	-

2.4.3.8 SLIMbus®

NOTE

For more information, see the Serial Communication Interface / Serial Low-Power Inter-Chip Media Bus Controller section of the OMAP4430 TRM.

Table 2-22. ABE SLIMbus1 Signal Descriptions

SIGNAL NAME [1]	DESCRIPTION [2]	TYPE [3]	BALL BOTTOM [4]	BALL TOP [5]
abe_clks	ABE clock input	I	AH26	-
abe_slimbus1_clock	ABE SLIMbus1 clock	IO	AC26	-
abe_slimbus1_data	ABE SLIMbus1 data	IO	AC25	-

Table 2-23. SLIMbus2 Signal Descriptions

SIGNAL NAME [1]	DESCRIPTION [2]	TYPE [3]	BALL BOTTOM [4]	BALL TOP [5]
abe_clks	ABE clock input	I	AH26	-
slimbus2_clock	SLIMbus2 clock	IO	AG24 / AG23	-
slimbus2_data	SLIMbus2 data	IO	AH24 / AH23	-

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2.4.3.9 HSI

NOTE

For more information, see the Serial Communication Interface / MIPI-HSI section of the OMAP4430 TRM.

Table 2-24. HSI Signal Descriptions

SIGNAL NAME [1]	DESCRIPTION [2]	TYPE [3]	BALL BOTTOM [4]	BALL TOP [5]
High-speed Synchronous Serial Interface (HSI1)				
hsi1_cawake	HSI1 cellular modem to APE wake signal	I	AE18	-
hsi1_cadata	HSI1 cellular modem to APE signal	I	AG19	-
hsi1_caflag	HSI1 cellular modem to APE flag signal	I	AF19	-
hsi1_acready	HSI1 APE to cellular modem ready signal	O	AE19	-
hsi1_acwake	HS1 APE to cellular modem wake signal	O	AF18	-
hsi1_acdata	HSI1 APE to cellular modem data signal	O	AG18	-
hsi1_acflag	HSI1 APE to cellular modem ready signal	O	AE17	-
hsi1_caready	HSI1 cellular modem to APE ready signal	I	AF17	-
High-speed Synchronous Serial Interface (HSI2)				
hsi2_cawake	HSI2 cellular modem to APE wake signal	I	AG12	-
hsi2_cadata	HSI2 cellular modem to APE signal	I	AF12	-
hsi2_caflag	HSI2 cellular modem to APE flag signal	I	AE12	-
hsi2_acready	HSI2 APE to cellular modem ready signal	O	AG13	-
hsi2_acwake	HSI2 APE to cellular modem wake signal	O	AE11	-
hsi2_acdata	HSI2 APE to cellular modem data signal	O	AF11	-
hsi2_acflag	HSI2 APE to cellular modem ready signal	O	AG11	-
hsi2_caready	HSI2 cellular modem to APE ready signal	I	AH11	-

2.4.3.10 McSPI

NOTE

For more information, see the Serial Communication Interface / Multichannel Serial Port Interface (MCSPI) section of the OMAP4430 TRM.

Table 2-25. McSPI Signal Descriptions

SIGNAL NAME [1]	DESCRIPTION [2]	TYPE [3]	BALL BOTTOM [4]	BALL TOP [5]
Multichannel Serial Port Interface (McSPI1)				
mcspi1_clk	McSPI1 clock (slave input, master output)	IO	AF22	-
mcspi1_somi	McSPI1 data (slave output, master input, Z when not shifting)	IO	AE22	-
mcspi1_simo	McSPI1 data (slave input, master output, Z when not shifting)	IO	AG22	-
mcspi1_cs0	McSPI1 chip select 0 (slave input, master output)	IO	AE23	-
mcspi1_cs1	McSPI1 chip select 1	O	AF23	-
mcspi1_cs2	McSPI1 chip select 2	O	AG23	-
mcspi1_cs3	McSPI1 chip select 3	O	AH23	-
Multichannel Serial Port Interface (McSPI2)				
mcspi2_clk	McSPI2 clock (slave input, master output)	IO	AD27 / AE5	-
mcspi2_somi	McSPI2 data (slave output, master input, Z when not shifting)	IO	AD26 / AE4	-
mcspi2_simo	McSPI2 data (slave input, master output, Z if not shifting)	IO	AD25 / AF5	-
mcspi2_cs0	McSPI2 chip select 0 (slave input, master output)	IO	AC28 / AF3	-

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Table 2-25. McSPI Signal Descriptions (continued)

SIGNAL NAME [1]	DESCRIPTION [2]	TYPE [3]	BALL BOTTOM [4]	BALL TOP [5]
mcspi2_cs1	McSPI2 chip select 1	O	AG3	-
Multichannel Serial Port Interface (McSPI3)				
mcspi3_clk	McSPI3 clock (slave input, master output)	IO	AE9	-
mcspi3_somi	McSPI3 data (slave output, master input, Z when not shifting)	IO	AE10	-
mcspi3_simo	McSPI3 data (slave input, master output, Z if not shifting)	IO	AG10	-
mcspi3_cs0	McSPI3 chip select 0 (slave input, master output)	IO	AF10	-
Multichannel Serial Port Interface (McSPI4)				
mcspi4_clk	McSPI4 clock (slave input, master output)	IO	AE21	-
mcspi4_somi	McSPI4 data (slave output, master input, Z when not shifting)	IO	AF21	-
mcspi4_simo	McSPI4 data (slave input, master output, Z if not shifting)	IO	AF20	-
mcspi4_cs0	McSPI4 chip select 0 (slave input, master output)	IO	AE20	-

2.4.3.11 UART

NOTE

For more information, see the Serial Communication Interface / UART/IrDA/CIR section of the OMAP4430 TRM.

Table 2-26. UART Signal Descriptions

SIGNAL NAME [1]	DESCRIPTION [2]	TYPE [3]	BALL BOTTOM [4]	BALL TOP [5]
Universal Asynchronous Receiver/Transmitter (UART1)				
uart1_cts	UART1 clear to send	I	AG23	-
uart1_rts	UART1 request to send	O	AH23	-
uart1_rx	UART1 receive data	I	E3 / C26 / AF23 / AA3	-
uart1_tx	UART1 transmit data	O	D26 / F27	-
Universal Asynchronous Receiver/Transmitter (UART2)				
uart2_cts	UART2 clear to send	I	AB26	-
uart2_rts	UART2 request to send	O	AB27	-
uart2_rx	UART2 receive data	I	AA25 / B5	-
uart2_tx	UART2 transmit data	O	AA26 / B4	-
Universal Asynchronous Receiver/Transmitter (UART3)				
uart3_cts_rctx	UART3 clear to send or remote control data output	IO	F27 / Y2	-
uart3_rts_sd	UART3 request to send or infrared transceiver shutdown	O	F28 / W4	-
uart3_rx_irrx	UART3 receive data input or infrared data input	I	G27 / B5 / W3	-
uart3_tx_irtx	UART3 transmit data output or infrared data output	O	G28 / B4 / W2	-
Universal Asynchronous Receiver/Transmitter (UART4)				
uart4_rx	UART4 receive data	I	AG20	-
uart4_tx	UART4 transmit data	O	AH19	-
uart4_cts	UART4 clear to send	I	AE24	-
uart4_rts	UART4 request to send	O	AF24	-

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2.4.3.12 USB

NOTE

For more information, see:

- Serial Communication Interface / High-Speed Multiport USB Host Subsystem section, or
- Serial Communication Interface / High-Speed USB OTG Controller section, or
- Serial Communication Interface / Full-Speed USB Host Controller section

of the OMAP4430 TRM.

Table 2-27. USB Signal Descriptions

SIGNAL NAME [1]	DESCRIPTION [2]	TYPE [3]	BALL BOTTOM [4]	BALL TOP [5]
Universal Serial Bus (USBA0)				
usba0_ulpiphy_clk	USBA0 IO to/from external transceiver 60-MHz clock	I	P2	-
usba0_ulpiphy_stp	USBA0 output to external transceiver to stop data stream	O	V1	-
usba0_ulpiphy_dir	USBA0 data direction control from external transceiver	I	V2	-
usba0_ulpiphy_nxt	USBA0 next signal control from external transceiver	I	W1	-
usba0_ulpiphy_dat0	USBA0 data bit 0 to/from external transceiver	IO	W2	-
usba0_ulpiphy_dat1	USBA0 data bit 1 to/from external transceiver	IO	W3	-
usba0_ulpiphy_dat2	USBA0 data bit 2 to/from external transceiver	IO	W4	-
usba0_ulpiphy_dat3	USBA0 data bit 3 to/from external transceiver	IO	Y2	-
usba0_ulpiphy_dat4	USBA0 data bit 4 to/from external transceiver	IO	Y3	-
usba0_ulpiphy_dat5	USBA0 data bit 5 to/from external transceiver	IO	Y4	-
usba0_ulpiphy_dat6	USBA0 data bit 6 to/from external transceiver	IO	AA1	-
usba0_ulpiphy_dat7	USBA0 data bit 7 to/from external transceiver	IO	AA2	-
usba0_otg_ce	USBA0 OTG charging enable signal	O	C3	-
usba0_otg_dp	USBA0 OTG data p	IODS	B5	-
usba0_otg_dm	USBA0 OTG data m	IODS	B4	-
Universal Serial Bus (USBB1)				
usbb1_ulpiphy_clk	USBB1 IO to/from external transceiver 60-MHz clock	I	AE18	-
usbb1_ulpiphy_stp	USBB1 output to external transceiver to stop data stream	O	AG19	-
usbb1_ulpiphy_dir	USBB1 data direction control from external transceiver	I	AF19	-
usbb1_ulpiphy_nxt	USBB1 next signal control from external transceiver	I	AE19	-
usbb1_ulpiphy_dat0	USBB1 data bit 0 to/from external transceiver	IO	AF18	-
usbb1_ulpiphy_dat1	USBB1 data bit 1 to/from external transceiver	IO	AG18	-
usbb1_ulpiphy_dat2	USBB1 data bit 2 to/from external transceiver	IO	AE17	-
usbb1_ulpiphy_dat3	USBB1 data bit 3 to/from external transceiver	IO	AF17	-
usbb1_ulpiphy_dat4	USBB1 data bit 4 to/from external transceiver	IO	AH17	-
usbb1_ulpiphy_dat5	USBB1 data bit 5 to/from external transceiver	IO	AE16	-
usbb1_ulpiphy_dat6	USBB1 data bit 6 to/from external transceiver	IO	AF16	-
usbb1_ulpiphy_dat7	USBB1 data bit 7 to/from external transceiver	IO	AG16	-
usbb1_ulpitll_clk	USBB1 ULPI TLL Clock	O	AE18	-
usbb1_ulpitll_stp	USBB1 ULPI TLL Stop	I	AG19	-
usbb1_ulpitll_dir	USBB1 ULPI TLL Dir	O	AF19	-
usbb1_ulpitll_nxt	USBB1 ULPI TLL Next	O	AE19	-
usbb1_ulpitll_dat0	USBB1 ULPI TLL data bit 0	IO	AF18	-
usbb1_ulpitll_dat1	USBB1 ULPI TLL data bit 1	IO	AG18	-

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Table 2-27. USB Signal Descriptions (continued)

SIGNAL NAME [1]	DESCRIPTION [2]	TYPE [3]	BALL BOTTOM [4]	BALL TOP [5]
usbb1_ulpitll_dat2	USBB1 ULPI TLL data bit 2	IO	AE17	-
usbb1_ulpitll_dat3	USBB1 ULPI TLL data bit 3	IO	AF17	-
usbb1_ulpitll_dat4	USBB1 ULPI TLL data bit 4	IO	AH17	-
usbb1_ulpitll_dat5	USBB1 ULPI TLL data bit 5	IO	AE16	-
usbb1_ulpitll_dat6	USBB1 ULPI TLL data bit 6	IO	AF16	-
usbb1_ulpitll_dat7	USBB1 ULPI TLL data bit 7	IO	AG16	-
usbb1_hsic_data	USBB1 Inter chip data	IO	AF14	-
usbb1_hsic_strobe	USBB1 Inter chip strobe	IO	AE14	-
usbb1_mm_rxdm	USBB1 Vminus receive data (not used in 3- or 4-pin configurations)	IO	AE19	-
usbb1_mm_rxdp	USBB1 Vplus receive data (not used in 3- or 4-pin configurations)	IO	AG19	-
usbb1_mm_rxrcv	USBB1 differential receiver signal input (not used in 3-pin mode)	IO	AF17	-
usbb1_mm_txse0	USBB1 single-ended zero. Used as VM in 4-pin VP_VM mode.	IO	AE17	-
usbb1_mm_txdat	USBB1 data. Used as VP in 4-pin VP_VM mode.	IO	AG18	-
usbb1_mm_txen	USBB1 transmit enable	IO	AF18	-
Universal Serial Bus (USBB2)				
usbb2_ulpiphy_clk	USBB2 IO to/from external transceiver 60-MHz clock	I	AG12	-
usbb2_ulpiphy_stp	USBB2 output to external transceiver to stop data stream	O	AF12	-
usbb2_ulpiphy_dir	USBB2 data direction control from external transceiver	I	AE12	-
usbb2_ulpiphy_nxt	USBB2 next signal control from external transceiver	I	AG13	-
usbb2_ulpiphy_dat0	USBB2 data bit 0 to/from external transceiver	IO	AE11	-
usbb2_ulpiphy_dat1	USBB2 data bit 1 to/from external transceiver	IO	AF11	-
usbb2_ulpiphy_dat2	USBB2 data bit 2 to/from external transceiver	IO	AG11	-
usbb2_ulpiphy_dat3	USBB2 data bit 3 to/from external transceiver	IO	AH11	-
usbb2_ulpiphy_dat4	USBB2 data bit 4 to/from external transceiver	IO	AE10	-
usbb2_ulpiphy_dat5	USBB2 data bit 5 to/from external transceiver	IO	AF10	-
usbb2_ulpiphy_dat6	USBB2 data bit 6 to/from external transceiver	IO	AG10	-
usbb2_ulpiphy_dat7	USBB2 data bit 7 to/from external transceiver	IO	AE9	-
usbb2_ulpitll_clk	USBB2 ULPI TLL Clock	O	AG12	-
usbb2_ulpitll_stp	USBB2 ULPI TLL Stop	I	AF12	-
usbb2_ulpitll_dir	USBB2 ULPI TLL Dir	O	AE12	-
usbb2_ulpitll_nxt	USBB2 ULPI TLL Next	O	AG13	-
usbb2_ulpitll_dat0	USBB2 ULPI TLL data bit 0	IO	AE11	-
usbb2_ulpitll_dat1	USBB2 ULPI TLL data bit 1	IO	AF11	-
usbb2_ulpitll_dat2	USBB2 ULPI TLL data bit 2	IO	AG11	-
usbb2_ulpitll_dat3	USBB2 ULPI TLL data bit 3	IO	AH11	-
usbb2_ulpitll_dat4	USBB2 ULPI TLL data bit 4	IO	AE10	-
usbb2_ulpitll_dat5	USBB2 ULPI TLL data bit 5	IO	AF10	-
usbb2_ulpitll_dat6	USBB2 ULPI TLL data bit 6	IO	AG10	-
usbb2_ulpitll_dat7	USBB2 ULPI TLL data bit 7	IO	AE9	-
usbb2_hsic_data	USBB2 Inter chip data	IO	AF13	-
usbb2_hsic_strobe	USBB2 Inter chip strobe	IO	AE13	-
usbb2_mm_rxdm	USBB2 Vminus receive data (not used in 3- or 4-pin configurations)	IO	AD27	-

Table 2-27. USB Signal Descriptions (continued)

SIGNAL NAME [1]	DESCRIPTION [2]	TYPE [3]	BALL BOTTOM [4]	BALL TOP [5]
usbb2_mm_rxdp	USBB2 Vplus receive data (not used in 3- or 4-pin configurations)	IO	AD26	-
usbb2_mm_rxrcv	USBB2 differential receiver signal input (not used in 3-pin mode)	IO	AD25	-
usbb2_mm_txse0	USBB2 single-ended zero. Used as VM in 4-pin VP_VM mode.	IO	AE24 / AG11	-
usbb2_mm_txdat	USBB2 data. Used as VP in 4-pin VP_VM mode.	IO	AF24 / AF11	-
usbb2_mm_txen	USBB2 transmit enable	IO	AC28 / AE11	-
Universal Serial Bus (USBC1)				
usbc1_icusb_dp	USBC1 interchip USB host D plus	IODS	H2 / AE5	-
usbc1_icusb_dm	USBC1 interchip USB host D minus	IODS	H3 / AF5	-
usbc1_icusb_txen	USBC1 transmit enable	O	D23 / AF4	-
usbc1_icusb_rcv	USBC1 receive	I	AE4	-

2.4.4 Removable Media Interfaces

2.4.4.1 MMC/SDIO

NOTE

For more information, see the MMC/SD/SDIO section of the OMAP4430 TRM.

Table 2-28. MMC/SDIO Signal Descriptions

SIGNAL NAME [1]	DESCRIPTION [2]	TYPE [3]	BALL BOTTOM [4]	BALL TOP [5]
Multimedia Memory Card / Secure Digital IO (SDMMC1)				
sdmmc1_clk	SDMMC1 clock	O	D25 / D2	-
sdmmc1_cmd	SDMMC1 command	IO	B22 / E3	-
sdmmc1_dat0	SDMMC1 data bit 0	IO	C16 / E4	-
sdmmc1_dat1	SDMMC1 data bit 1	IO	D16 / E2	-
sdmmc1_dat2	SDMMC1 data bit 2	IO	C17 / E1	-
sdmmc1_dat3	SDMMC1 data bit 3	IO	D17 / F4	-
sdmmc1_dat4	SDMMC1 data bit 4	IO	C18 / F3	-
sdmmc1_dat5	SDMMC1 data bit 5	IO	D18 / F1	-
sdmmc1_dat6	SDMMC1 data bit 6	IO	C19 / G4	-
sdmmc1_dat7	SDMMC1 data bit 7	IO	D19 / G3	-
Multimedia Memory Card / Secure Digital IO (SDMMC2)				
sdmmc2_clk	SDMMC2 clock	O	B11 / AE5	-
sdmmc2_cmd	SDMMC2 command	IO	B12 / AF5	-
sdmmc2_dat0	SDMMC2 data bit 0	IO	C12 / AE4	-
sdmmc2_dat1	SDMMC2 data bit 1	IO	D12 / AF4	-
sdmmc2_dat2	SDMMC2 data bit 2	IO	C13 / AG3	-
sdmmc2_dat3	SDMMC2 data bit 3	IO	D13 / AF3	-
sdmmc2_dat4	SDMMC2 data bit 4	IO	C15 / AD3	-
sdmmc2_dat5	SDMMC2 data bit 5	IO	D15 / AD4	-
sdmmc2_dat6	SDMMC2 data bit 6	IO	A16 / AC2	-
sdmmc2_dat7	SDMMC2 data bit 7	IO	B16 / AD2	-
sdmmc2_dir_cmd	SDMMC2 command direction signal to drive external level shifter	O	A16	-

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Table 2-28. MMC/SDIO Signal Descriptions (continued)

SIGNAL NAME [1]	DESCRIPTION [2]	TYPE [3]	BALL BOTTOM [4]	BALL TOP [5]
sdmmc2_dir_dat0	SDMMC2 data bit 0 direction signal to drive external level shifter	O	C15	-
sdmmc2_dir_dat1	SDMMC2 data bit 1/3 direction signal to drive external level shifter	O	D15	-
sdmmc2_clk_fdbk	SDMMC2 clock feedback if external loop back is needed	I	B16	-
Multimedia Memory Card / Secure Digital IO (SDMMC3)				
sdmmc3_clk	SDMMC3 clock	O	AB26 / AE9	-
sdmmc3_cmd	SDMMC3 command	IO	AB27 / AG10	-
sdmmc3_dat0	SDMMC3 data bit 0	IO	AA25 / AE10	-
sdmmc3_dat1	SDMMC3 data bit 1	IO	AA26 / AH11	-
sdmmc3_dat2	SDMMC3 data bit 2	IO	AB25 / AG11	-
sdmmc3_dat3	SDMMC3 data bit 3	IO	AC27 / AF10	-
Multimedia Memory Card / Secure Digital IO (SDMMC4)				
sdmmc4_clk	SDMMC4 clock	O	AE21 / AF12	-
sdmmc4_cmd	SDMMC4 command	IO	AF20 / AG12	-
sdmmc4_dat0	SDMMC4 data bit 0	IO	AF21 / AE12	-
sdmmc4_dat1	SDMMC4 data bit 1	IO	AH19 / AG13	-
sdmmc4_dat2	SDMMC4 data bit 2	IO	AG20 / AE11	-
sdmmc4_dat3	SDMMC4 data bit 3	IO	AE20 / AF11	-
Multimedia Memory Card / Secure Digital IO (SDMMC5)				
sdmmc5_clk	SDMMC5 clock	O	AE5	-
sdmmc5_cmd	SDMMC5 command	IO	AF5	-
sdmmc5_dat0	SDMMC5 data bit 0	IO	AE4	-
sdmmc5_dat1	SDMMC5 data bit 1	IO	AF4	-
sdmmc5_dat2	SDMMC5 data bit 2	IO	AG3	-
sdmmc5_dat3	SDMMC5 data bit 3	IO	AF3	-

2.4.4.2 USIM

Table 2-29. USIM Signal Descriptions

SIGNAL NAME [1]	DESCRIPTION [2]	TYPE [3]	BALL BOTTOM [4]	BALL TOP [5]
sim_io	SIM data	IO	H4	-
sim_clk	SIM clock	O	J2	-
sim_reset	SIM reset	O	G2	-
sim_cd	SIM card detect	I	J1	-
sim_pwrctrl	SIM power control	O	K1	-

2.4.5 Test Interfaces

2.4.5.1 JTAG

NOTE

For more information, see the On-Chip Debug Support / Debug Ports section of the OMAP4430 TRM.

Table 2-30. JTAG Signal Descriptions

SIGNAL NAME [1]	DESCRIPTION [2]	TYPE [3]	BALL BOTTOM [4]	BALL TOP [5]
jtag_ntrst	JTAG® test reset	I	AH2	-
jtag_tck	JTAG test clock	I	F4 / AG1	-
jtag_tms_tmsc	JTAG test mode select / compressed JTAG packet (CJTAG)	IO	E1 / AH1	-
jtag_rtck	JTAG ARM® clock emulation	O	AE3	-
jtag_tdi	JTAG test data input	I	AE1	-
jtag_tdo	JTAG test data output	O	AE2	-

2.4.5.2 DPM

NOTE

For more information, see the On-Chip Debug Support / Debug Ports section of the OMAP4430 TRM.

Table 2-31. DPM Signal Descriptions

SIGNAL NAME [1]	DESCRIPTION [2]	TYPE [3]	BALL BOTTOM [4]	BALL TOP [5]
dpm_emu0	Debug pin manager pin 0	IO	M2	-
dpm_emu1	Debug pin manager pin 1	IO	N2	-
dpm_emu2	Debug pin manager pin 2	O	P2	-
dpm_emu3	Debug pin manager pin 3	O	V1	-
dpm_emu4	Debug pin manager pin 4	O	V2	-
dpm_emu5	Debug pin manager pin 5	O	W1	-
dpm_emu6	Debug pin manager pin 6	O	W2	-
dpm_emu7	Debug pin manager pin 7	O	W3	-
dpm_emu8	Debug pin manager pin 8	O	W4	-
dpm_emu9	Debug pin manager pin 9	O	Y2	-
dpm_emu10	Debug pin manager pin 10	O	Y3	-
dpm_emu11	Debug pin manager pin 11	O	Y4	-
dpm_emu12	Debug pin manager pin 12	O	AA1	-
dpm_emu13	Debug pin manager pin 13	O	AA2	-
dpm_emu14	Debug pin manager pin 14	O	AA3	-
dpm_emu15	Debug pin manager pin 15	O	F4 / AA4	-
dpm_emu16	Debug pin manager pin 16	O	E1 / AB2	-
dpm_emu17	Debug pin manager pin 17	O	E2 / AB3	-
dpm_emu18	Debug pin manager pin 18	O	E4 / AF8 / AB4	-
dpm_emu19	Debug pin manager pin 19	O	D2 / AE8 / AC4	-

2.4.5.3 TPIU

NOTE

For more information, see the On-Chip Debug Support / Debug Ports section of the OMAP4430 TRM.

Table 2-32. TPIU 16-Bit Signal Descriptions

SIGNAL NAME [1]	PIN NAME [6]	DESCRIPTION [2]	TYPE [3]	BALL BOTTOM [4]	BALL TOP [5]
-	dpm_emu0	-	NA	M2	-

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Table 2-32. TPIU 16-Bit Signal Descriptions (continued)

SIGNAL NAME [1]	PIN NAME [6]	DESCRIPTION [2]	TYPE [3]	BALL BOTTOM [4]	BALL TOP [5]
-	dpm_emu1	-	NA	N2	-
atpiu_clk	dpm_emu2	TPIU ARM trace 16-bit clock	O	P2	-
atpiu_cntl	dpm_emu3	TPIU ARM trace 16-bit clock control	O	V1	-
atpiu_d0	dpm_emu4	TPIU ARM trace 16-bit data 0	O	V2	-
atpiu_d1	dpm_emu5	TPIU ARM trace 16-bit data 1	O	W1	-
atpiu_d2	dpm_emu6	TPIU ARM trace 16-bit data 2	O	W2	-
atpiu_d3	dpm_emu7	TPIU ARM trace 16-bit data 3	O	W3	-
atpiu_d4	dpm_emu8	TPIU ARM trace 16-bit data 4	O	W4	-
atpiu_d5	dpm_emu9	TPIU ARM trace 16-bit data 5	O	Y2	-
atpiu_d6	dpm_emu10	TPIU ARM trace 16-bit data 6	O	Y3	-
atpiu_d7	dpm_emu11	TPIU ARM trace 16-bit data 7	O	Y4	-
atpiu_d8	dpm_emu12	TPIU ARM trace 16-bit data 8	O	AA1	-
atpiu_d9	dpm_emu13	TPIU ARM trace 16-bit data 9	O	AA2	-
atpiu_d10	dpm_emu14	TPIU ARM trace 16-bit data 10	O	AA3	-
atpiu_d11	dpm_emu15	TPIU ARM trace 16-bit data 11	O	F4 / AA4	-
atpiu_d12	dpm_emu16	TPIU ARM trace 16-bit data 12	O	E1 / AB2	-
atpiu_d13	dpm_emu17	TPIU ARM trace 16-bit data 13	O	E2 / AB3	-
atpiu_d14	dpm_emu18	TPIU ARM trace 16-bit data 14	O	E4 / AF8 / AB4	-
atpiu_d15	dpm_emu19	TPIU ARM trace 16-bit data 15	O	D2 / AE8 / AC4	-

Table 2-33. TPIU 18-Bit Signal Descriptions

SIGNAL NAME [1]	PIN NAME [6]	DESCRIPTION [2]	TYPE [3]	BALL BOTTOM [4]	BALL TOP [5]
atpiu_d0	dpm_emu0	TPIU ARM trace 18-bit data 0	O	M2	-
atpiu_d1	dpm_emu1	TPIU ARM trace 18-bit data 1	O	N2	-
atpiu_clk	dpm_emu2	TPIU ARM trace 18-bit clock	O	P2	-
atpiu_cntl	dpm_emu3	TPIU ARM trace 18-bit clock control	O	V1	-
atpiu_d2	dpm_emu4	TPIU ARM trace 18-bit data 2	O	V2	-
atpiu_d3	dpm_emu5	TPIU ARM trace 18-bit data 3	O	W1	-
atpiu_d4	dpm_emu6	TPIU ARM trace 18-bit data 4	O	W2	-
atpiu_d5	dpm_emu7	TPIU ARM trace 18-bit data 5	O	W3	-
atpiu_d6	dpm_emu8	TPIU ARM trace 18-bit data 6	O	W4	-
atpiu_d7	dpm_emu9	TPIU ARM trace 18-bit data 7	O	Y2	-
atpiu_d8	dpm_emu10	TPIU ARM trace 18-bit data 8	O	Y3	-
atpiu_d9	dpm_emu11	TPIU ARM trace 18-bit data 9	O	Y4	-
atpiu_d10	dpm_emu12	TPIU ARM trace 18-bit data 10	O	AA1	-
atpiu_d11	dpm_emu13	TPIU ARM trace 18-bit data 11	O	AA2	-
atpiu_d12	dpm_emu14	TPIU ARM trace 18-bit data 12	O	AA3	-
atpiu_d13	dpm_emu15	TPIU ARM trace 18-bit data 13	O	F4 / AA4	-
atpiu_d14	dpm_emu16	TPIU ARM trace 18-bit data 14	O	E1 / AB2	-
atpiu_d15	dpm_emu17	TPIU ARM trace 18-bit data 15	O	E2 / AB3	-
atpiu_d16	dpm_emu18	TPIU ARM trace 18-bit data 16	O	E4 / AF8 / AB4	-
atpiu_d17	dpm_emu19	TPIU ARM trace 18-bit data 17	O	D2 / AE8 / AC4	-

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2.4.5.4 STM

NOTE

For more information, see the On-Chip Debug Support / Debug Ports section of the OMAP4430 TRM.

Table 2-34. STM Signal Descriptions

SIGNAL NAME [1]	PIN NAME [6]	DESCRIPTION [2]	TYPE [3]	BALL BOTTOM [4]	BALL TOP [5]
Option 1					
astm_d0	dpm_emu0	System trace data 0	IO	M2	-
astm_d1	dpm_emu1	System trace data 1	IO	N2	-
astm_clk	dpm_emu2	System trace clock	O	P2	-
astm_d2	dpm_emu3	System trace data 3	O	V1	-
astm_d3	dpm_emu4	System trace data 4	O	V2	-
Option 2					
astm_d3	dpm_emu15	System trace data 3	O	F4 / AA4	-
astm_d2	dpm_emu16	System trace data 2	O	E1 / AB2	-
astm_d1	dpm_emu17	System trace data 1	O	E2 / AB3	-
astm_d0	dpm_emu18	System trace data 0	O	E4 / AF8 / AB4	-
astm_clk	dpm_emu19	System trace clock	O	D2 / AE8 / AC4	-
Option 3					
astm_clk	dpm_emu1	System trace clock	IO	N2	-
astm_d0	dpm_emu0	System trace data 0	IO	M2	-

2.4.5.5 ATTILA

Table 2-35. ATTILA Signal Descriptions

SIGNAL NAME [1]	DESCRIPTION [2]	TYPE [3]	BALL BOTTOM [4]	BALL TOP [5]
attila_hw_dbg0	Attila hardware debug pin 0	O	M2	-
attila_hw_dbg1	Attila hardware debug pin 1	O	H4 / N2	-
attila_hw_dbg2	Attila hardware debug pin 2	O	J2 / P2	-
attila_hw_dbg3	Attila hardware debug pin 3	O	G2 / V1	-
attila_hw_dbg4	Attila hardware debug pin 4	O	J1 / V2	-
attila_hw_dbg5	Attila hardware debug pin 5	O	K1 / W1	-
attila_hw_dbg6	Attila hardware debug pin 6	O	AD2 / W2	-
attila_hw_dbg7	Attila hardware debug pin 7	O	AD3 / W3	-
attila_hw_dbg8	Attila hardware debug pin 8	O	AD4 / W4	-
attila_hw_dbg9	Attila hardware debug pin 9	O	AC2 / Y2	-
attila_hw_dbg10	Attila hardware debug pin 10	O	AC3 / Y3	-
attila_hw_dbg11	Attila hardware debug pin 11	O	AG6 / Y4	-
attila_hw_dbg12	Attila hardware debug pin 12	O	AF8 / AA1	-
attila_hw_dbg13	Attila hardware debug pin 13	O	AE8 / AA2	-
attila_hw_dbg14	Attila hardware debug pin 14	O	AA3	-
attila_hw_dbg15	Attila hardware debug pin 15	O	AA4	-
attila_hw_dbg16	Attila hardware debug pin 16	O	AB2	-
attila_hw_dbg17	Attila hardware debug pin 17	O	AB3	-
attila_hw_dbg18	Attila hardware debug pin 18	O	AB4	-
attila_hw_dbg19	Attila hardware debug pin 19	O	AC4	-

Table 2-35. ATTILA Signal Descriptions (continued)

SIGNAL NAME [1]	DESCRIPTION [2]	TYPE [3]	BALL BOTTOM [4]	BALL TOP [5]
attila_hw_dbg20	Attila hardware debug pin 20	O	AE18	-
attila_hw_dbg21	Attila hardware debug pin 21	O	AG19	-
attila_hw_dbg22	Attila hardware debug pin 22	O	AF19	-
attila_hw_dbg23	Attila hardware debug pin 23	O	AE19	-
attila_hw_dbg24	Attila hardware debug pin 24	O	AF18	-
attila_hw_dbg25	Attila hardware debug pin 25	O	AG18	-
attila_hw_dbg26	Attila hardware debug pin 26	O	AE17	-
attila_hw_dbg27	Attila hardware debug pin 27	O	AF17	-
attila_hw_dbg28	Attila hardware debug pin 28	O	AH17	-
attila_hw_dbg29	Attila hardware debug pin 29	O	AE16	-
attila_hw_dbg30	Attila hardware debug pin 30	O	AF16	-
attila_hw_dbg31	Attila hardware debug pin 31	O	AG16	-

2.4.5.6 Video Encoder Test

NOTE

For more information, see the Display Subsystem / Video Encoder section of the OMAP4430 TRM.

Table 2-36. Video Encoder Test Signal Descriptions

SIGNAL NAME [1]	DESCRIPTION [2]	TYPE [3]	BALL BOTTOM [4]	BALL TOP [5]
venc_656_data0	Video encoder display debug signal 0	I	B17	-
venc_656_data1	Video encoder display debug signal 1	I	A18	-
venc_656_data2	Video encoder display debug signal 2	I	B18	-
venc_656_data3	Video encoder display debug signal 3	I	A19	-
venc_656_data4	Video encoder display debug signal 4	I	B19	-
venc_656_data5	Video encoder display debug signal 5	I	B20	-
venc_656_data6	Video encoder display debug signal 6	I	A21	-
venc_656_data7	Video encoder display debug signal 7	I	B21	-

2.4.6 General-Purpose IOs

NOTE

For more information, see the General-Purpose Interface section of the OMAP4430 TRM.

Table 2-37. GPIO Signal Descriptions

SIGNAL NAME [1]	DESCRIPTION [2]	TYPE [3]	BALL BOTTOM [4]	BALL TOP [5]
gpio_wk0	General-purpose IO 0, Bank1, always GPIO	IO	H4	-
gpio_0	General-purpose IO 0, Bank1	IO	J27	-
gpio_wk1	General-purpose IO 1, Bank1, always GPIO	IO	J2	-
gpio_1	General-purpose IO 1, Bank1	IO	H27	-
gpio_wk2	General-purpose IO 2, Bank1, always GPIO	IO	G2	-
gpio_2	General-purpose IO 2, Bank1	IO	L27	-
gpio_wk3	General-purpose IO 3, Bank1, always GPIO	IO	J1	-
gpio_3	General-purpose IO 3, Bank1	IO	K27	-

Table 2-37. GPIO Signal Descriptions (continued)

SIGNAL NAME [1]	DESCRIPTION [2]	TYPE [3]	BALL BOTTOM [4]	BALL TOP [5]
gpio_wk4	General-purpose IO 4, Bank1, always GPIO	IO	K1	-
gpio_wk6	General-purpose IO 5, Bank1, always GPIO	IO	AD2	-
gpio_wk7	General-purpose IO 6, Bank1, always GPIO	IO	AC2	-
gpio_wk8	General-purpose IO 7, Bank1, always GPIO	IO	AC3	-
gpio_wk9	General-purpose IO 8, Bank1, always GPIO	IO	AF8	-
gpio_wk10	General-purpose IO 9, Bank1, always GPIO	IO	AE8	-
gpio_11	General-purpose IO 11, Bank1	IO	M2	-
gpio_12	General-purpose IO 12, Bank1	IO	N2	-
gpio_13	General-purpose IO 13, Bank1	IO	P2	-
gpio_14	General-purpose IO 14, Bank1	IO	V1	-
gpio_15	General-purpose IO 15, Bank1	IO	V2	-
gpio_16	General-purpose IO 16, Bank1	IO	W1	-
gpio_17	General-purpose IO 17, Bank1	IO	W2	-
gpio_18	General-purpose IO 18, Bank1	IO	W3	-
gpio_19	General-purpose IO 19, Bank1	IO	W4	-
gpio_20	General-purpose IO 20, Bank1	IO	Y2	-
gpio_21	General-purpose IO 21, Bank1	IO	Y3	-
gpio_22	General-purpose IO 22, Bank1	IO	Y4	-
gpio_23	General-purpose IO 23, Bank1	IO	AA1	-
gpio_24	General-purpose IO 24, Bank1	IO	AA2	-
gpio_25	General-purpose IO 25, Bank1	IO	AA3	-
gpio_26	General-purpose IO 26, Bank1	IO	AA4	-
gpio_27	General-purpose IO 27, Bank1	IO	AB2	-
gpio_28	General-purpose IO 28, Bank1	IO	AB3	-
gpio_wk29	General-purpose IO 29, Bank1, always GPIO	IO	AG6	-
gpio_wk30	General-purpose IO 30, Bank1, always GPIO	IO	AD3	-
gpio_wk31	General-purpose IO 31, Bank1, always GPIO	IO	AD4	-
gpio_32	General-purpose IO 32	IO	C16	-
gpio_33	General-purpose IO 33	IO	D16	-
gpio_34	General-purpose IO 34	IO	C17	-
gpio_35	General-purpose IO 35	IO	D17	-
gpio_36	General-purpose IO 36	IO	C18	-
gpio_37	General-purpose IO 37	IO	D18	-
gpio_38	General-purpose IO 38	IO	C19	-
gpio_39	General-purpose IO 39	IO	D19	-
gpio_40	General-purpose IO 40	IO	B17	-
gpio_41	General-purpose IO 41	IO	A18	-
gpio_42	General-purpose IO 42	IO	B18	-
gpio_43	General-purpose IO 43	IO	A19	-
gpio_44	General-purpose IO 44	IO	B19	-
gpio_45	General-purpose IO 45	IO	B20	-
gpio_46	General-purpose IO 46	IO	A21	-
gpio_47	General-purpose IO 47	IO	B21	-
gpio_48	General-purpose IO 48	IO	C20	-
gpio_49	General-purpose IO 49	IO	D20	-
gpio_50	General-purpose IO 50	IO	B25	-
gpio_51	General-purpose IO 51	IO	C21	-

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Table 2-37. GPIO Signal Descriptions (continued)

SIGNAL NAME [1]	DESCRIPTION [2]	TYPE [3]	BALL BOTTOM [4]	BALL TOP [5]
gpio_52	General-purpose IO 52	IO	D21	-
gpio_53	General-purpose IO 53	IO	C22	-
gpio_54	General-purpose IO 54	IO	C25	-
gpio_55	General-purpose IO 55	IO	B22	-
gpio_56	General-purpose IO 56	IO	D25	-
gpio_59	General-purpose IO 59	IO	C23	-
gpio_60	General-purpose IO 60	IO	D22	-
gpio_61	General-purpose IO 61	IO	B26	-
gpio_62	General-purpose IO 62	IO	B23	-
gpio_63	General-purpose IO 63	IO	B9	-
gpio_64	General-purpose IO 64	IO	B10	-
gpio_65	General-purpose IO 65	IO	A8	-
gpio_66	General-purpose IO 66	IO	B8	-
gpio_81	General-purpose IO 81	IO	T27	-
gpio_82	General-purpose IO 82	IO	U27	-
gpio_83	General-purpose IO 83	IO	V27	-
gpio_84	General-purpose IO 84	IO	AE18	-
gpio_85	General-purpose IO 85	IO	AG19	-
gpio_86	General-purpose IO 86	IO	AF19	-
gpio_87	General-purpose IO 87	IO	AE19	-
gpio_88	General-purpose IO 88	IO	AF18	-
gpio_89	General-purpose IO 89	IO	AG18	-
gpio_90	General-purpose IO 90	IO	AE17	-
gpio_91	General-purpose IO 91	IO	AF17	-
gpio_92	General-purpose IO 92	IO	AH17	-
gpio_93	General-purpose IO 93	IO	AE16	-
gpio_94	General-purpose IO 94	IO	AF16	-
gpio_95	General-purpose IO 95	IO	AG16	-
gpio_96	General-purpose IO 96	IO	AF14	-
gpio_97	General-purpose IO 97	IO	AE14	-
gpio_98	General-purpose IO 98	IO	H2	-
gpio_99	General-purpose IO 99	IO	H3	-
gpio_100	General-purpose IO 100	IO	D23 / D2	-
gpio_101	General-purpose IO 101	IO	A24 / E3	-
gpio_102	General-purpose IO 102	IO	B24 / E4	-
gpio_103	General-purpose IO 103	IO	C24 / E2	-
gpio_104	General-purpose IO 104	IO	D24 / E1	-
gpio_105	General-purpose IO 105	IO	F4	-
gpio_106	General-purpose IO 106	IO	F3	-
gpio_107	General-purpose IO 107	IO	F1	-
gpio_108	General-purpose IO 108	IO	G4	-
gpio_109	General-purpose IO 109	IO	G3	-
gpio_110	General-purpose IO 110	IO	AD27	-
gpio_111	General-purpose IO 111	IO	AD26	-
gpio_112	General-purpose IO 112	IO	AD25	-
gpio_113	General-purpose IO 113	IO	AC28	-
gpio_114	General-purpose IO 114	IO	AC26	-

Table 2-37. GPIO Signal Descriptions (continued)

SIGNAL NAME [1]	DESCRIPTION [2]	TYPE [3]	BALL BOTTOM [4]	BALL TOP [5]
gpio_115	General-purpose IO 115	IO	AC25	-
gpio_116	General-purpose IO 116	IO	AB25	-
gpio_117	General-purpose IO 117	IO	AC27	-
gpio_118	General-purpose IO 118	IO	AH26	-
gpio_119	General-purpose IO 119	IO	AE24	-
gpio_120	General-purpose IO 120	IO	AF24	-
gpio_121	General-purpose IO 121	IO	AG24	-
gpio_122	General-purpose IO 122	IO	AH24	-
gpio_123	General-purpose IO 123	IO	AB26	-
gpio_124	General-purpose IO 124	IO	AB27	-
gpio_125	General-purpose IO 125	IO	AA25	-
gpio_126	General-purpose IO 126	IO	AA26	-
gpio_127	General-purpose IO 127	IOD	AA27	-
gpio_128	General-purpose IO 128	IO	C26	-
gpio_129	General-purpose IO 129	IO	D26	-
gpio_130	General-purpose IO 130	IO	W27	-
gpio_131	General-purpose IO 131	IO	Y27	-
gpio_132	General-purpose IO 132	IO	AG21	-
gpio_133	General-purpose IO 133	IO	AH22	-
gpio_134	General-purpose IO 134	IO	AF22	-
gpio_135	General-purpose IO 135	IO	AE22	-
gpio_136	General-purpose IO 136	IO	AG22	-
gpio_137	General-purpose IO 137	IO	AE23	-
gpio_138	General-purpose IO 138	IO	AF23	-
gpio_139	General-purpose IO 139	IO	AG23	-
gpio_140	General-purpose IO 140	IO	AH23	-
gpio_141	General-purpose IO 141	IO	F27	-
gpio_142	General-purpose IO 142	IO	F28	-
gpio_143	General-purpose IO 143	IO	G27	-
gpio_144	General-purpose IO 144	IO	G28	-
gpio_145	General-purpose IO 145	IO	AE5	-
gpio_146	General-purpose IO 146	IO	AF5	-
gpio_147	General-purpose IO 147	IO	AE4	-
gpio_148	General-purpose IO 148	IO	AF4	-
gpio_149	General-purpose IO 149	IO	AG3	-
gpio_150	General-purpose IO 150	IO	AF3	-
gpio_151	General-purpose IO 151	IO	AE21	-
gpio_152	General-purpose IO 152	IO	AF20	-
gpio_153	General-purpose IO 153	IO	AF21	-
gpio_154	General-purpose IO 154	IO	AE20	-
gpio_155	General-purpose IO 155	IO	AG20	-
gpio_156	General-purpose IO 156	IO	AH19	-
gpio_157	General-purpose IO 157	IO	AG12	-
gpio_158	General-purpose IO 158	IO	AF12	-
gpio_159	General-purpose IO 159	IO	AE12	-
gpio_160	General-purpose IO 160	IO	AG13	-
gpio_161	General-purpose IO 161	IO	AE11	-

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Table 2-37. GPIO Signal Descriptions (continued)

SIGNAL NAME [1]	DESCRIPTION [2]	TYPE [3]	BALL BOTTOM [4]	BALL TOP [5]
gpio_162	General-purpose IO 162	IO	AF11	-
gpio_163	General-purpose IO 163	IO	AG11	-
gpio_164	General-purpose IO 164	IO	AH11	-
gpio_165	General-purpose IO 165	IO	AE10	-
gpio_166	General-purpose IO 166	IO	AF10	-
gpio_167	General-purpose IO 167	IO	AG10	-
gpio_168	General-purpose IO 168	IO	AE9	-
gpio_169	General-purpose IO 169	IO	AF13	-
gpio_170	General-purpose IO 170	IO	AE13	-
gpio_171	General-purpose IO 171	IO	G26	-
gpio_172	General-purpose IO 172	IO	G25	-
gpio_173	General-purpose IO 173	IO	H26	-
gpio_174	General-purpose IO 174	IO	H25	-
gpio_175	General-purpose IO 175	IO	J26	-
gpio_176	General-purpose IO 176	IO	J25	-
gpio_177	General-purpose IO 177	IO	K26	-
gpio_178	General-purpose IO 178	IO	K25	-
gpio_181	General-purpose IO 181	IO	AA28	-
gpio_182	General-purpose IO 182	IO	Y28	-
gpio_183	General-purpose IO 183	IO	AF6	-
gpio_184	General-purpose IO 184	IO	F26	-
gpio_185	General-purpose IO 185	IO	E27	-
gpio_186	General-purpose IO 186	IO	E26	-
gpio_187	General-purpose IO 187	IO	E25	-
gpio_188	General-purpose IO 188	IO	D28	-
gpio_189	General-purpose IO 189	IO	D27	-
gpio_190	General-purpose IO 190	IO	AB4	-
gpio_191	General-purpose IO 191	IO	AC4	-

2.4.7 General-Purpose In

NOTE

For more information, see the General-Purpose Interface section of the OMAP4430 TRM.

Table 2-38. GPIN Signal Descriptions

SIGNAL NAME [1]	DESCRIPTION [2]	TYPE [3]	BALL BOTTOM [4]	BALL TOP [5]
gpi_wk5	General-purpose In 5, Bank1, always GPIN	I	AG8	-
gpi_67	General-purpose In 67	I	R26	-
gpi_68	General-purpose In 68	I	R25	-
gpi_69	General-purpose In 69	I	T26	-
gpi_70	General-purpose In 70	I	T25	-
gpi_71	General-purpose In 71	I	U26	-
gpi_72	General-purpose In 72	I	U25	-
gpi_73	General-purpose In 73	I	V26	-
gpi_74	General-purpose In 74	I	V25	-
gpi_75	General-purpose In 75	I	W26	-

Table 2-38. GPIN Signal Descriptions (continued)

SIGNAL NAME [1]	DESCRIPTION [2]	TYPE [3]	BALL BOTTOM [4]	BALL TOP [5]
gpi_76	General-purpose In 76	I	W25	-
gpi_77	General-purpose In 77	I	M26	-
gpi_78	General-purpose In 78	I	M25	-
gpi_79	General-purpose In 79	I	N26	-
gpi_80	General-purpose In 80	I	N25	-

2.4.8 System and Miscellaneous

2.4.8.1 DM Timer

NOTE

For more information, see the Timers section of the OMAP4430 TRM.

Table 2-39. DM Timer Signal Descriptions

SIGNAL NAME [1]	DESCRIPTION [2]	TYPE [3]	BALL BOTTOM [4]	BALL TOP [5]
dmtimer8_pwm_evt	DM timer event input or PWM output	IO	AH17 / G27 / AB2	-
dmtimer9_pwm_evt	DM timer event input or PWM output	IO	AE16 / AH24 / G28 / AB3	-
dmtimer10_pwm_evt	DM timer event input or PWM output	IO	AF16 / AB4	-
dmtimer11_pwm_evt	DM timer event input or PWM output	IO	AG16 / AG24 / AC4	-

2.4.8.2 KeyPad

NOTE

For more information, see Keyboard Controller / Keyboard Controller Environment section of the OMAP4430 TRM.

Table 2-40. Keypad Signal Descriptions

SIGNAL NAME [1]	DESCRIPTION [2]	TYPE [3]	BALL BOTTOM [4]	BALL TOP [5]
kpd_row0	Keypad row 0	I	C16 / J26 / K25	-
kpd_row1	Keypad row 1	I	D16 / J25 / L27	-
kpd_row2	Keypad row 2	I	C17 / K26 / K27	-
kpd_row3	Keypad row 3	I	D17 / J26 / K25	-
kpd_row4	Keypad row 4	I	B17 / J25 / L27	-
kpd_row5	Keypad row 5	I	A18 / K26 / K27	-
kpd_row6	Keypad row 6	I	B18 / AF21	-
kpd_row7	Keypad row 7	I	A19 / AE20	-
kpd_row8	Keypad row 8	I	D21 / AG20	-
kpd_col0	Keypad column 0	OD	C18 / G26 / H25	-
kpd_col1	Keypad column 1	OD	D18 / G25 / J27	-
kpd_col2	Keypad column 2	OD	C19 / H26 / H27	-
kpd_col3	Keypad column 3	OD	D19 / G26 / H25	-
kpd_col4	Keypad column 4	OD	B19 / G25 / J27	-
kpd_col5	Keypad column 5	OD	B20 / H26 / H27	-
kpd_col6	Keypad column 6	OD	A21 / AE21	-
kpd_col7	Keypad column 7	OD	B21 / AF20	-

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Table 2-40. Keypad Signal Descriptions (continued)

SIGNAL NAME [1]	DESCRIPTION [2]	TYPE [3]	BALL BOTTOM [4]	BALL TOP [5]
kpd_col8	Keypad column 8	OD	C20 / AH19	-

2.4.8.3 POP

NOTE

For more information, see Package-On-Package Concept section of the OMAP4430 TRM.

Table 2-41. POP Signal Descriptions

SIGNAL NAME [1]	DESCRIPTION [2]	TYPE [3]	BALL BOTTOM [4]	BALL TOP [5]
pop_lpddr21_zq	Feedthrough to top lpddr21 ZQ pin	FEED	AH16	AJ17
pop_lpddr22_zq	Feedthrough to top lpddr22 ZQ pin	FEED	AF28	AG29
pop_vacc_lpddr2	Feedthrough to top lpddr21and lpddr22 vacc power supply	PWR	A26 / B2	B2 / B28
pop_vdd1_lpddr2_ shared	Feedthrough to shared top lpddr21 vand lpddr22 dd1 power supply	PWR	AG27 / C1 / AG2	C1 / AH2 / AH28
pop_vdd1_lpddr21	Feedthrough to top lpddr21 vdd1 power supply	PWR	A13 / C27 / AH14	A15 / C28 / AJ15
pop_vdd1_lpddr22	Feedthrough to top lpddr22 vdd2 power supply	PWR	N1 / P1 / R28	N2 / P29 / R1
pop_vdd2_lpddr2_ shared	Feedthrough to shared top lpddr21 and lpddr22 vdd2 power supply	PWR	AH3 / A3 / C28 / AF27	A3 / C29 / AG28 / AH3
pop_vdd2_lpddr21	Feedthrough to top lpddr21 vdd2 power supply	PWR	AG14 / A15 / B15	A16 / B16 / AH15
pop_vdd2_lpddr22	Feedthrough to top lpddr22 vdd2 power supply	PWR	T1 / T2 / N28	P28 / T1 / T2

2.4.8.4 System And Miscellaneous

NOTE

For more information, see:

- Power, Reset and Clock Management / PRCM Subsystem Environment / External Clock Signals section, or
- Power, Reset and Clock Management / PRCM Subsystem Environment / External Reset Signals section, or
- Power, Reset and Clock Management / PRCM Subsystem Environment / External Power Control Signals section

of the OMAP4430 TRM.

Table 2-42. System and Miscellaneous Signal Descriptions

SIGNAL NAME [1]	DESCRIPTION [2]	TYPE [3]	BALL BOTTOM [4]	BALL TOP [5]
sys_32k	32-kHz clock input	I	AG7	-
sys_nrespwron	Global cold reset input	I	AE7	-
sys_nreswarm	Global warm reset input/output	IOD	AF7	-
sys_nirq1	External interrupt (aimed at TWL6030 PMIC power device connection)	I	AE6	-
sys_nirq2	External interrupt (aimed at TWL6030 PMIC power device connection)	I	AF6	-
sys_pwr_req	Power request to exit off mode. Active high by default but configurable	O	AH7	-
sys_pwron_reset_out	Peripheral power on reset output	O	AG6	-
sys_drm_msecure	Secure mode output	O	AD2 / AD3 / AA3	-
sys_secure_indicator	Secure mode indicator	O	AD4 / AA4	-

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Table 2-42. System and Miscellaneous Signal Descriptions (continued)

SIGNAL NAME [1]	DESCRIPTION [2]	TYPE [3]	BALL BOTTOM [4]	BALL TOP [5]
sys_boot0	System boot configration pin0	I	F26	-
sys_boot1	System boot configration pin1	I	E27	-
sys_boot2	System boot configration pin2	I	E26	-
sys_boot3	System boot configration pin3	I	E25	-
sys_boot4	System boot configration pin4	I	D28	-
sys_boot5	System boot configration pin5	I	D27	-
sys_boot6	System boot configration pin6	I	AF8	-
sys_boot7	System boot configration pin7	I	AE8	-
sys_ndmareq0	External DMA request 0	I	B25 / D23	-
sys_ndmareq1	External DMA request 1	I	C25 / A24	-
sys_ndmareq2	External DMA request 2	I	B22 / B24	-
sys_ndmareq3	External DMA request 3	I	D25 / C24	-
fref_xtal_in	FREF oscillator cell drive pad input or alternate clock square input	AI-I	AH6	-
fref_xtal_out	FREF oscillator cell drive pad output	AO	AH5	-
fref_xtal_vssosc	FREF oscillator kelvin ground	na	AG5	-
fref_slicer_in	FREF main clock input to slicer or alternate clock input to internal peripheral	AI-I	AG8	-
fref_clk_ioreq	FREF input (sysboot[67] = 00) or output (sysboot[67] = 01, 10, 11) clock request for main clock	IO	AD1	-
fref_clk0_out	FREF clock 0 output	O	AD2	-
fref_clk1_out	FREF clock 1 output	O	AA28	-
fref_clk2_out	FREF clock 2 output	O	Y28	-
fref_clk3_out	FREF clock 3 output	O	AD4	-
fref_clk4_out	FREF clock 4 output. Active by default	O	AC3	-
fref_clk5_out	FREF clock 5 output	O	AC2	-
fref_clk1_req	FREF clock request 1	I	AD2 / AD3	-
fref_clk2_req	FREF clock request 2	I	AD4	-
fref_clk3_req	FREF clock request 3	I	AD3	-
fref_clk4_req	FREF clock request 4	I	AC2	-
abe_clks	ABE clock input	I	AH26	-
atestv(1)	Reserved	AO	A27	-
vsense(1)	Reserved	AO	AG28	-
iforce(1)	Reserved	AI	AH27	-

(1) atestv, iforce, and vsense pins must be left unconnected.
The following bottom balls are reserved: C4 / C5 / C6 / D3 / D4 / D5 / D6 / L22 / N7. These balls must be left unconnected.

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2.4.9 Power Supplies

NOTE

For more information, see Power, Reset and Clock Management / PRCM Subsystem Environment / External Voltage Inputs section of the OMAP4430 TRM.

Table 2-43. Power Supplies Signal Descriptions

SIGNAL NAME [1]	DESCRIPTION [2]	TYPE [3]	BALL BOTTOM [4]	BALL TOP [5]
vss	Main and slicer ground	GND	H1 / M1 / AB1 / C2 / F2 / K2 / U2 / AF2 / B3 / J3 / J4 / AG4 / B6 / K8 / U8 / AH8 / N9 / A10 / AH10 / H11 / AA11 / N12 / P12 / R12 / T12 / U12 / AA12 / B13 / H13 / M13 / N13 / P13 / R13 / T13 / U13 / AH13 / M14 / N14 / P14 / R14 / T14 / U14 / M15 / N15 / P15 / R15 / T15 / U15 / M16 / N16 / P16 / R16 / T16 / U16 / H17 / M17 / N17 / P17 / R17 / T17 / U17 / Y17 / AG17 / H19 / A20 / AA20 / J21 / L21 / M21 / U21 / AH21 / M22 / A23 / F25 / L25 / Y25 / L26 / Y26 / AG26 / B27 / AE27 / H28 / K28 / U28	A2 / A6 / A9 / A11 / A14 / A28 / B1 / B14 / B21 / B24 / B29 / E28 / F1 / H28 / J1 / L29 / M2 / P1 / P2 / R28 / V2 / V28 / AA28 / AB2 / AE2 / AF28 / AH1 / AH5 / AH14 / AH18 / AH29 / AJ2 / AJ7 / AJ11 / AJ16 / AJ22 / AJ28
vpp(1)	eFuse power supply	PWR	Y22	-
vpp_cust(1)	Customer eFuse power supply	PWR	J8	-
vdd_core	Core and oscillator power supply	PWR	J9 / K9 / L9 / M9 / T9 / J10 / J11 / Y11 / H12 / J12 / Y12 / J13 / Y13 / AA13 / J15 / J16 / J17 / H18 / J18 / J19 / J20 / K20 / L20 / M20 / N20 / R20 / T20 / U20 / V20	-
vdd_mpu	MPU power supply	PWR	V8 / W8 / Y8 / U9 / V9 / W9 / Y9 / Y10 / AA10	-
vdd_iva_audio	IVA and audio BE power supply	PWR	AA17 / Y18 / AA18 / Y19 / AA19 / W20 / Y20 / V21 / W21 / Y21	-
vdds_1p2v	1.2-V IO power supply	PWR	AA16	-
vdds_1p8v	1.8-V IO power supply	PWR	AB7 / U7 / V7 / K7 / H22 / J22 / W22	
vdds_1p8_fref	1.8-V FREF IO power supply	PWR	Y7	-
vddq_lpddr2	LPDDR2 dm / dqs / ndqs—0/2 and 1/3 IOs power supply	PWR	D1 / G1 / U1 / Y1 / AC1 / AF1 / A4 / AH4 / A6 / L7 / G8 / H8 / L8 / M8 / AA8 / A9 / H9 / AA9 / AB9 / AH9 / A12 / AH12 / A17 / H20 / G21 / H21 / A22 / A25 / E28 / J28 / L28	A22 / B4 / B7 / B9 / B13 / B18 / B25 / D2 / D29 / F29 / G2 / J2 / J28 / M28 / U1 / Y1 / AC1 / AF2 / AH9 / AH12 / AJ4 / AJ6
vddq_vref_lpddr2	LPDDR2 DQ VREF power supply: Channel 1 on ball G15 Channel 2 on ball T8	PWR	G15 / T8	-
vddca_lpddr2	LPDDR2 CA / clk / clk enable / chip select IO power supply	PWR	AH18 / AH20 / AA21 / AB21 / AA22 / AB22 / AH25 / T28 / AB28 / AD28	T28 / AC28 / AE29 / AH22 / AJ19 / AJ26
vddca_vref_lpddr2	LPDDR2 CA VREF power supply: Channel 1 on ball Y14 Channel 2 on ball R27	PWR	Y14 / R27	-
lpddr2_vref_ca	LPDDR2 CA VREF output power supply to memory: Channel 1 on ball AH16 Channel 2 on ball U28	PWR	-	AH16 / U28
lpddr2_vref_dq	LPDDR2 DQ VREF output power supply to memory: Channel 1 on ball B15 Channel 2 on ball R2	PWR	-	B15 / R2

Table 2-43. Power Supplies Signal Descriptions (continued)

SIGNAL NAME [1]	DESCRIPTION [2]	TYPE [3]	BALL BOTTOM [4]	BALL TOP [5]
vdda_dll0_lpddr21	LPDDR21 DLL power supply providing clocks to byte 0 and 2	PWR	G22	-
vdda_dll1_lpddr21	LPDDR21 DLL power supply providing clocks to byte 1 and 3	PWR	G9	-
vdda_dll0_lpddr22	LPDDR22 DLL power supply providing clocks to byte 0 and 2	PWR	M7	-
vdda_dll1_lpddr22	LPDDR22 DLL power supply providing clocks to byte 1 and 3	PWR	AB10	-
vdda_dsi1	DSI1 PHY power supply	PWR	L1	-
vssa_dsi	DSI1 and DSI2 PHY ground	GND	N8 / P8	-
vdda_dsi2	DSI2 PHY power supply	PWR	L2	-
vdda_csi21	CSI21 PHY power supply	PWR	W28	-
vssa_csi2	CSI21 and CSI22 PHY ground	GND	R22	-
vdda_csi22	CSI22 PHY power supply	PWR	V28	-
vdda_hdmi_vdac	HDMI PHY and VDAC PHY power supply	PWR	A11 / G12	-
vssa_hdmi_vdac	HDMI and VDAC PHY ground	GND	G11	-
vdda_usba0otg_3p3v	USB PHY 3.3-V power supply	PWR	A5	-
vssa_usba0otg_3p3v	USB PHY 3.3-V ground	GND	G10	-
vdda_usba0otg_1p8v	USB PHY 1.8-V power supply	PWR	A7	-
vssa_usba0otg	USB PHY 1.8-V ground	GND	H10	-
vdds_usim	SIM dual voltage IO power supply	PWR	J7	-
pbias_sim	SIM pbias output	PWR	A2	
vdds_sdmmc1	SDMMC1 dual voltage IO power supply	PWR	G7 / H7	-
pbias_mmc1	SDMMC1 pbias output	PWR	A1	
vdda_dpll_mpu	MPU DPLL power supply	PWR	P9	-
vdda_dpll_core_audio	Core and audio DPLLs power supply	PWR	G13	-
vdda_dpll_iva_per	Peripheral and IVA DPLL power supply	PWR	Y16	-
vdds_dv_gpmc	GPMC dual voltage IO power supply	PWR	G20	-
vdds_dv_sdmmc2	SDMMC2 dual voltage IO power supply	PWR	G16 / H16	-
vdds_dv_c2c	GPMC second dual voltage power supply	PWR	G17 / G18 / G19	-
vdds_dv_cam	Camera dual voltage IO power supply	PWR	V22	-
vdds_dv_bank0	Serial bank0 dual voltage IO power supply	PWR	AB16	-
vdds_dv_bank1	Serial bank1 dual voltage IO power supply	PWR	AB20	-
vdds_dv_bank2	Serial bank2 dual voltage IO power supply	PWR	AB8 / AB19	-

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Table 2-43. Power Supplies Signal Descriptions (continued)

SIGNAL NAME [1]	DESCRIPTION [2]	TYPE [3]	BALL BOTTOM [4]	BALL TOP [5]
vdds_dv_bank3	Serial bank3 dual voltage IO power supply	PWR	AB18	-
vdds_dv_bank4	Serial bank4 dual voltage IO power supply	PWR	AA7	-
vdds_dv_bank5	Serial bank5 dual voltage IO power supply	PWR	AB17	-
vdds_dv_bank6	Serial bank6 dual voltage IO power supply	PWR	AA14	-
vdds_dv_bank7	Serial bank7 dual voltage IO power supply	PWR	M28	-
vdds_dv_fref	FREF dual voltage IO power supply	PWR	W7	-
vdda_ldo_sram_mpu	MPU SRAM LDO power supply	PWR	AB14	-
vdda_ldo_sram_iva_audio	IVA SRAM LDO power supply	PWR	N22	-
vdda_ldo_sram_core	Core SRAM LDO power supply	PWR	T22	-
vdda_ldo_emu_wkup	Wake-up / emulation and WKUP EMU Array LDOs power supply	PWR	P7	-
vdda_bdgp_vbb	Bandgap, MPU and IVA VBB LDOs supply input	PWR	AB12	-
cap_vbb_ldo_mpu	MPU VBB LDO output	PWR	AB13	-
cap_vbb_ldo_iva_audio	Audio VBB LDO output	PWR	R21	-
cap_vdd_ldo_sram_mpu	MPU SRAM LDO output	PWR	AB11	-
cap_vdd_ldo_sram_iva_audio	IVA SRAM LDO output	PWR	N21	-
cap_vdd_ldo_sram_core	Core SRAM LDO output	PWR	U22	-
cap_vdd_ldo_emu_wkup	Wake-Up LDO output	PWR	T7	-

(1) vpp must be unconnected. vpp_cust is only powered when programming CPFROM eFuses. Otherwise, it is recommended to leave vpp_cust turned off (floating). Note that if the TWL6030 PMIC is used then the vpp pull-down resistor inside the TWL6030 must be disabled when the vpp_cust is turned off.

3 Electrical Characteristics

NOTE

For more information, see Power, Reset and Clock Management / PRCM Subsystem Environment / External Voltage Inputs or Initialization / Preinitialization / Power Requirements section of the OMAP4430 TRM.

3.1 Absolute Maximum Ratings

Stresses beyond those listed as absolute maximum ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those listed under Section 3.2, *Recommended Operating Conditions*, is not implied. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.

Table 3-1. Absolute Maximum Ratings Over Junction Temperature Range

PARAMETER		MIN	MAX	UNIT
vdd_mpu	Supply voltage for ARM MPU domain	–0.5	1.50	V
vdd_iva_audio	Supply voltage for IVA3 and audio BE domain	–0.5	1.50	V
vdd_core	Supply voltage for OMAP core domain	–0.5	1.50	V
vpp[(4)]	Supply for eFuse programming	–0.5	2.20	V
vpp_cust[(4)]	Supply for customer eFuse programming	–0.5	2.20	V
I_{vpp}[(4)]	Peak vpp current for eFuse programming	0.05	50	mA
vdda_dll0_lpddr21	Supply voltage for LPDDR21 DLL providing clocks to byte 0 and 2	–0.5	2.10	V
vdda_dll1_lpddr21	Supply voltage for LPDDR21 DLL providing clocks to byte 1 and 3	–0.5	2.10	V
vdda_dll0_lpddr22	Supply voltage for LPDDR22 DLL providing clocks to byte 0 and 2	–0.5	2.10	V
vdda_dll1_lpddr22	Supply voltage for LPDDR22 DLL providing clocks to byte 1 and 3	–0.5	2.10	V
vdda_dpll_mpu	Supply voltage for MPU DPLLs	–0.5	2.10	V
vdda_dpll_core_audio	Supply voltage for core and audio DPLLs	–0.5	2.10	V
vdda_dpll_iva_per	Supply voltage for IVA and peripherals DPLLs	–0.5	2.10	V
vdda_csi21	Supply voltage for CSI21 PHY buffer	–0.5	2.10	V
vdda_csi22	Supply voltage for CSI22 PHY buffer	–0.5	2.10	V
vdda_dsi1	Supply voltage for DSI1 PHY buffer	–0.5	2.10	V
vdda_dsi2	Supply voltage for DSI2 PHY buffer	–0.5	2.10	V
vdda_ldo_sram_mpu	Supply voltage for MPU SRAM LDO	–0.5	2.10	V
vdda_ldo_sram_iva_audio	Supply voltage for IVA and audio SRAM LDO	–0.5	2.10	V
vdda_ldo_sram_core	Supply voltage for core SRAM LDO	–0.5	2.10	V
vdda_ldo_emu_wkup	Supply voltage for wake-up / emulation LDO	–0.5	2.10	V
vdda_bdgp_vbb	Supply voltage for bandgap	–0.5	2.10	V
vdda_hdmi_vdac	Supply voltage for HDMI PHY buffers and video DAC	–0.5	2.10	V
vdda_usba0otg_3p3v	Supply voltage for USB PHY 3.3-V buffers	–0.5	4.00	V
vdda_usba0otg_1p8v	Supply voltage for USB PHY 1.8-V buffers	–0.5	2.10	V
vdds_1p2v	Supply voltage for 1.2-V I/O macros	–0.5	1.50	V
vdds_1p8v	Supply voltage for 1.8-V I/O macros	–0.5	2.10	V
vdds_1p8_fref	Supply voltage for 1.8-V FREF I/O macros	–0.5	2.10	V
vdds_dv_gpmc	Supply voltage for GPMC dual voltage IOs	–0.5	2.10	V
vdds_sdmmc1	Supply voltage for SDMMC1 dual voltage IOs	–0.5	3.80	V
vdds_dv_sdmmc2	Supply voltage for SDMMC2 dual voltage IOs	–0.5	2.10	V
vdds_dv_c2c	Supply voltage for GPMC second dual voltage IOs	–0.5	2.10	V
vdds_dv_cam	Supply voltage for camera dual voltage IOs	–0.5	2.10	V
vdds_dv_bank0	Supply voltage for serial interface bank0 dual voltage IOs	–0.5	2.10	V

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Table 3-1. Absolute Maximum Ratings Over Junction Temperature Range (continued)

PARAMETER			MIN	MAX	UNIT
vdds_dv_bank1	Supply voltage for serial interface bank1 dual voltage IOs		–0.5	2.10	V
vdds_dv_bank2	Supply voltage for serial interface bank2 dual voltage IOs		–0.5	2.10	V
vdds_dv_bank3	Supply voltage for serial interface bank3 dual voltage IOs		–0.5	2.10	V
vdds_dv_bank4	Supply voltage for serial interface bank4 dual voltage IOs		–0.5	2.10	V
vdds_dv_bank5	Supply voltage for serial interface bank5 dual voltage IOs		–0.5	2.10	V
vdds_dv_bank6	Supply voltage for serial interface bank6 dual voltage IOs		–0.5	2.10	V
vdds_dv_bank7	Supply voltage for serial interface bank7 dual voltage IOs		–0.5	2.10	V
vdds_dv_fref	Supply voltage for FREF dual voltage IOs		–0.5	2.10	V
vdds_usim	Supply voltage for SIM dual voltage IOs		–0.5	3.80	V
vddq_lpddr2	Supply voltage for LPDDR2 IOs		–0.4	1.50	V
vddq_vref_lpddr2	Supply voltage for LPDDR2 DQ VREF: Channel 1 on ball G15 Channel 2 on ball T8		–0.4	1.50	V
vddca_lpddr2	Supply voltage for LPDDR2 CA, clock, clock enable, and chip select IOs		–0.4	1.50	V
vddca_vref_lpddr2	Supply voltage for LPDDR2 CA VREF: Channel 1 on ball Y14 Channel 2 on ball R27		–0.4	1.50	V
V_{ESD}	ESD stress voltage[1]	HBM (Human Body Model)[2]	>1000		V
		CDM (Charged Device Model)[3]	>250		
I_{IOI}	Current-pulse injection on each I/O pin[6]		100		mA
I_{clamp}	Clamp current for an input or output		–20	20	mA
T_{STG} [5]	Storage temperature range after soldered onto PC Board		–65	150	°C

(1) Electrostatic discharge (ESD) to measure device sensitivity/immunity to damage caused by electrostatic discharges into the device.

(2) ANSI/ESDA/JEDEC JS-001-2010. JEDEC documents JEP155 states that 1000-V HBM allows safe manufacturing with basic ESD control methods.

(3) JEDEC JESD22-C101E. JEDEC documents JEP157 states that 250-V CDM allows safe manufacturing with basic ESD control methods.

(4) vpp must be unconnected. vpp_cust is only powered when programming CPFROM eFuses. Otherwise, it is recommended to leave vpp_cust turned off (floating). Note that if the TWL6030 PMIC is used then the vpp pull-down resistor inside the TWL6030 must be disabled when the vpp_cust is turned off.

(5) For tape and reel the storage temperature range is [–10°C to 50°C] with a maximum relative humidity of 70%. It is recommended returning to ambient room temperature before usage.

(6) Device meets latch-up requirement per JEDEC JESD78 class I when stressed at room temperature with I/O pin injection of the lower of specified current or current reached at 1.5 times maximum I/O voltage.

Table 3-2 summarizes the power consumption at the ball level.

Table 3-2. Maximum Current Ratings at Ball Level

PARAMETER				MAX	UNIT
SIGNAL	DESCRIPTION				
vdd_mpu[1]	Maximum current rating for ARM MPU	OPPNTSB (MPU @ 1200 MHz)[5]	Peak current	1900	mA
			Sustained current (worst case)	1600	
		OPPNT (MPU @ 1000 MHz)	Peak current	1450	mA
			Sustained current (worst case)	1300	
vdd_iva_audio[1]	Maximum current rating for IVA3 and audio back-end (BE)			700	mA
vdd_core[1]	Maximum current rating for OMAP Core		Sustained current (worst case)	850	mA
vpp[4]	Maximum current rating for eFuse programming			50	mA
vpp_cust[4]	Maximum current rating for customer eFuse programming			50	mA
vdda_dll0_lpddr21	Maximum current rating for LPDDR21 DLL providing clocks to bytes 0 and 2			5	mA
vdda_dll1_lpddr21	Maximum current rating for LPDDR21 DLL providing clocks to bytes 1 and 3			5	mA
vdda_dll0_lpddr22	Maximum current rating for LPDDR22 DLL providing clocks to bytes 0 and 2			5	mA

Table 3-2. Maximum Current Ratings at Ball Level (continued)

PARAMETER		MAX	UNIT
SIGNAL	DESCRIPTION		
vdda_dll1_lpddr22	Maximum current rating for LPDDR22 DLL providing clocks to bytes 1 and 3	5	mA
vdda_dpll_mpu	Maximum current rating for MPU DPLLs	5	mA
vdda_dpll_core_audio	Maximum current rating for core and audio DPLLs	10	mA
vdda_dpll_iva_per	Maximum current rating for IVA and peripheral DPLLs	10	mA
vdda_csi21	Maximum current rating for CSI21 PHY buffer	10	mA
vdda_csi22	Maximum current rating for CSI22 PHY buffer	5	mA
vdda_dsi1	Maximum current rating for DSI1 PHY buffer	15	mA
vdda_dsi2	Maximum current rating for DSI2 PHY buffer	10	mA
vdda_ldo_sram_mpu	Maximum current rating for MPU SRAM LDO	30	mA
vdda_ldo_sram_iva_audio	Maximum current rating for IVA and audio SRAM LDO	30	mA
vdda_ldo_sram_core	Maximum current rating for Core SRAM LDO	30	mA
vdda_ldo_emu_wkup	Maximum current rating for wake-up / emulation LDO	60	mA
vdda_bdgp_vbb	Maximum current rating for bandgap	60	mA
vdda_hdmi_vdac	Maximum current rating for HDMI PHY buffers and Video DAC	35	mA
vdda_usba0otg_3p3v	Maximum current rating for USB PHY 3.3-V buffers	30	mA
vdda_usba0otg_1p8v	Maximum current rating for USB PHY 1.8-V buffers	35	mA
vdds_1p2v	Maximum current rating for 1.2-V I/O macros	20	mA
vdds_1p8v	Maximum current rating for 1.8-V I/O macros	140	mA
vdds_1p8_fref	Maximum current rating for 1.8-V FREF I/O macros	5	mA
vdds_dv_gpmc	Maximum current rating for GPMC dual voltage IOs	10	mA
vdds_sdmmc1(2)	Maximum current rating for SDMMC1 dual voltage IOs	20	mA
vdds_dv_sdmmc2(2)	Maximum current rating for SDMMC2 dual voltage IOs	10	mA
vdds_dv_c2c	Maximum current rating for GPMC second dual voltage IOs	5	mA
vdds_dv_cam	Maximum current rating for Camera dual voltage IOs	5	mA
vdds_dv_bank0	Maximum current rating for serial interface bank0 dual voltage IOs	5	mA
vdds_dv_bank1	Maximum current rating for serial interface bank1 dual voltage IOs	5	mA
vdds_dv_bank2	Maximum current rating for serial interface bank2 dual voltage IOs	5	mA
vdds_dv_bank3	Maximum current rating for serial interface bank3 dual voltage IOs	5	mA
vdds_dv_bank4	Maximum current rating for serial interface bank4 dual voltage IOs	5	mA
vdds_dv_bank5	Maximum current rating for serial interface bank5 dual voltage IOs	5	mA
vdds_dv_bank6	Maximum current rating for serial interface bank6 dual voltage IOs	5	mA
vdds_dv_bank7	Maximum current rating for serial interface bank6 dual voltage IOs	5	mA
vdds_dv_fref	Maximum current rating for FREF dual voltage IOs	5	mA
vdds_usim(3)	Maximum current rating for SIM dual voltage IOs	20	mA
vddq_lpddr2	Maximum current rating for LPDDR2 IOs	275	mA
vddq_vref_lpddr2	Maximum current rating for LPDDR2 DQ VREF: Channel 1 on ball G15 Channel 2 on ball T8	1	mA
vddca_lpddr2	Maximum current rating for LPDDR2 CA, clock, clock enable and chip select IOs	25	mA
vddca_vref_lpddr2	Maximum current rating for LPDDR2 CA VREF: Channel 1 on ball Y14 Channel 2 on ball R27	1	mA

(1) With SmartReflex™ enabled.

(2) MMC card and I/O card are not included.

(3) SIM card and I/O card are not included.

(4) vpp must be unconnected. vpp_cust is only powered when programming CPFROM eFuses. Otherwise, it is recommended to leave vpp_cust turned off (floating). Note that if the TWL6030 PMIC is used then the vpp pull-down resistor inside the TWL6030 must be disabled when the vpp_cust is turned off.

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(5) Maximum currents for the MPU at 1.2 GHz are preliminary data. They could change following the silicon results.

3.2 Recommended Operating Conditions

The device is used under the recommended operating conditions described in Table 3-3.

NOTE

Logic functions and parameter values are not assured out of the range specified in the recommended operating conditions.

Table 3-3. Recommended Operating Conditions

PARAMETER	DESCRIPTION		MIN	NOM	MAX	UNIT
Input Power Supply Voltage Range						
vdd_mpu	Supply voltage for ARM MPU domain			See [(1)]		V
	Noise (peak-peak)	f < 10 MHz		80		mV_{PPmax}
		f ≥ 10 MHz		50		
vdd_iva_audio	Supply voltage range for IVA3 and audio BE domain			See [(1)]		V
	Noise (peak-peak)	f < 10 MHz		80		mV_{PPmax}
		f ≥ 10 MHz		50		
vdd_core	Supply voltage range for OMAP Core domain			See [(1)]		V
	Noise (peak-peak)	f < 10 MHz		80		mV_{PPmax}
		f ≥ 10 MHz		50		
vdda_dll0_lpddr21	Supply voltage for LPDDR21 DLL providing clocks to bytes 0 and 2		1.0	1.1	1.2	V
	Noise (peak-peak)			50		mV_{PPmax}
vdda_dll1_lpddr21	Supply voltage for LPDDR21 DLL providing clocks to bytes 1 and 3		1.0	1.1	1.2	V
	Noise (peak-peak)			50		mV_{PPmax}
vdda_dll0_lpddr22	Supply voltage for LPDDR22 DLL providing clocks to bytes 0 and 2		1.0	1.1	1.2	V
	Noise (peak-peak)			50		mV_{PPmax}
vdda_dll1_lpddr22	Supply voltage for LPDDR22 DLL providing clocks to bytes 1 and 3		1.0	1.1	1.2	V
	Noise (peak-peak)			50		mV_{PPmax}
vdda_dpll_mpu	Supply voltage for MPU DPLLs		1.71	1.80	1.89	V
	Noise (peak-peak)			50		mV_{PPmax}
vdda_dpll_core_audio	Supply voltage for core and audio DPLLs		1.71	1.80	1.89	V
	Noise (peak-peak)			50		mV_{PPmax}
vdda_dpll_iva_per	Supply voltage for IVA and peripheral DPLLs		1.71	1.80	1.89	V
	Noise (peak-peak)			50		mV_{PPmax}
vdda_csi21	Supply voltage for CSI21 PHY buffer		1.71	1.80	1.89	V
	Noise (peak-peak)			50		mV_{PPmax}
vdda_csi22	Supply voltage for CSI22 PHY buffer		1.71	1.80	1.89	V
	Noise (peak-peak)			50		mV_{PPmax}
vdda_dsi1	Supply voltage for DSI1 PHY buffer		1.71	1.80	1.89	V
	Noise (peak-peak)	High-speed mode		50		mV_{PPmax}
		Low-power mode				
vdda_dsi2	Supply voltage for DSI2 PHY buffer		1.71	1.80	1.89	V
	Noise (peak-peak)	High-speed mode		50		mV_{PPmax}
		Low-power mode				

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Table 3-3. Recommended Operating Conditions (continued)

PARAMETER	DESCRIPTION		MIN	NOM	MAX	UNIT
vdda_ldo_sram_mpu	Supply voltage for MPU SRAM LDO		1.71	1.80	1.89	V
	Noise (peak-peak)			50		mV_{PPmax}
vdda_ldo_sram_iva_ audio	Supply voltage for IVA and audio SRAM LDO		1.71	1.80	1.89	V
	Noise (peak-peak)			50		mV_{PPmax}
vdda_ldo_sram_core	Supply voltage for Core SRAM LDO		1.71	1.80	1.89	V
	Noise (peak-peak)			50		mV_{PPmax}
vdda_ldo_emu_wkup	Supply voltage for wake-up / emulation LDO		1.00	1.20	1.26	V
	Noise (peak-peak)			50		mV_{PPmax}
vdda_bdgp_vbb	Supply voltage for bandgap		1.71	1.80	1.89	V
	Noise (peak-peak)			50		mV_{PPmax}
vdda_hdmi_vdac	Supply voltage for HDMI PHY buffers		1.71	1.80	1.89	V
	Noise (peak-peak)			50		mV_{PPmax}
	Supply voltage for video DAC		1.71	1.80	1.89	V
	Maximum noise (peak-peak) for a frequency from 0 to 100 kHz (For a frequency > 100 kHz, decreases 20dB/dec)			30		mV_{PPmax}
vdda_usba0otg_3p3v	Supply voltage for USB PHY 3.3-V buffers		3.0	3.3	3.6	V
	Noise (peak-peak)			50		mV_{PPmax}
vdda_usba0otg_1p8v	Supply voltage for USB PHY 1.8-V buffers		1.71	1.80	1.89	V
	Noise (peak-peak)			50		mV_{PPmax}
vdds_1p2v	Supply voltage for 1.2-V I/O macros		1.14	1.20	1.26	V
	Noise (peak-peak)			50		mV_{PPmax}
vdds_1p8v	Supply voltage for 1.8-V I/O macros		1.71	1.80	1.89	V
	Noise (peak-peak)			50		mV_{PPmax}
vdds_1p8_fref	Supply voltage for 1.8-V FREF I/O macros		1.71	1.80	1.89	V
	Noise (peak-peak)			50		mV_{PPmax}
vdds_dv_gpmc	Supply voltage for GPMC dual voltage IOs	1.2-V Mode	1.14	1.20	1.26	V
		1.8-V Mode	1.71	1.80	1.89	
	Noise (peak-peak)	1.2-V Mode		50		mV_{PPmax}
		1.8-V Mode				
vdds_sdmmc1[2]	Supply voltage for SDMMC1 dual voltage IOs	1.8-V Mode	1.71	1.80	1.89	V
		3.0-V Mode	2.7	3.0	3.6	
	Noise (peak-peak)	1.8-V Mode		50		mV_{PPmax}
		3.0-V Mode				
vdds_dv_sdmmc2[2]	Supply voltage for SDMMC2 dual voltage IOs	1.2-V Mode	1.14	1.20	1.26	V
		1.8-V Mode	1.71	1.80	1.89	
	Noise (peak-peak)	1.2-V Mode		50		mV_{PPmax}
		1.8-V Mode				
vdds_dv_c2c	Supply voltage for GPMC second dual voltage IOs	1.2-V Mode	1.14	1.20	1.26	V
		1.8-V Mode	1.71	1.80	1.89	
	Noise (peak-peak)	1.2-V Mode		50		mV_{PPmax}
		1.8-V Mode				
vdds_dv_cam	Supply voltage for Camera dual voltage IOs	1.2-V Mode	1.14	1.20	1.26	V
		1.8-V Mode	1.71	1.80	1.89	
	Noise (peak-peak)	1.2-V Mode		50		mV_{PPmax}
		1.8-V Mode				

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Table 3-3. Recommended Operating Conditions (continued)

PARAMETER	DESCRIPTION		MIN	NOM	MAX	UNIT
vdds_dv_bank0	Supply voltage for serial interface bank0 dual voltage IOs	1.2-V Mode	1.14	1.20	1.26	V
		1.8-V Mode	1.71	1.80	1.89	
	Noise (peak-peak)	1.2-V Mode		50		mV_{PPmax}
		1.8-V Mode				
vdds_dv_bank1	Supply voltage for serial interface bank1 dual voltage IOs	1.2-V Mode	1.14	1.20	1.26	V
		1.8-V Mode	1.71	1.80	1.89	
	Noise (peak-peak)	1.2-V Mode		50		mV_{PPmax}
		1.8-V Mode				
vdds_dv_bank2	Supply voltage for serial interface bank2 dual voltage IOs	1.2-V Mode	1.14	1.20	1.26	V
		1.8-V Mode	1.71	1.80	1.89	
	Noise (peak-peak)	1.2-V Mode		50		mV_{PPmax}
		1.8-V Mode				
vdds_dv_bank3	Supply voltage for serial interface bank3 dual voltage IOs	1.2-V Mode	1.14	1.20	1.26	V
		1.8-V Mode	1.71	1.80	1.89	
	Noise (peak-peak)	1.2-V Mode		50		mV_{PPmax}
		1.8-V Mode				
vdds_dv_bank4	Supply voltage for serial interface bank4 dual voltage IOs	1.2-V Mode	1.14	1.20	1.26	V
		1.8-V Mode	1.71	1.80	1.89	
	Noise (peak-peak)	1.2-V Mode		50		mV_{PPmax}
		1.8-V Mode				
vdds_dv_bank5	Supply voltage for serial interface bank5 dual voltage IOs	1.2-V Mode	1.14	1.20	1.26	V
		1.8-V Mode	1.71	1.80	1.89	
	Noise (peak-peak)	1.2-V Mode		50		mV_{PPmax}
		1.8-V Mode				
vdds_dv_bank6	Supply voltage for serial interface bank6 dual voltage IOs	1.2-V Mode	1.14	1.20	1.26	V
		1.8-V Mode	1.71	1.80	1.89	
	Noise (peak-peak)	1.2-V Mode		50		mV_{PPmax}
		1.8-V Mode				
vdds_dv_bank7	Supply voltage for serial interface bank7 dual voltage IOs	1.2-V Mode	1.14	1.20	1.26	V
		1.8-V Mode	1.71	1.80	1.89	
	Noise (peak-peak)	1.2-V Mode		50		mV_{PPmax}
		1.8-V Mode				
vdds_dv_fref	Supply voltage for FREF dual voltage IOs	1.2-V Mode	1.14	1.20	1.26	V
		1.8-V Mode	1.71	1.80	1.89	
	Noise (peak-peak)	1.2-V Mode		50		mV_{PPmax}
		1.8-V Mode				
vdds_usim[(3)]	Supply voltage for SIM dual voltage IOs	1.8-V Mode	1.71	1.80	1.89	V
		3.0-V Mode	2.7	3.0	3.6	
	Noise (peak-peak)	1.8-V Mode		50		mV_{PPmax}
		3.0-V Mode				
vddq_lpddr2	Supply voltage for LPDDR2 IOs		1.14	1.20	1.30	V
	Noise (peak-peak)				100	mV_{PPmax}
vddq_vref_lpddr2	Supply voltage for LPDDR2 DQ VREF: Channel 1 on ball G15 Channel 2 on ball T8		1.14	1.20	1.30	V
	Noise (peak-peak)				12	mV_{PPmax}

Table 3-3. Recommended Operating Conditions (continued)

PARAMETER	DESCRIPTION	MIN	NOM	MAX	UNIT
vddca_lpddr2	Supply voltage for LPDDR2 CA, clock, clock enable and chip select IOs	1.14	1.20	1.30	V
	Noise (peak-peak)			100	mV_{PPmax}
vddca_vref_lpddr2	Supply voltage for LPDDR2 CA VREF: Channel 1 on ball Y14 Channel 2 on ball R27	1.14	1.20	1.30	V
	Noise (peak-peak)			12	mV_{PPmax}
vpp[(2)]	Supply voltage for eFuse	1.65	1.70	1.75	V
vpp_cust[(2)]	Supply voltage for customer eFuse	1.65	1.70	1.75	V
V_{PAD}	Voltage at I/O pad	0		vddy[(3)]	V
vssa_usba0otg_3p3v	Ground for USB PHY 3.3-V buffer		0		V
vssa_usba0otg	Ground for USB PHY 1.8-V buffer		0		V
vssa_hdmi_vdac	Ground for HDMI PHY buffers and Video DAC		0		V
vssa_csi2	Ground for CSI2 PHY buffer		0		V
vssa_dsi	Ground for DSI buffer		0		V
vss	Main ground		0		V
T_B[(4)]	Operating board (PCB) temperature range	–40		85	°C
T_J [(4)(5)]	Operating junction temperature range (vpp turned off—floating)	–40		110[(5)]	°C
$T_{J\text{-}VPP}$[(2)]	Operating junction temperature range during eFuse programming (vpp turned on)	–10		65	°C
Output Power Supply Voltage Range					
lpddr2_vref_dq	LPDDR2 DQ VREF output power supply to memory: Channel 1 on ball B15 Channel 2 on ball R2	0.49 * vddq_vref_ lpddr2	0.50 * vddq_vref_ lpddr2	0.51 * vddq_vref_ lpddr2	V
lpddr2_vref_ca	LPDDR2 CA VREF output power supply to memory: Channel 1 on ball AH16 Channel 2 on ball U28	0.49 * vddca_vref_ lpddr2	0.50 * vddca_vref_ lpddr2	0.51 * vddca_vref_ lpddr2	V

(1) See the operating condition addendum for values. OPP voltage values may change following the silicon characterization result.

(2) vpp must be unconnected. vpp_cust is only powered when programming CPFROM eFuses. Otherwise, it is recommended to leave vpp_cust turned off (floating). Note that if the TWL6030 PMIC is used then the vpp pull-down resistor inside the TWL6030 must be disabled when the vpp_cust is turned off.

(3) vddy refers to vdda_csiphy1, vdda_csiphy2, vdda_dsi, vdda_dac, vdds, vdds_mem, vdds_sdmmc1, and vdds_usim.

(4) The board temperature (T_B) and junction temperature (T_J) ranges are defined for 2S2P board types (reference JEDEC standard JESD51-9, *Test Board for Array Surface Mount Package Thermal Measurements*). Note that the board temperature is measured at 1 mm from the package edge.

(5) Maximum supported junction temperature in functional operating condition is 110°C. That does not mean that 110°C of junction temperature is supported continuously. For more information on reliability, see Table 3-4, *Power On Hour (POH) Limits* example of profile.

Table 3-4. Power On Hour (POH) Limits[(1)(4)(5)]

OMAP4430 DEVICE	CASE	VOLTAGE (V)[(3)]	MAXIMUM FREQUENCY (MHz)			T_J(°C)[(2)]	POH (h)
			MPU	IVA	CORE		
OMAP4430-1000	43830 Hours (5 years)	≤ OPPNT	1000	266	400	93	2641
		≤ OPP100	600	266	400	48	1377
		≤ OPP50	300	133	200	59	6487
		≤ OPP50	98	133	200	30	1381
		RETENTION	-	-	-	25	31945
		Total					**43830**

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(1) For other use cases, contact TI for evaluation to determine if they can be supported.

(2) T_J is the average operating junction temperature.

(3) See the operating condition addendum for values.

(4) With SmartReflex™ enabled.

(5) The power on hour (POH) analysis is based on a typical use case with following parameters:
- The percentage (%) of activity by day for each application of the use case
- The MPU, IVA, and CORE voltages and frequencies by application (ideally the use of vdd_mpu, vdd_iva_audio, or vdd_core OPPs)
- The average operating junction temperature
- SmartReflex™ (power optimization techniques) use or not.

The above power on hour use case is based on a 5 years lifetime use profile for smartphones and other mobile devices. Other use cases can apply for other devices in other fields and for a lifetime up to 5 years.

3.3 DC Electrical Characteristics

Table 3-5 through Table 3-20 summarize the dc electrical characteristics.

NOTE

The data specified in Table 3-5 through Table 3-20 are subject to change.

NOTE

The dc electrical characteristics of the CVIDEO IO are detailed in Section 5, *Video DAC Specifications*.

NOTE

The interfaces or signals described in Table 3-5 through Table 3-20 correspond to the interfaces or signals available in multiplexing mode 0.

All interfaces or signals multiplexed on the balls / pins described in these tables have the same dc electrical characteristics, unless multiplexing involves a PHY/GPIO combination in which case different dc electrical characteristics are specified for the different multiplexing modes.

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3.3.1 GPMC DC Electrical Characteristics

Table 3-5 summarizes the GPMC dc electrical characteristics in multiplexing mode 0.

NOTE

For more information on the IO cell configurations (SC[1:0], MB[1:0] and LB0), see the Control Module / Control Module Functional Description / Functional Register Description / Signal Integrity Parameter Control Registers With Pad Group Assignment section of the OMAP4430 TRM.

Table 3-5. GPMC DC Electrical Characteristics

PARAMETER		MIN	NOM	MAX	UNIT
Signals in Mode 0: gpmc_ad[15:0], gpmc_a[25:16], gpmc_ncs[7:0], gpmc_clk, gpmc_nadv_ale, gpmc_noe, gpmc_nwe, gpmc_nbe0_cle, gpmc_nbe1, gpmc_wait[2:1][(5)] (**Bottom Balls**: C12 / D12 / C13 / D13 / C15 ,D15 / A16 / B16 / C16 / D16 / C17 / D17 / C18 / D18 / C19 / D19 / B17 / A18 / B18 / A19 / B19 / B20 / A21 / B21 / C20 / D20 / B25 / C21 / D21 / C22 / B22 / D25 / B11 / B12 / C23 / D22 / B23 / D23 / A24 / B24 / C24 / D24)[(5)]					
GPMC Mode					
C_{LOAD}	Load capacitance	5		10	pF
t_{OT}	Output transition time (rise time, t_R or fall time, t_F), measured between 20% and 80% of PAD voltage, maximum at maximum load)			2	ns
1.8-V Mode					
V_{IH}	Input high-level threshold	0.65 * vdds_dv_y[(2)]			V
V_{IL}	Input low-level threshold			0.35 * vdds_dv_y[(2)]	V
V_{OH}	Output high-level threshold (I_{OH} = –6 mA)	vdds_dv_y[(2)] – 0.45			V
V_{OL}	Output low-level threshold (I_{OL} = 6 mA)			0.45	V
V_{HYS}[(3)]	Input hysteresis voltage	150			mV
1.2-V Mode					
V_{IH}	Input high-level threshold	0.65 * vdds_dv_y[(2)]			V
V_{IL}	Input low-level threshold			0.35 * vdds_dv_y[(2)]	V
V_{OH}	Output high-level threshold (I_{OH} = –6 mA)	0.75 * vdds_dv_y[(2)]			V
V_{OL}	Output low-level threshold (I_{OL} = 6 mA)			0.25 * vdds_dv_y[(2)]	V
V_{HYS}[(3)]	Input hysteresis voltage	135			mV
SDMMC2					
1.8-V Mode					
C_{LOAD}	Load capacitance	2		5	pF
t_{OT}	Output transition time (rise time, t_R or fall time, t_F), measured between 20% and 80% of PAD voltage, maximum at maximum load)			2.7	ns
V_{IH}	Input high-level threshold	0.65 * vdds_dv_y[(2)]			V
V_{IL}	Input low-level threshold			0.35 * vdds_dv_y[(2)]	V
V_{OH}	Output high-level threshold (I_{OH} = –6 mA)	vdds_dv_y[(2)] – 0.45			V
V_{OL}	Output low-level threshold (I_{OL} = 6 mA)			0.45	V
V_{HYS}[(3)]	Input hysteresis voltage	150			mV
1.2-V Mode					
C_{LOAD}	Load capacitance	2		5	pF
t_{OT}	Output transition time (rise time, t_R or fall time, t_F), measured between 20% and 80% of PAD voltage, maximum at maximum load)			2.8	ns
V_{IH}	Input high-level threshold	0.65 * vdds_dv_y[(2)]			V
V_{IL}	Input low-level threshold			0.35 * vdds_dv_y[(2)]	V
V_{OH}	Output high-level threshold (I_{OH} = –6 mA)	0.75 * vdds_dv_y[(2)]			V

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Table 3-5. GPMC DC Electrical Characteristics (continued)

PARAMETER			MIN	NOM	MAX	UNIT
V_{OL}	Output low-level threshold (I_{OL} = 6 mA)				0.25 * vdds_dv_y(2)	V
V_{HYS}(3)	Input hysteresis voltage		135			mV
Signal in Mode 0: gpmc_wait0 (**Bottom Ball**: B26)						
C_{LOAD}	Load capacitance	SC[1:0] = 00	4		60	pF
		SC[1:0] = 01	2		21	
		SC[1:0] = 10	7		33	
t_{OT}	Output transition time (rise time, t_R or fall time, t_F) measured between 10% to 90% of PAD voltage, minimum at the minimum load and maximum at the maximum load	SC[1:0] = 00	1		15	ns
		SC[1:0] = 01	0.4		5	
		SC[1:0] = 10	0.6		7	
1.2-V Mode						
V_{IH}	Input high-level threshold		0.65 * vdds_dv_gpmc		vdds_dv_gpmc + 0.3	V
V_{IL}	Input low-level threshold		–0.3		0.35 * vdds_dv_gpmc	V
V_{HYS}(3)	Input hysteresis voltage		135			mV
V_{OH}	Output high-level threshold (I_{OH} = –4 mA)		0.75 * vdds_dv_gpmc			V
V_{OL}	Output low-level threshold (I_{OL} = 4 mA)				0.25 * vdds_dv_gpmc	V
1.8-V Mode						
V_{IH}	Input high-level threshold		0.65 * vdds_dv_gpmc		vdds_dv_gpmc + 0.3	V
V_{IL}	Input low-level threshold		–0.3		0.35 * vdds_dv_gpmc	V
V_{HYS}(3)	Input hysteresis voltage		150			mV
V_{OH}	Output high-level threshold (I_{OH} = –4 mA)		vdds_dv_gpmc – 0.45			V
V_{OL}	Output low-level threshold (I_{OL} = 4 mA)				0.45	V
Signal in Mode 0: gpmc_nwp (**Bottom Ball**: C25)						

Table 3-5. GPMC DC Electrical Characteristics (continued)

PARAMETER			MIN	NOM	MAX	UNIT
C_{LOAD}[(4)]	Load capacitance	MB[1:0] = 11 LB0 = 1 (Mode1) maximum frequency = 24 MHz transmission line delay = 670 ps	20		25	pF
		MB[1:0] = 11 LB0 = 1 (Mode1) maximum frequency = 60 MHz transmission line delay = 335 ps	2		5	
		MB[1:0] = 01 LB0 = 0 (Mode2) maximum frequency = 25 MHz transmission line delay = 335 ps	14		17	
		MB[1:0] = 01 LB0 = 0 (Mode2) maximum frequency = 48 MHz transmission line delay = 536 ps	2		5	
		MB[1:0] = 10 LB0 = 1 (Mode3) maximum frequency = 20 MHz transmission line delay = 838 ps	23		28	
		MB[1:0] = 10 LB0 = 1 (Mode3) maximum frequency = 24 MHz transmission line delay = 670 ps	16		20	
		MB[1:0] = 10 LB0 = 0 (Mode4) maximum frequency = 4 MHz transmission line delay = 1675 ps	16		20	
		MB[1:0] = 10 LB0 = 0 (Mode4) maximum frequency = 25 MHz transmission line delay = 670 ps	2		5	
		MB[1:0] = 10 LB0 = 0 (Mode4) maximum frequency = 25 MHz transmission line delay = 670 ps	5		7	
		MB[1:0] = 10 LB0 = 0 (Mode4) maximum frequency = 25 MHz transmission line delay = 536 ps	2		11	
t_{OT}[(4)]	Output transition time (rise time, t_R or fall time, t_F) measured between 10% to 90% of PAD voltage, maximum at the maximum load	MB[1:0] = 11 LB0 = 1 (Mode1) maximum frequency = 24 MHz transmission line delay = 670 ps			10	ns
		MB[1:0] = 11 LB0 = 1 (Mode1) maximum frequency = 60 MHz transmission line delay = 335 ps			4	
		MB[1:0] = 01 LB0 = 0 (Mode2) maximum frequency = 25 MHz transmission line delay = 335 ps			5.6[(1)]	
		MB[1:0] = 01 LB0 = 0 (Mode2) maximum frequency = 48 MHz transmission line delay = 536 ps			6.3	
		MB[1:0] = 10 LB0 = 1 (Mode3) maximum frequency = 20 MHz transmission line delay = 838 ps			10.5[(1)]	
		MB[1:0] = 10 LB0 = 1 (Mode3) maximum frequency = 24 MHz transmission line delay = 670 ps			12.5	
		MB[1:0] = 10 LB0 = 0 (Mode4) maximum frequency = 4 MHz transmission line delay = 1675 ps			16.8[(1)]	
		MB[1:0] = 10 LB0 = 0 (Mode4) maximum frequency = 25 MHz transmission line delay = 670 ps			10	
		MB[1:0] = 10 LB0 = 0 (Mode4) maximum frequency = 25 MHz transmission line delay = 670 ps			12.2	
		MB[1:0] = 10 LB0 = 0 (Mode4) maximum frequency = 25 MHz transmission line delay = 536 ps			8[(1)]	

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Table 3-5. GPMC DC Electrical Characteristics (continued)

PARAMETER		MIN	NOM	MAX	UNIT
1.2-V Mode					
V_{IH}	Input high-level threshold	0.65 * vdds_dv_gpmc		vdds_dv_gpmc + 0.3	V
V_{IL}	Input low-level threshold	–0.3		0.35 * vdds_dv_gpmc	V
V_{HYS} (3)	Input hysteresis voltage	135			mV
V_{OH}	Output high-level threshold (I_{OH} = 4 mA)	0.75 * vdds_dv_gpmc			V
V_{OL}	Output low-level threshold (I_{OL} = 4 mA)			0.25 * vdds_dv_gpmc	V
1.8-V Mode					
V_{IH}	Input high-level threshold	0.65 * vdds_dv_gpmc		vdds_dv_gpmc + 0.3	V
V_{IL}	Input low-level threshold	–0.3		0.35 * vdds_dv_gpmc	V
V_{HYS} (3)	Input hysteresis voltage	150			mV
V_{OH}	Output high-level threshold (I_{OH} = 4 mA)	vdds_dv_gpmc – 0.45			V
V_{OL}	Output low-level threshold (I_{OL} = 4 mA)			0.45	V

(1) Output transition time measured between 20% to 80% of vdds_dv_gpmc.

(2) In vdds_dv_y, y can have the value gpmc, sdmmc1, c2c depending on the pin or ball used. For more information of the power supply name and the corresponding pin, ball, see the POWER [9] column of Table 2-1.

(3) V_{HYS} is the magnitude of the difference between the positive-going threshold voltage V_{T+} and the negative-going threshold voltage V_{T-}.

(4) Depending on the programming mode, different output load and transition time are available following the targeted maximum frequency, transmission line or output transition time.

(5) The following signals in Mode 0 gpmc_ad[15:0], gpmc_a[25:16], gpmc_ncs[7:0], gpmc_clk, gpmc_nadv_ale, gpmc_noe, gpmc_nwe, gpmc_nbe0_cle, gpmc_nbe1, and gpmc_wait[2:1] (bottom balls: C12 / D12 / C13 / D13 / C15 ,D15 / A16 / B16 / C16 / D16 / C17 / D17 / C18 / D18 / C19 / D19 / B17 / A18 / B18 / A19 / B19 / B20 / A21 / B21 / C20 / D20 / B25 / C21 / D21 / C22 / B22 / D25 / B11 / B12 / C23 / D22 / B23 / D23 / A24 / B24 / C24 / D24) are compliant with the JEDEC standard for the following parameters:
V_{OL} = 0.2 V and V_{OH} = VDDS – 0.2 V when absolute value of I_{OH} / I_{OL} = 100 µA.

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3.3.2 LPDDR2 DC Electrical Characteristics

Table 3-6 summarizes the LPDDR2 dc electrical characteristics in multiplexing mode 0.

NOTE

For more information on the IO cell configurations (i[2:0], sr[1:0], vref_tap[1:0]), see the Control Module / Control Module Functional Description / Functional Register Description / Signal Integrity Parameter Control Registers With Pad Group Assignment section of the OMAP4430 TRM.

Table 3-6. LPDDR2 DC Electrical Characteristics

PARAMETER			MIN	NOM	MAX	UNIT
Signals in Mode 0: lpddr21_dq[31:0], lpddr21_ca[9:0], lpddr21_dm[3:0], lpddr21_ncs[1:0], lpddr21_cke[1:0], lpddr22_dq[31:0], lpddr22_ca[9:0], lpddr22_dm[9:0], lpddr22_ncs[1:0], lpddr22_cke[1:0] (**Top Balls**: E29 / D28 / B27 / A27 / A26 / B26 / A25 / A24 / B19 / A19 / A18 / A17 / B17 / A13 / A12 / B12 / N28 / N29 / M29 / L28 / K28 / K29 / J29 / H29 / B8 / A8 / A7 / B6 / B5 / A5 / A4 / B3 / AJ27 / AH27 / AH26 / AH25 / AJ25 / AJ20 / AH20 / AH19 / AJ18 / AH17 / B22 / A21 / F28 / B11 / AH24 / AJ24 / AH23 / AJ23 / L2 / M1 / N1 / U2 / V1 / W2 / W1 / Y2 / AE1 / AF1 / AG1 / AG2 / AJ3 / AH4 / AJ5 / AH6 / C2 / D1 / E1 / E2 / F2 / G1 / H1 / H2 / AJ9 / AJ10 / AH10 / AH11 / AJ12 / AJ13 / AH13 / AJ14 / R29 / T29 / U29 / V29 / W28 / AC29 / AD29 / AD28 / AE28 / AF29 / AB1 / AC2 / L1 / AH7 / Y28 / W29 / AA29 / Y29)						
V_{IH}	Input high-level threshold		0.5 * vddx_lpddr2(7) + 0.13		vddx_lpddr2(7) + 0.2	V
V_{IL}	Input low-level threshold		–0.2		0.5 * vddx_lpddr2(7) – 0.13	V
V_{HYS}(1)	Input hysteresis voltage			NA(1)		mV
C_{IN}	Input capacitance				3	pF
V_{OH}	Output high-level threshold (I_{OH} = 0.1 mA)		0.9 * vddx_lpddr2(7)			V
V_{OL}	Output low-level threshold (I_{OL} = 0.1 mA)				0.1 * vddx_lpddr2(7)	V
Z_O	Output impedance	i[2:0] = 000 (Drv5)		1.66 * R_{REF}		Ω
		i[2:0] = 001 (Drv6)		1.33 * R_{REF}		
		i[2:0] = 010 (Drv7)		1.14 * R_{REF}		
		i[2:0] = 011 (Drv8)		R_{REF}(2)		
		i[2:0] = 100 (Drv9)		0.88 * R_{REF}		
		i[2:0] = 101 (Drv10)		0.8 * R_{REF}		
		i[2:0] = 110 (Drv11)		0.73 * R_{REF}		
		i[2:0] = 111 (Drv12)		0.67 * R_{REF}		
t_{OT}	Output transition time/turn-on time (rise time, t_R or fall time, t_F) measured between 10% to 90% of PAD voltage(3)(4)(6)	sr[1:0] = 00 (Fastest)		250		ps
		sr[1:0] = 01 (Faster)		315		
		sr[1:0] = 10 (Fast)		340		
		sr[1:0] = 11 (Slow)		390		
	Maximum noise on the IO supply voltage(3)(5)(6)	sr[1:0] = 00 (Fastest)			215	mV_{PP}
		sr[1:0] = 01 (Faster)			110	
		sr[1:0] = 10 (Fast)			108	
		sr[1:0] = 11 (Slow)			110	
Signals in Mode 0: lpddr21_dqs[3:0], lpddr21_ndqs[3:0], lpddr21_ck, lpddr21_nck, lpddr22_dqs[3:0], lpddr22_ndqs[3:0], lpddr22_ck, lpddr22_nck (**Top Balls**: A23 / B23 / A20 / B20 / G28 / G29 / B10 / A10 / AJ21 / AH21 / AA1 / AA2 / AD2 / AD1 / K2 / K1 / AH8 / AJ8 / AB28 / AB29)						
V_{SWING} (DC)	Input differential swing		0.26		vddx_lpddr2(7) + 0.4	V
V_{CM}	Input common mode range		0.4 * vddx_lpddr2(7)		0.6 * vddx_lpddr2(7)	V
V_{HYS}(1)	Input hysteresis voltage			NA(1)		mV
C_{IN}	Input capacitance				3	pF
V_{OH}	Output high-level threshold (I_{OH} = 0.1 mA)		0.9 * vddx_lpddr2(7)			V
V_{OL}	Output low-level threshold (I_{OL} = 0.1 mA)				0.1 * vddx_lpddr2(7)	V

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Table 3-6. LPDDR2 DC Electrical Characteristics (continued)

PARAMETER			MIN	NOM	MAX	UNIT
Z_O	Output impedance	i[2:0] = 000 (Drv5)		1.66 * R_{REF}		Ω
		i[2:0] = 001 (Drv6)		1.33 * R_{REF}		
		i[2:0] = 010 (Drv7)		1.14 * R_{REF}		
		i[2:0] = 011 (Drv8)		R_{REF}(2)		
		i[2:0] = 100 (Drv9)		0.88 * R_{REF}		
		i[2:0] = 101 (Drv10)		0.8 * R_{REF}		
		i[2:0] = 110 (Drv11)		0.73 * R_{REF}		
		i[2:0] = 111 (Drv12)		0.67 * R_{REF}		
t_{OT}	Output transition time/turn-on time (rise time, t_R or fall time, t_F) measured between 10% to 90% of PAD voltage(3)(4)(6)	sr[1:0] = 00 (Fastest)		250		ps
		sr[1:0] = 01 (Faster)		315		
		sr[1:0] = 10 (Fast)		340		
		sr[1:0] = 11 (Slow)		390		
	Maximum noise on the IO supply voltage(3)(5)(6)	sr[1:0] = 00 (Fastest)			215	mV_{PP}
		sr[1:0] = 01 (Faster)			110	
		sr[1:0] = 10 (Fast)			108	
		sr[1:0] = 11 (Slow)			110	
Signals in Mode 0: lpddr21_vref_ca, lpddr21_vref_dq, lpddr22_vref_ca, lpddr22_vref_dq (**Top Balls**: AH16 / B15 / U28 / R2)						
V_{REF}	Reference generation dc voltage level	vref_tap[1:0] = 00 (Mint_2ua mode)	0.495 * vddy_vref_lpddr2(8)	0.500 * vddy_vref_lpddr2(8)	0.505 * vddy_vref_lpddr2(8)	V
		vref_tap[1:0] = 01 (Mint_4ua mode)	0.492 * vddy_vref_lpddr2(8)	0.500 * vddy_vref_lpddr2(8)	0.508 * vddy_vref_lpddr2(8)	
		vref_tap[1:0] = 10 (Mint_6ua mode)	0.490 * vddy_vref_lpddr2(8)	0.500 * vddy_vref_lpddr2(8)	0.510 * vddy_vref_lpddr2(8)	
		vref_tap[1:0] = 11 (Mint_8ua mode)	0.490 * vddy_vref_lpddr2(8)	0.500 * vddy_vref_lpddr2(8)	0.510 * vddy_vref_lpddr2(8)	

(1) This buffer is designed for high-speed application. In high-speed mode, it is fast enough to avoid any noise on the signal during transition and then hysteresis is not required.

(2) R_{REF} (reference output impedance) is considered to be the production trimming setting for Drv8 mode, with R_{REF} = 50 Ω, which corresponds to Z_O = 50 Ω (I_{OUT} = 8 mA). For a full description of the output impedance setting, see the the Control Module / Control Module Functional Description / Functional Register Description / Signal Integrity Parameter Control Registers With Pad Group Assignment section of the OMAP4430 TRM.

(3) To achieve optimal noise/speed trade off, the slew rate (turn-on time) of the output signal can be programmed using the slew rate control bits sr[1:0]. Please note that the control bits sr[1:0] do not affect the driver DC drive-strength. They only control the driver turn-on time. It is to be noted that turn-on time and maximum supply noise are the parameter defined to help user make relative comparison and correlate the driver operation at different turn-on time settings.

(4) Output transition time/turn-on time for Drv8 setting, i[2:0] = 011. For a full description of this setting, see the Control Module / Control Module Functional Description / Functional Register Description / Signal Integrity Parameter Control Registers With Pad Group Assignment section of the OMAP4430 TRM.

(5) Maximum noise (peak-peak) on the IO supply voltage for Drv8 setting, i[2:0] = 011.

(6) The measurement setup (see Figure 3-1 and Figure 3-2) is not intended as a precise representation of any particular system environment or a depiction of the actual load presented. Maximum output supply noise (see Figure 3-2, L*di/dt) on the IO supply is measured with 1 nH of inductance on the IO supply.

(7) vddx_lpddr2 can have the value vddq_lpddr2, vddca_lpddr21, vddca_lpddr22 depending on the ball used. For more information of the power supply name and the corresponding pin, ball, see the POWER [9] column of Table 2-1.

(8) vddy_vref_lpddr2 can have the value vddca_vref_lpddr21, vddca_lpddr22, vddq_vref_lpddr21, vddq_vref_lpddr22 depending on the ball used. For more information of the power supply name and the corresponding pin, ball, see the POWER [9] column of Table 2-1.

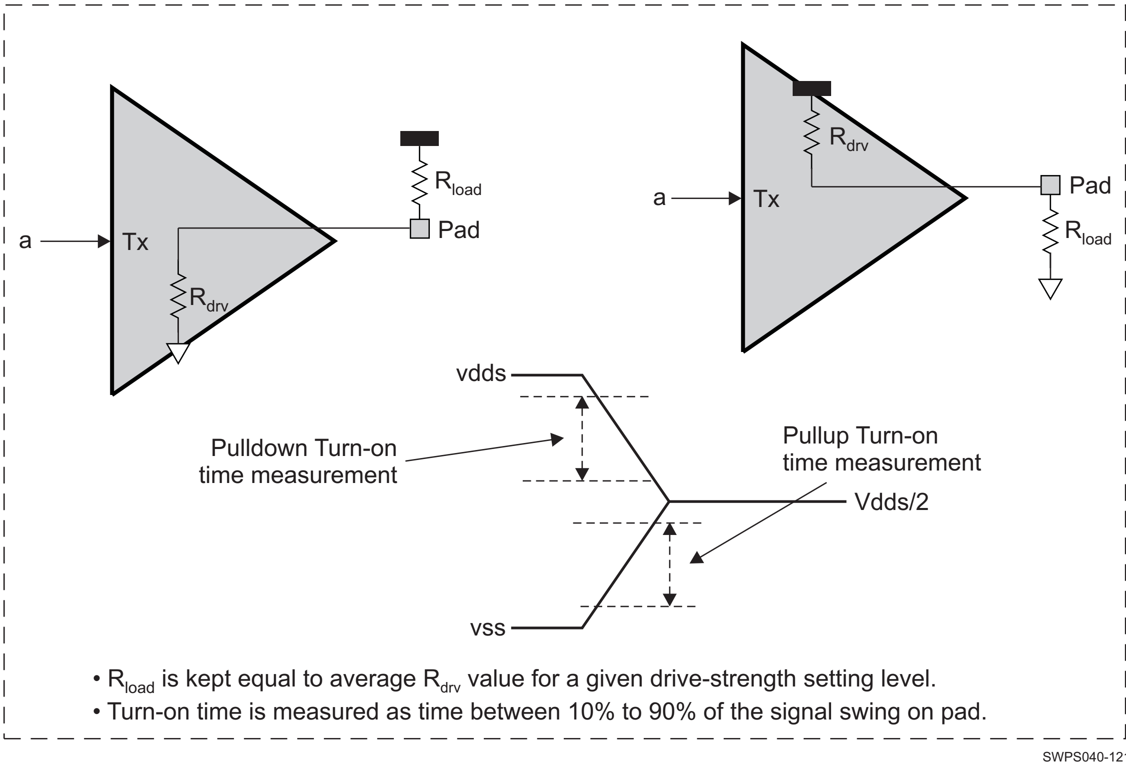

Figure 3-1. Output Turn-on Time Measurement

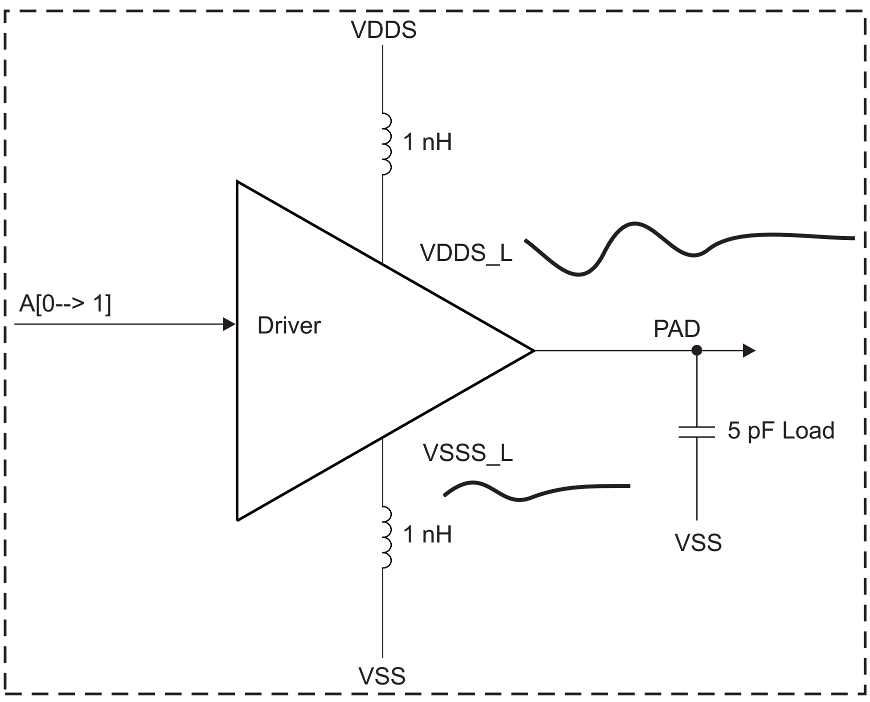

Figure 3-2. Output Supply Noise Measurement Setup(1)(2)

(1) Maximum supply noise = VDDS – minimum (VDDS_L – VSSS_L)
(2) 1 nH is used for a typical package inductance on the supplies.

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3.3.3 Camera DC Electrical Characteristics

Table 3-7 and Table 3-8 summarize the camera dc electrical characteristics in multiplexing mode 0.

Table 3-7. Camera CSI2 DC Electrical Characteristics

PARAMETER		MIN	TYP	MAX	UNIT
Signals in Mode 0: csi21_dx[4:0], csi21_dy[4:0], csi22_dx[1:0], csi22_dy[1:0] (**Bottom Balls**: R26 / R25 / T26 / T25 / U26 / U25 / V26 / V25 / W26 / W25 / M26 / M25 / N26 / N25)					
GPI Mode[13]					
V_{IH}	High-level input voltage	0.65 * vdda_y[10]		vdda_y[10] + 0.3	V
V_{IL}	Low-level input voltage	–0.3		0.35 * vdda_y[10]	V
V_{HYS}[11]	Hysteresis voltage at an input	0.15			V
C_{IN}	Input capacitance			2.0	pF
t_{TIN}[12]	Input transition time (t_{RIN} or t_{FIN} evaluated between 10% and 90% at PAD)			10	ns
MIPI D-PHY Mode Low-Power Receiver (LP-RX)					
V_{IH}	Input high-level voltage	880		1350	mV
V_{IL}	Input low-level voltage			550	mV
V_{ITH}[1]	Input high-level threshold			880	mV
V_{ITL}[2]	Input low-level threshold	550			mV
V_{HYS}[3]	Input hysteresis	25			mV
C_{IN}	Input capacitance			2.0	pF
MIPI D-PHY Mode Ultralow-Power Receiver (ULP-RX)					
V_{IH}	Input high-level voltage	880			mV
V_{IL}	Input low-level voltage			300	mV
V_{ITH}[1]	Input high-level threshold			880	mV
V_{ITL}[4]	Input low-level threshold	300			mV
V_{HYS}[3]	Input hysteresis	25			mV
C_{IN}	Input capacitance			2.0	pF
MIPI D-PHY Mode High-Speed Receiver (HS-RX)					
V_{IDTH}	Differential input high-level threshold	70			mV
V_{IDTL}	Differential input low-level threshold			–70	mV
V_{IDMAX}[7]	Maximum differential input voltage			270	mV
V_{IHHS}[5]	Single-ended input high voltage			460	mV
V_{ILHS}[5]	Single-ended input low voltage	–40			mV
V_{CMRXDC}[5][6]	Differential input common-mode voltage	70		330	mV
Z_{ID}	Differential input impedance	80	100	125	Ω
C_{IN}	Input capacitance			2.0	pF
CCP2 Mode (only on CSI2B)					
V_{CM}	Common mode input voltage range[8]	0.6	0.9	1.2	V
V_{OS}	Receiver input dc offset	–20		20	mV
V_{ID}	Receiver input differential amplitude	140	200	400	mV_{PP}
$\Delta V_{ID}/V_{ID}$	Amplitude mismatch between lane modules	–10%		10%	
ΔV_{CMRX}	Common mode mismatch between lane modules[8]	–100		100	mV
ΔV_{CMn}	Common mode noise ripple[9]	–15		15	mV
Z_{ID}	Differential input impedance	80	100	120	Ω
C_{IN}	Input capacitance			2.0	pF

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(1) V_{ITH} is the voltage at which the receiver is required to detect a high state in the input signal.

(2) V_{ITL} is the voltage at which the receiver is required to detect a low state in the input signal. V_{ITL} is larger than the maximum single-ended line high voltage during HS transmission. Therefore, both LP receivers will detect low during HS signaling.

(3) To reduce noise sensitivity on the received signal, the LP receiver is required to incorporate a hysteresis, V_{HYST}.

(4) V_{ITL} is the voltage at which the receiver is required to detect a low state in the input signal. Specification is relaxed for detecting 0 during Ultralow-Power (ULP) state. The LP receiver is not required to detect HS single-ended voltage as 0 in this state.

(5) Excluding possible additional RF interference of 200 mV_{PP} beyond 450 MHz.

(6) This value includes a ground difference of 50 mV between the transmitter and the receiver, the static common-mode level tolerance and variations below 450 MHz.

(7) This number is the transmitter V_{ODMAX}.

(8) Common mode is defined as the average voltage level of DX and DY: $V_{CM} = (V_{DX} + V_{DY})/2$.

(9) Common mode ripple may be due to rise-fall time and transmission line impairments in the PCB.

(10) In vdda_y, y can have the value csi21 or csi22 depending on the ball used. For more information of the power supply name and the corresponding pin, ball, see the POWER [9] column of Table 2-1.

(11) V_{HYS} is the magnitude of the difference between the positive-going threshold voltage V_{T+} and the negative-going threshold voltage V_{T-}.

(12) The t_{TIN} (t_{RIN} and t_{FIN} also) value is the recommended condition. The t_{TIN} (t_{RIN} and t_{FIN} also) mismatch causes additional delay time inside the device then leads to ac timing invalidation in this DM. The t_{TIN} (t_{RIN} and t_{FIN} also) mismatch does not necessarily mean functional failure. This global value may be overridden on a per basis if another value is explicitly defined for that in the Timing Requirements and Switching Characteristics Chapter of the data manual.

(13) The GPI mode is only available through multiplexing mode 3.

NOTE

For more information on the IO cell configurations (SC[1:0]), see the Control Module / Control Module Functional Description / Functional Register Description / Signal Integrity Parameter Control Registers With Pad Group Assignment section of the OMAP4430 TRM.

Table 3-8. Camera Control DC Electrical Characteristics

PARAMETER			MIN	NOM	MAX	UNIT
Signals in Mode 0: cam_shutter, cam_strobe, cam_globalreset (**Bottom Balls** : T27 / U27 / V27)						
C_{LOAD}	Load capacitance	SC[1:0] = 00	4		60	pF
		SC[1:0] = 01	2		21	
		SC[1:0] = 10	7		33	
t_{OT}	Output transition time (rise time, t_R or fall time, t_F) measured between 10% to 90% of PAD voltage, minimum at the minimum load and maximum at the maximum load	SC[1:0] = 00	1		15	ns
		SC[1:0] = 01	0.4		5	
		SC[1:0] = 10	0.6		7	
1.2-V Mode						
V_{IH}	Input high-level threshold		0.65 * vdds_dv_cam		vdds_dv_cam + 0.3	V
V_{IL}	Input low-level threshold		–0.3		0.35 * vdds_dv_cam	V
V_{HYS} (1)	Input hysteresis voltage		135			mV
V_{OH}	Output high-level threshold (I_{OH} = –4 mA)		0.75 * vdds_dv_cam			V
V_{OL}	Output low-level threshold (I_{OL} = 4 mA)				0.25 * vdds_dv_cam	V
1.8-V Mode						
V_{IH}	Input high-level threshold		0.65 * vdds_dv_cam		vdds_dv_cam + 0.3	V
V_{IL}	Input low-level threshold		–0.3		0.35 * vdds_dv_cam	V
V_{HYS} (1)	Input hysteresis voltage		150			mV
V_{OH}	Output high-level threshold (I_{OH} = –4 mA)		vdds_dv_cam – 0.45			V
V_{OL}	Output low-level threshold (I_{OL} = 4 mA)				0.45	V

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(1) V_{HYS} is the magnitude of the difference between the positive-going threshold voltage V_{T+} and the negative-going threshold voltage V_{T-}.

3.3.4 Display DC Electrical Characteristics

Table 3-9 summarizes the display dc electrical characteristics in multiplexing mode 0.

NOTE

For more information on HDMI, please contact your TI representative.

Table 3-9. Display DSI1 DC Electrical Characteristics

PARAMETER		MIN	NOM	MAX	UNIT
Signals in Mode 0: dsi1_dx[4:0], dsi1_dy[4:0], dsi2_dx[2:0], dsi2_dy[2:0] (**Bottom Balls**: P3 / P4 / N3 / N4 / M3 / M4 / L3 / L4 / K3 / K4 / T3 / T4 / U3 / U4 / V3 / V4)					
MIPI D-PHY—High-Speed Transmitter (HS-TX) mode					
$\|V_{OD}\|$(1)	High-speed transmit differential voltage	140	200	270	mV
V_{CMTX}(1)	High-speed transmit static common mode voltage	150	200	250	mV
$\|\Delta V_{OD}\|$	V_{OD} mismatch when output is differential-1 or differential-0			10	mV
$\|\Delta V_{CMTX(1,0)}\|$	V_{CMTX} mismatch when output is differential-1 or differential-0			5	mV
V_{OHHS}(1)	High-speed output high voltage			360	mV
Z_{OS}	Single-ended output impedance	40	50	62.5	Ω
ΔZ_{OS}	Single-ended output impedance mismatch			10%	
$\Delta V_{CMTX(HF)}$	Common-level variation above 450 MHz			15	mV_{RMS}
$\Delta V_{CMTX(LF)}$	Common-level variation between 50 MHz and 450 MHz	–50		50	mV_{PEAK}
t_{TOUT}	Output transition time (t_{ROUT} or t_{FOUT} evaluated between 20% and 80% of PAD voltage)	0.15			ns
				0.3	UI
MIPI D-PHY—Low-Power Transmitter (LP-TX) mode					
V_{OL}	Thevenin output low level	–50		50	mV
V_{OH}	Thevenin output high level	1.1	1.2	1.3	V
Z_{OLP}	Output impedance of LP transmitter	110			Ω
t_{TOUT}	Output transition time (t_{ROUT} or t_{FOUT} evaluated between 20% and 80% of PAD voltage)			25	ns
MIPI D-PHY—Low-Power Receiver (LP-RX) Mode					
V_{IH}	Input high-level voltage	880			mV
V_{IL}	Input low-level voltage			550	mV
V_{ITH}(2)	Input high-level threshold			880	mV
V_{ITL}(3)	Input low-level threshold	550			mV
V_{HYS}(4)	Input hysteresis	25			mV
MIPI D-PHY Mode Ultralow-Power Receiver (ULP-RX)					
V_{IH}	Input high-level voltage	880			mV
V_{IL}	Input low-level voltage			300	mV
V_{ITH}(2)	Input high-level threshold			880	mV
V_{ITL}(5)	Input low-level threshold	300			mV
V_{HYS}(4)	Input hysteresis	25			mV
MIPI D-PHY Mode Low Power Contention Detector (LPCD)					
V_{IHCD}	High-level input voltage	450			mV
V_{ILCD}	Low-level input voltage			200	mV

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(1) Value when driving into differential load impedance anywhere in the range of 80 to 125 Ω. See Chapter 8 of the MIPI D-PHY standard v1.0 for complete specification on the electrical characteristics. The PCB interconnect must be 50-Ω transmission line on DSI dsi1_dx[4;0], DSI dsi1_dy[4;0] and DSI dsi2_dx[2;0], DSI dsi2_dy[2;0]. These lines must be well matched. See Chapter 7 of the MIPI D-PHY standard v1.0 for complete specification of the Interconnect.

(2) V_{ITH} is the voltage at which the receiver is required to detect a high state in the input signal.

(3) V_{ITL} is the voltage at which the receiver is required to detect a low state in the input signal. V_{ITL} is larger than the maximum single-ended line high voltage during HS transmission. Therefore, both low-power receivers will detect low during high-speed signaling.

(4) V_{HYS} is the magnitude of the difference between the positive-going threshold voltage V_{T+} and the negative-going threshold voltage $V_{T–}$. Hysteresis feature is added on the low-power received signal to reduce noise sensitivity.

(5) V_{ITL} is the voltage at which the receiver is required to detect a low state in the input signal. Specification is relaxed for detecting 0 during Ultralow-Power (ULP) state. The low-power receiver is not required to detect high-speed, single-ended voltage as 0 in this state.

3.3.5 HDQ/1-Wire DC Electrical Characteristics

Table 3-10 summarizes the HDQ/1-Wire dc electrical characteristics in multiplexing mode 0.

NOTE

For more information on the IO cell configurations (SC[1:0]), see the Control Module / Control Module Functional Description / Functional Register Description / Signal Integrity Parameter Control Registers With Pad Group Assignment section of the OMAP4430 TRM.

Table 3-10. HDQ/1-Wire DC Electrical Characteristics

PARAMETER			MIN	NOM	MAX	UNIT
Signal in Mode 0: hdq_sio (**Bottom Ball**: AA29)						
C_{LOAD}	Load capacitance	SC[1:0] = 00	4		60	pF
		SC[1:0] = 01	2		21	
		SC[1:0] = 10	7		33	
t_{OT}	Output transition time (rise time, t_R or fall time, t_F) measured between 10% to 90% of PAD voltage, minimum at the minimum load and maximum at the maximum load	SC[1:0] = 00	1		15	ns
		SC[1:0] = 01	0.4		5	
		SC[1:0] = 10	0.6		7	
1.8-V Mode						
V_{IH}	Input high-level threshold		0.65 * vdds_1p8v		vdds_1p8v + 0.3	V
V_{IL}	Input low-level threshold		–0.3		0.35 * vdds_1p8v	V
V_{HYS}(1)	Input hysteresis voltage		150			mV
V_{OH}	Output high-level threshold (I_{OH} = –4 mA)		vdds_1p8v – 0.45			V
V_{OL}	Output low-level threshold (I_{OL} = 4 mA)				0.45	V

(1) V_{HYS} is the magnitude of the difference between the positive-going threshold voltage V_{T+} and the negative-going threshold voltage $V_{T–}$.

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3.3.6 I^2C DC Electrical Characteristics

Table 3-11 summarizes the I^2C dc electrical characteristics in multiplexing mode 0.

NOTE

For more information on the IO cell configurations (LB0[1:0]), see the Control Module / Control Module Functional Description / Functional Register Description / Signal Integrity Parameter Control Registers With Pad Group Assignment section of the OMAP4430 TRM.

Table 3-11. I^2C DC Electrical Characteristics

PARAMETER		MIN	NOM	MAX	UNIT
Signals in Mode 0: i2c[4:1]_scl, i2c[4:1]_sda, sr_scl, sr_sda (**Bottom Balls**: AE28 / AE26 / C26 / D26 / W27 / Y27 / AG21 / AH22 / AG9 / AF9)					
I^2C Standard Mode—1.2-V Mode and 1.8-V Mode					
V_{IH}	Input high-level threshold	0.7 * vdds_dv_y[2]		vdds_dv_y[2] + 0.5	V
V_{IL}	Input low-level threshold	–0.5		0.3 * vdds_dv_y[2]	V
I_I	Input current at each I/O pin with an input voltage between 0.1 * vdds_dv_y[2] to 0.9 * vdds_dv_y[2]	–10		10	µA
C_I	Input capacitance			10	pF
V_{OL3}	Output low-level threshold open-drain at 3-mA sink current	NA[1]		NA[1]	V
t_{OF}	Output fall time from V_{IHmin} to V_{ILmax} with a bus capacitance C_b from 5 pF to 400 pF			250	ns
t_{OR}	Output rise time from V_{ILmax} to V_{IHmin} with a capacitive load from 5 pF to 150 pF with internal pullup enabled	20 + 0.1*C_b		250	ns
I^2C Fast Mode—1.2-V Mode and 1.8-V Mode					
V_{IH}	Input high-level threshold	0.7 * vdds_dv_y[2]		vdds_dv_y[2] + 0.5	V
V_{IL}	Input low-level threshold	–0.5		0.3 * vdds_dv_y[2]	V
I_I	Input current at each I/O pin with an input voltage between 0.1 * vdds_dv_y[2] to 0.9 * vdds_dv_y[2]	–10		10	µA
C_I	Input capacitance			10	pF
V_{OL3}	Output low-level threshold open-drain at 3-mA sink current	0		0.2 * vdds_dv_y[2]	V
t_{OF}	Output fall time from V_{IHmin} to V_{ILmax} with a bus capacitance C_b from 5 pF to 400 pF	20 + 0.1*C_b		250	ns
t_{OR}	Output rise time from V_{ILmax} to V_{IHmin} with a capacitive load from 5 pF to 150 pF with internal pullup enabled	20 + 0.1*C_b		250	ns
R_{INPU}	Internal pullup resistance for a given load range: LB[1:0] = 00	3.42	4.5 (for a load in the range of 5 pF to 15 pF)	6.8	kΩ
	LB[1:0] = 01	1.6	2.1 (for a load in the range of 15 pF to 50 pF)	3.17	
	LB[1:0] = 10	0.65	0.86 (for a load in the range of 50 pF to 150 pF)	1.3	
	LB[1:0] = 11	NA	NA	NA	
I^2C High-Speed Mode—1.2-V Mode and 1.8-V Mode					
V_{IH}	Input high-level threshold	0.7 * vdds_dv_y[2]		vdds_dv_y[2] + 0.5	V
V_{IL}	Input low-level threshold	–0.5		0.3 * vdds_dv_y[2]	V
I_I	Input current at each I/O pin with an input voltage between 0.1 * vdds_dv_y[2] to 0.9 * vdds_dv_y[2]	–10		10	µA

Table 3-11. I^2C DC Electrical Characteristics (continued)

PARAMETER			MIN	NOM	MAX	UNIT
C_I	Input capacitance				10	pF
V_{OL3}	Output low-level threshold open-drain at 3-mA sink current		0		0.2 * vdds_dv_y(2)	V
t_{OF}	Output fall time from V_{IHmin} to V_{ILmax} with a capacitive load from 5 pF to 100 pF at 3-mA sink current		10		40	ns
	Output fall time from V_{IHmin} to V_{ILmax} with a capacitive load of 400 pF at 3-mA sink current		20		80	ns
t_{OR}	Output rise time from V_{ILmax} to V_{IHmin} with a capacitive load from 5 pF to 80 pF with internal pullup enabled		10		40	ns
R_{INPU}	Internal pullup resistance for a given load range	LB[1:0] = 00	1.26	1.66 (for a load in the range of 5 pF to 12 pF)	2.5	kΩ
		LB[1:0] = 01	0.7	0.92 (for a load in the range of 12 pF to 25 pF)	1.39	
		LB[1:0] = 10	0.38	0.5 (for a load in the range of 25 pF to 50 pF)	0.75	
		LB[1:0] = 11	0.23	0.3 (for a load in the range of 50 pF to 80 pF)	0.45	
Non-I^2C Mode (Standard LVCMOS mode)						
1.2-V Mode						
V_{IH}	Input high-level threshold		0.7 * vdds_dv_y(2)		vdds_dv_y(2) + 0.5	V
V_{IL}	Input low-level threshold		–0.5		0.3 * vdds_dv_y(2)	V
I_I	Input current at each I/O pin with an input voltage between 0.1 * vdds_dv_y(2) to 0.9 * vdds_dv_y(2)		–10		10	µA
C_I	Input capacitance				10	pF
V_{OH}	Output high-level threshold at 4-mA sink current (I_{OL} = 4 mA)		0.75 * vdds_dv_y(2)			V
V_{OL}	Output low-level threshold at 4-mA sink current (I_{OL} = 4 mA)				0.25 * vdds_dv_y(2)	V
t_{OT}	Output transition time (rise time, t_R or fall time, t_F) at 40 pF load, measured between 10% to 90% PAD voltage				10	ns
1.8-V Mode						
V_{IH}	Input high-level threshold		0.7 * vdds_dv_y(2)		vdds_dv_y(2) + 0.5	V
V_{IL}	Input low-level threshold		–0.5		0.3 * vdds_dv_y(2)	V
I_I	Input current at each I/O pin with an input voltage between 0.1 * vdds_dv_y(2) to 0.9 * vdds_dv_y(2)		–10		10	µA
C_I	Input capacitance				10	pF
V_{OH}	Output high-level threshold at 4-mA sink current (I_{OL} = 4 mA)		vdds_dv_y(2) – 0.45			V
V_{OL}	Output low-level threshold at 4-mA sink current (I_{OL} = 4 mA)				0.45	V
t_{OT}	Output transition time (rise time, t_R or fall time, t_F) at 40 pF load, measured between 10% to 90% of PAD voltage				10	ns

(1) V_{OL} specification is not applicable in the Standard mode.

(2) In vdds_dv_y, y can have the value: bank2, bank5, 1p8v, cam depending on the ball used. For more information on a ball and the corresponding power, see Table 2-1, POWER [9] column.

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3.3.7 Audio McBSP / PDM / DMIC DC Electrical Characteristics

Table 3-12 summarizes the audio McBSP / PDM / DMIC dc electrical characteristics in multiplexing mode 0.

NOTE

For more information on the IO cell configurations (MB[1:0] and LB0, SC[1:0]), see the Control Module / Control Module Functional Description / Functional Register Description / Signal Integrity Parameter Control Registers With Pad Group Assignment section of the OMAP4430 TRM.

Table 3-12. Audio McBSP / PDM / DMIC DC Electrical Characteristics

PARAMETER			MIN	NOM	MAX	UNIT
Signals in Mode 0: abe_mcbsp2_clkx, abe_mcbsp2_dr, abe_mcbsp2_dx, abe_mcbsp2_fsx, abe_mcbsp1_clkx, abe_mcbsp1_dr, abe_mcbsp1_dx, abe_mcbsp1_fsx, abe_pdm_ul_data, abe_pdm_dl_data, abe_pdm_frame, abe_pdm_lb_clk, abe_dmic_clk1, abe_dmic_din[3:1] (**Bottom Balls**: AD27 / AD26 / AD25 / AC28 / AC26 / AC25 / AB25 / AC27 / AG25 / AF25 / AE25 / AF26 / AE24 / AF24 / AG24 / AH24) (5)						
C_{LOAD}(4)	Load capacitance	MB[1:0] = 11 LB0 = 1 (Mode1) maximum frequency = 24 MHz transmission line delay = 670 ps	20		25	pF
		MB[1:0] = 11 LB0 = 1 (Mode1) maximum frequency = 60 MHz transmission line delay = 335 ps	2		5	
		MB[1:0] = 01 LB0 = 0 (Mode2) maximum frequency = 25 MHz transmission line delay = 335 ps	14		17	
		MB[1:0] = 01 LB0 = 0 (Mode2) maximum frequency = 48 MHz transmission line delay = 536 ps	2		5	
		MB[1:0] = 10 LB0 = 1 (Mode3) maximum frequency = 20 MHz transmission line delay = 838 ps	23		28	
		MB[1:0] = 10 LB0 = 1 (Mode3) maximum frequency = 24 MHz transmission line delay = 670 ps	16		20	
		MB[1:0] = 10 LB0 = 0 (Mode4) maximum frequency = 4 MHz transmission line delay = 1675 ps	16		20	
		MB[1:0] = 10 LB0 = 0 (Mode4) maximum frequency = 25 MHz transmission line delay = 670 ps	2		5	
		MB[1:0] = 10 LB0 = 0 (Mode4) maximum frequency = 25 MHz transmission line delay = 670 ps	5		7	
		MB[1:0] = 10 LB0 = 0 (Mode4) maximum frequency = 25 MHz transmission line delay = 536 ps	2		11	

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Table 3-12. Audio McBSP / PDM / DMIC DC Electrical Characteristics (continued)

PARAMETER			MIN	NOM	MAX	UNIT
t_{OT}[4]	Output transition time (rise time, t_R or fall time, t_F) measured between 10% to 90% of PAD voltage, the maximum at maximum load	MB[1:0] = 11 LB0 = 1 (Mode1) maximum frequency = 24 MHz transmission line delay = 670 ps			10	ns
		MB[1:0] = 11 LB0 = 1 (Mode1) maximum frequency = 60 MHz transmission line delay = 335 ps			4	
		MB[1:0] = 01 LB0 = 0 (Mode2) maximum frequency = 25 MHz transmission line delay = 335 ps			5.6[1]	
		MB[1:0] = 01 LB0 = 0 (Mode2) maximum frequency = 48 MHz transmission line delay = 536 ps			6.3	
		MB[1:0] = 10 LB0 = 1 (Mode3) maximum frequency = 20 MHz transmission line delay = 838 ps			10.5[1]	
		MB[1:0] = 10 LB0 = 1 (Mode3) maximum frequency = 24 MHz transmission line delay = 670 ps			12.5	
		MB[1:0] = 10 LB0 = 0 (Mode4) maximum frequency = 4 MHz transmission line delay = 1675 ps			16.8[1]	
		MB[1:0] = 10 LB0 = 0 (Mode4) maximum frequency = 25 MHz transmission line delay = 670 ps			10	
		MB[1:0] = 10 LB0 = 0 (Mode4) maximum frequency = 25 MHz transmission line delay = 670 ps			12.2	
		MB[1:0] = 10 LB0 = 0 (Mode4) maximum frequency = 25 MHz transmission line delay = 536 ps			8[1]	
1.2-V Mode						
V_{IH}	Input high-level threshold		0.65 * vdds_dv_y[2]		vdds_dv_y[2] + 0.3	V
V_{IL}	Input low-level threshold		–0.3		0.35 * vdds_dv_y[2]	V
V_{HYS}[3]	Input hysteresis voltage		135			mV
V_{OH}	Output high-level threshold (I_{OH} = 4 mA)		0.75 * vdds_dv_y[2]			V
V_{OL}	Output low-level threshold (I_{OL} = 4 mA)				0.25 * vdds_dv_y[2]	V
1.8-V Mode						
V_{IH}	Input high-level threshold		0.65 * vdds_dv_y[2]		vdds_dv_y[2] + 0.3	V
V_{IL}	Input low-level threshold		–0.3		0.35 * vdds_dv_y[2]	V
V_{HYS}[3]	Input hysteresis voltage		150			mV
V_{OH}	Output high-level threshold (I_{OH} = 4 mA)		vdds_dv_y[2] – 0.45			V
V_{OL}	Output low-level threshold (I_{OL} = 4 mA)				0.45	V
Signal in Mode 0: abe_clks (**Bottom Ball**: AH26)[5]						
C_{LOAD}	Load capacitance	SC[1:0] = 00	4		60	pF
		SC[1:0] = 01	2		21	
		SC[1:0] = 10	7		33	
t_{OT}	Output transition time (rise time, t_R or fall time, t_F) measured between 10% to 90% of PAD voltage, minimum at the minimum load and maximum at the maximum load	SC[1:0] = 00	1		15	ns
		SC[1:0] = 01	0.4		5	
		SC[1:0] = 10	0.6		7	
1.2-V Mode						
V_{IH}	Input high-level threshold		0.65 * vdds_dv_bank2		vdds_dv_bank2 + 0.3	V
V_{IL}	Input low-level threshold		–0.3		0.35 * vdds_dv_bank2	V
V_{HYS}[3]	Input hysteresis voltage		135			mV

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Table 3-12. Audio McBSP / PDM / DMIC DC Electrical Characteristics (continued)

PARAMETER		MIN	NOM	MAX	UNIT
V_{OH}	Output high-level threshold (I_{OH} = –4 mA)	0.75 * vdds_dv_bank2			V
V_{OL}	Output low-level threshold (I_{OL} = 4 mA)			0.25 * vdds_dv_bank2	V
1.8-V Mode					
V_{IH}	Input high-level threshold	0.65 * vdds_dv_bank2		vdds_dv_bank2 + 0.3	V
V_{IL}	Input low-level threshold	–0.3		0.35 * vdds_dv_bank2	V
V_{HYS}(3)	Input hysteresis voltage	150			mV
V_{OH}	Output high-level threshold (I_{OH} = –4 mA)	vdds_dv_bank2 – 0.45			V
V_{OL}	Output low-level threshold (I_{OL} = 4 mA)			0.45	V

(1) Output transition time measured between 20% to 80% of PAD voltage.

(2) In vdds_dv_y, y can have the value: bank1 or bank2 depending on the ball used. For more information on a ball and the corresponding power, see Table 2-1, POWER [9] column.

(3) V_{HYS} is the magnitude of the difference between the positive-going threshold voltage V_{T+} and the negative-going threshold voltage V_{T-}.

(4) Depending on the programming mode, different output load and transition time are available following the targeted maximum frequency, transmission line or output transition time.

(5) The following signals abe_mcbsp2_clkx, abe_mcbsp2_dr, abe_mcbsp2_dx, abe_mcbsp2_fsx, abe_mcbsp1_clkx, abe_mcbsp1_dr, abe_mcbsp1_dx, abe_mcbsp1_fsx, abe_pdm_ul_data, abe_pdm_dl_data, abe_pdm_frame, abe_pdm_lb_clk, abe_dmic_clk1, abe_dmic_din[3:1], abe_clks (bottom balls: AD27 / AD26 / AD25 / AC28 / AC26 / AC25 / AB25 / AC27 / AG25 / AF25 / AE25 / AF26 / AE24 / AF24 / AG24 / AH24 / AH26) are compliant with the JEDEC standard for the following parameters: V_{OL} = 0.2 V and V_{OH} = VDDS – 0.2 V when absolute value of I_{OH} / I_{OL} = 100 µA.

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3.3.8 McSPI DC Electrical Characteristics

Table 3-13 summarizes the McSPI dc electrical characteristics in multiplexing mode 0.

NOTE

For more information on the IO cell configurations (MB[1:0] and LB0, SC[1:0]), see the Control Module / Control Module Functional Description / Functional Register Description / Signal Integrity Parameter Control Registers With Pad Group Assignment section of the OMAP4430 TRM.

Table 3-13. McSPI DC Electrical Characteristics

PARAMETER			MIN	NOM	MAX	UNIT
Signals in Mode 0: mcspi1_clk, mcspi1_somi, mcspi1_simo, mcspi1_cs[1:0] (**Bottom Balls**: AF22 / AE22 / AG22 / AE23 / AF23)						
C_{LOAD}	Load capacitance	SC[1:0] = 00	4		60	pF
		SC[1:0] = 01	2		21	
		SC[1:0] = 10	7		33	
t_{OT}	Output transition time (rise time, t_R or fall time, t_F) measured between 10% to 90% of PAD voltage, minimum at the minimum load and maximum at the maximum load	SC[1:0] = 00	1		15	ns
		SC[1:0] = 01	0.4		5	
		SC[1:0] = 10	0.6		7	
1.2-V Mode						
V_{IH}	Input high-level threshold		0.65 * vdds_dv_bank3		vdds_dv_bank3 + 0.3	V
V_{IL}	Input low-level threshold		–0.3		0.35 * vdds_dv_bank3	V
V_{HYS}(3)	Input hysteresis voltage		135			mV
V_{OH}	Output high-level threshold (I_{OH} = –4 mA)		0.75 * vdds_dv_bank3			V
V_{OL}	Output low-level threshold (I_{OL} = 4 mA)				0.25 * vdds_dv_bank3	V
1.8-V Mode						
V_{IH}	Input high-level threshold		0.65 * vdds_dv_bank3		vdds_dv_bank3 + 0.3	V
V_{IL}	Input low-level threshold		–0.3		0.35 * vdds_dv_bank3	V

Table 3-13. McSPI DC Electrical Characteristics (continued)

PARAMETER			MIN	NOM	MAX	UNIT
V_{HYS}[3]	Input hysteresis voltage		150			mV
V_{OH}	Output high-level threshold (I_{OH} = –4 mA)		vdds_dv_bank3 – 0.45			V
V_{OL}	Output low-level threshold (I_{OL} = 4 mA)				0.45	V
Signals in Mode 0: mcspi1_cs[3:2], mcspi4_clk, mcspi4_simo, mcspi4_somi, mcspi4_cs0 (**Bottom Balls**: AG23 / AH23 / AE21 / AF20 / AF21 / AE20)						
C_{LOAD}[4]	Load capacitance	MB[1:0] = 11 LB0 = 1 (Mode1) maximum frequency = 24 MHz transmission line delay = 670 ps	20		25	pF
		MB[1:0] = 11 LB0 = 1 (Mode1) maximum frequency = 60 MHz transmission line delay = 335 ps	2		5	
		MB[1:0] = 01 LB0 = 0 (Mode2) maximum frequency = 25 MHz transmission line delay = 335 ps	14		17	
		MB[1:0] = 01 LB0 = 0 (Mode2) maximum frequency = 48 MHz transmission line delay = 536 ps	2		5	
		MB[1:0] = 10 LB0 = 1 (Mode3) maximum frequency = 20 MHz transmission line delay = 838 ps	23		28	
		MB[1:0] = 10 LB0 = 1 (Mode3) maximum frequency = 24 MHz transmission line delay = 670 ps	16		20	
		MB[1:0] = 10 LB0 = 0 (Mode4) maximum frequency = 4 MHz transmission line delay = 1675 ps	16		20	
		MB[1:0] = 10 LB0 = 0 (Mode4) maximum frequency = 25 MHz transmission line delay = 670 ps	2		5	
		MB[1:0] = 10 LB0 = 0 (Mode4) maximum frequency = 25 MHz transmission line delay = 670 ps	5		7	
		MB[1:0] = 10 LB0 = 0 (Mode4) maximum frequency = 25 MHz transmission line delay = 536 ps	2		11	

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Table 3-13. McSPI DC Electrical Characteristics (continued)

PARAMETER			MIN	NOM	MAX	UNIT
t_{OT}[4]	Output transition time (rise time, t_R or fall time, t_F) measured between 10% to 90% of PAD voltage, the maximum at the maximum load	MB[1:0] = 11 LB0 = 1 (Mode1) maximum frequency = 24 MHz transmission line delay = 670 ps			10	ns
		MB[1:0] = 11 LB0 = 1 (Mode1) maximum frequency = 60 MHz transmission line delay = 335 ps			4	
		MB[1:0] = 01 LB0 = 0 (Mode2) maximum frequency = 25 MHz transmission line delay = 335 ps			5.6[1]	
		MB[1:0] = 01 LB0 = 0 (Mode2) maximum frequency = 48 MHz transmission line delay = 536 ps			6.3	
		MB[1:0] = 10 LB0 = 1 (Mode3) maximum frequency = 20 MHz transmission line delay = 838 ps			10.5[1]	
		MB[1:0] = 10 LB0 = 1 (Mode3) maximum frequency = 24 MHz transmission line delay = 670 ps			12.5	
		MB[1:0] = 10 LB0 = 0 (Mode4) maximum frequency = 4 MHz transmission line delay = 1675 ps			16.8[1]	
		MB[1:0] = 10 LB0 = 0 (Mode4) maximum frequency = 25 MHz transmission line delay = 670 ps			10	
		MB[1:0] = 10 LB0 = 0 (Mode4) maximum frequency = 25 MHz transmission line delay = 670 ps			12.2	
		MB[1:0] = 10 LB0 = 0 (Mode4) maximum frequency = 25 MHz transmission line delay = 536 ps			8[1]	
1.2-V Mode						
V_{IH}	Input high-level threshold		0.65 * vdds_dv_y[2]		vdds_dv_y[2] + 0.3	V
V_{IL}	Input low-level threshold		–0.3		0.35 * vdds_dv_y[2]	V
V_{HYS}[3]	Input hysteresis voltage		135			mV
V_{OH}	Output high-level threshold (I_{OH} = 4 mA)		0.75 * vdds_dv_y[2]			V
V_{OL}	Output low-level threshold (I_{OL} = 4 mA)				0.25 * vdds_dv_y[2]	V
1.8-V Mode						
V_{IH}	Input high-level threshold		0.65 * vdds_dv_y[2]		vdds_dv_y[2] + 0.3	V
V_{IL}	Input low-level threshold		–0.3		0.35 * vdds_dv_y[2]	V
V_{HYS}[3]	Input hysteresis voltage		150			mV
V_{OH}	Output high-level threshold (I_{OH} = 4 mA)		vdds_dv_y[2] – 0.45			V
V_{OL}	Output low-level threshold (I_{OL} = 4 mA)				0.45	V

(1) Output transition time measured between 20% to 80% of PAD voltage.

(2) In vdds_dv_y, y can have the value: bank3 or bank5 depending on the ball used. For more information on a ball and the corresponding power, see Table 2-1, POWER [9] column.

(3) V_{HYS} is the magnitude of the difference between the positive-going threshold voltage V_{T+} and the negative-going threshold voltage V_{T-}.

(4) Depending on the programming mode, different output load and transition time are available following the targeted maximum frequency, transmission line or output transition time.

3.3.9 UART DC Electrical Characteristics

Table 3-14 summarizes the UART dc electrical characteristics in multiplexing mode 0.

NOTE

For more information on the IO cell configurations (MB[1:0] and LB0, SC[1:0]), see the Control Module / Control Module Functional Description / Functional Register Description / Signal Integrity Parameter Control Registers With Pad Group Assignment section of the OMAP4430 TRM.

Table 3-14. UART DC Electrical Characteristics

PARAMETER			MIN	NOM	MAX	UNIT
Signals in Mode 0: uart3_cts_rctx, uart3_rts_sd, uart3_rx_irrx, uart3_tx_irtx (**Bottom Balls**: F27 / F28 / G27 / G28)						
C_{LOAD}	Load capacitance	SC[1:0] = 00	4		60	pF
		SC[1:0] = 01	2		21	
		SC[1:0] = 10	7		33	
t_{OT}	Output transition time (rise time, t_R or fall time, t_F) measured between 10% to 90% of PAD voltage, minimum at the minimum load and maximum at the maximum load	SC[1:0] = 00	1		15	ns
		SC[1:0] = 01	0.4		5	
		SC[1:0] = 10	0.6		7	
1.8-V Mode						
V_{IH}	Input high-level threshold		0.65 * vdds_1p8v		vdds_1p8v + 0.3	V
V_{IL}	Input low-level threshold		–0.3		0.35 * vdds_1p8v	V
V_{HYS}(3)	Input hysteresis voltage		150			mV
V_{OH}	Output high-level threshold (I_{OH} = –4 mA)		vdds_1p8v – 0.45			V
V_{OL}	Output low-level threshold (I_{OL} = 4 mA)				0.45	V

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Table 3-14. UART DC Electrical Characteristics (continued)

PARAMETER			MIN	NOM	MAX	UNIT
Signals in Mode 0: uart2_cts, uart2_rts, uart2_rx, uart2_tx, uart4_rx, uart4_tx (**Bottom Balls**: AB26 / AB27 / AA25 / AA26 / AG20 / AH19)						
C_{LOAD} (4)	Load capacitance	MB[1:0] = 11 LB0 = 1 (Mode1) maximum frequency = 24 MHz transmission line delay = 670 ps	20		25	pF
		MB[1:0] = 11 LB0 = 1 (Mode1) maximum frequency = 60 MHz transmission line delay = 335 ps	2		5	
		MB[1:0] = 01 LB0 = 0 (Mode2) maximum frequency = 25 MHz transmission line delay = 335 ps	14		17	
		MB[1:0] = 01 LB0 = 0 (Mode2) maximum frequency = 48 MHz transmission line delay = 536 ps	2		5	
		MB[1:0] = 10 LB0 = 1 (Mode3) maximum frequency = 20 MHz transmission line delay = 838 ps	23		28	
		MB[1:0] = 10 LB0 = 1 (Mode3) maximum frequency = 24 MHz transmission line delay = 670 ps	16		20	
		MB[1:0] = 10 LB0 = 0 (Mode4) maximum frequency = 4 MHz transmission line delay = 1675 ps	16		20	
		MB[1:0] = 10 LB0 = 0 (Mode4) maximum frequency = 25 MHz transmission line delay = 670 ps	2		5	
		MB[1:0] = 10 LB0 = 0 (Mode4) maximum frequency = 25 MHz transmission line delay = 670 ps	5		7	
		MB[1:0] = 10 LB0 = 0 (Mode4) maximum frequency = 25 MHz transmission line delay = 536 ps	2		11	

Table 3-14. UART DC Electrical Characteristics (continued)

PARAMETER			MIN	NOM	MAX	UNIT
t_{OT}[4]	Output transition time (rise time, t_R or fall time, t_F) measured between 10% to 90% of PAD voltage, the maximum at the maximum load	MB[1:0] = 11 LB0 = 1 (Mode1) maximum frequency = 24 MHz transmission line delay = 670 ps			10	ns
		MB[1:0] = 11 LB0 = 1 (Mode1) maximum frequency = 60 MHz transmission line delay = 335 ps			4	
		MB[1:0] = 01 LB0 = 0 (Mode2) maximum frequency = 25 MHz transmission line delay = 335 ps			5.6[1]	
		MB[1:0] = 01 LB0 = 0 (Mode2) maximum frequency = 48 MHz transmission line delay = 536 ps			6.3	
		MB[1:0] = 10 LB0 = 1 (Mode3) maximum frequency = 20 MHz transmission line delay = 838 ps			10.5[1]	
		MB[1:0] = 10 LB0 = 1 (Mode3) maximum frequency = 24 MHz transmission line delay = 670 ps			12.5	
		MB[1:0] = 10 LB0 = 0 (Mode4) maximum frequency = 4 MHz transmission line delay = 1675 ps			16.8[1]	
		MB[1:0] = 10 LB0 = 0 (Mode4) maximum frequency = 25 MHz transmission line delay = 670 ps			10	
		MB[1:0] = 10 LB0 = 0 (Mode4) maximum frequency = 25 MHz transmission line delay = 670 ps			12.2	
		MB[1:0] = 10 LB0 = 0 (Mode4) maximum frequency = 25 MHz transmission line delay = 536 ps			8[1]	
1.2-V Mode						
V_{IH}	Input high-level threshold		0.65 * vdds_dv_y[2]		vdds_dv_y[2] + 0.3	V
V_{IL}	Input low-level threshold		–0.3		0.35 * vdds_dv_y[2]	V
V_{HYS}[3]	Input hysteresis voltage		135			mV
V_{OH}	Output high-level threshold (I_{OH} = 2 mA)[6]		0.75 * vdds_dv_y[2]			V
V_{OL}	Output low-level threshold (I_{OL} = 2 mA)[6]				0.25 * vdds_dv_y[2]	V
1.8-V Mode						
V_{IH}	Input high-level threshold		0.65 * vdds_dv_y[2]		vdds_dv_y[2] + 0.3	V
V_{IL}	Input low-level threshold		–0.3		0.35 * vdds_dv_y[2]	V
V_{HYS}[3]	Input hysteresis voltage		150			mV
V_{OH}	Output high-level threshold (I_{OH} = 2 mA)[6]		vdds_dv_y[2] – 0.45[5]			V
V_{OL}	Output low-level threshold (I_{OL} = 2 mA)[6]				0.45[5]	V

(1) Output transition time measured between 20% to 80% of PAD voltage.

(2) In vdds_dv_y, y can have the value: bank1 or bank5 depending on the ball used. For more information on a ball and the corresponding power, see Table 2-1, POWER [9] column.

(3) V_{HYS} is the magnitude of the difference between the positive-going threshold voltage V_{T+} and the negative-going threshold voltage V_{T-}.

(4) Depending on the programming mode, different output load and transition time are available following the targeted maximum frequency, transmission line or output transition time.

(5) For uart4_rx ball (AG20) and uart4_tx ball (AH19):
V_{OH} = vdds_dv_y – 0.3 V and V_{OL} = 0.3 V for I_{OH} = 1 mA
V_{OH} = vdds_dv_y – 0.2 V and V_{OL} = 0.2 V for I_{OL} = 250 µA

(6) This IO buffer supports up to 4 mA of drive strength. For this drive strength, the V_{OL}/V_{OH} described in the table above are not assured.

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3.3.10 USB DC Electrical Characteristics

Table 3-15 summarizes the USB dc electrical characteristics in multiplexing mode 0.

NOTE

For more information on the IO cell configurations (DS0, MB[1:0], i[2:0], sr[1:0], SPEEDCTRL), see the Control Module / Control Module Functional Description / Functional Register Description / Signal Integrity Parameter Control Registers With Pad Group Assignment section of the OMAP4430 TRM.

Table 3-15. USB DC Electrical Characteristics

PARAMETER			MIN	NOM	MAX	UNIT
Signals in Mode 0: usbb1_ulpitll_clk, usbb2_ulpitll_clk (**Bottom Balls**: AE18 / AG12)						
C_{LOAD}	Load capacitance	DS0 = 0 (Mode2) maximum frequency = 20 MHz transmission line delay = 1340 ps	5		35	pF
		DS0 = 0 (Mode2) maximum frequency = 48 MHz transmission line delay = 670 ps	2		5	
		DS0 = 0 (Mode2) maximum frequency = 60 MHz transmission line delay = 335 ps	2		5	
		DS0 = 0 (Mode2) maximum frequency = 75 MHz transmission line delay = 402 ps	2		5	
		DS0 = 1 (Mode1) maximum frequency = 100 MHz transmission line delay = 203 ps	2		5	
t_{OT}	Output transition time (rise time, t_R or fall time, t_F), the maximum at the maximum load	DS0 = 0 (Mode2) maximum frequency = 20 MHz transmission line delay = 1340 ps			15(1)	ns
		DS0 = 0 (Mode2) maximum frequency = 48 MHz transmission line delay = 670 ps			3(1)	
		DS0 = 0 (Mode2) maximum frequency = 60 MHz transmission line delay = 335 ps			3(2)	
		DS0 = 0 (Mode2) maximum frequency = 75 MHz transmission line delay = 402 ps			4(3)	
		DS0 = 1 (Mode1) maximum frequency = 100 MHz transmission line delay = 203 ps			2(3)	
1.2-V Mode						
V_{IH}	Input high-level threshold		0.65 * vdds_dv_y(4)		vdds_dv_y(4) + 0.3	V
V_{IL}	Input low-level threshold		–0.3		0.35 * vdds_dv_y(4)	V
V_{HYS}(11)	Input hysteresis voltage		60			mV
V_{OH}	Output high-level threshold (I_{OH} = 4 mA for 50Ω mode, I_{OH} = 8 mA for 25Ω mode)		0.75 * vdds_dv_y(4)			V
V_{OL}	Output low-level threshold (I_{OL} = 4 mA for 50Ω mode, I_{OL} = 8 mA for 25Ω mode)				0.25 * vdds_dv_y(4)	V
1.8-V Mode						
V_{IH}	Input high-level threshold		0.65 * vdds_dv_y(4)		vdds_dv_y(4) + 0.3	V
V_{IL}	Input low-level threshold		–0.3		0.35 * vdds_dv_y(4)	V
V_{HYS}(11)	Input hysteresis voltage		70			mV

Table 3-15. USB DC Electrical Characteristics (continued)

PARAMETER			MIN	NOM	MAX	UNIT
V_{OH}	Output high-level threshold (I_{OH} = 4 mA for 50Ω mode, I_{OH} = 8 mA for 25Ω mode)		vdds_dv_y[(4)] – 0.45			V
V_{OL}	Output low-level threshold (I_{OL} = 4 mA for 50Ω mode, I_{OL} = 8 mA for 25Ω mode)				0.45	V
Signals in Mode 0: usbb1_ulpitll_stp, usbb1_ulpitll_dir, usbb1_ulpitll_nxt, usbb1_ulpitll_dat[7:0] (**Bottom Balls**: AG19 / AF19 / AE19 / AF18 / AG18 / AE17 / AF17 / AH17 / AE16 / AF16 / AG16)						
C_{LOAD}	Load capacitance	MB[1:0] = 01 (Mode1) maximum frequency = 48 MHz	2		10	pF
		MB[1:0] = 10 (Mode2) maximum frequency = 4 MHz	5		35	
		MB[1:0] = 11 (Mode3) maximum frequency = 200 MHz	3		5	
		MB[1:0] = 11 (Mode4) maximum frequency = 60 MHz	2		5	
t_{OT}	Output transition time (rise time, t_R or fall time, t_F) measured between 10% to 90% of PAD voltage, minimum at minimum load and minimum transmission line length and maximum at maximum load	MB[1:0] = 01 (Mode1) maximum frequency = 48 MHz	1.2		5.2	ns
		MB[1:0] = 10 (Mode2) maximum frequency = 4 MHz	1.35		10.6	
		MB[1:0] = 11 (Mode3) maximum frequency = 200 MHz	0.6		1.2	
		MB[1:0] = 11 (Mode4) maximum frequency = 60 MHz	1.2		3.4	
1.8-V Mode						
V_{IH}	Input high-level threshold		0.65*vdds_dv_bank0		vdds_dv_bank0 + 0.3	V
V_{IL}	Input low-level threshold		–0.3		0.35 * vdds_dv_bank0	V
V_{HYS}[(11)]	Input hysteresis voltage		150			mV
V_{OH}	Output high-level threshold (I_{OH} = –6 mA)		vdd – 0.45			V
V_{OL}	Output low-level threshold (I_{OL} = 6 mA)				0.45	V
1.2-V Mode						
V_{IH}	High-level input threshold		0.65*vdds_dv_bank0		vdds_dv_bank0 + 0.3	V
V_{IL}	Low-level input threshold		–0.3		0.35 * vdds_dv_bank0	V
V_{HYS}[(11)]	Input hysteresis voltage		135			mV
V_{OH}	High-level output threshold (I_{OH} = 6 mA)		0.75*vdds_dv_bank0			V
V_{OL}	Low-level output threshold (I_{OL} = 6 mA)				0.25 * vdds_dv_bank0	V
Signals in Mode 0: usbb2_ulpitll_stp, usbb2_ulpitll_dir, usbb2_ulpitll_nxt, usbb2_ulpitll_dat[7:0] (**Bottom Balls**: AF12 / AE12 / AG13 / AE11 / AF11 / AG11 / AH11 / AE10 / AF10 / AG10 / AE9)						
C_{LOAD}	Load capacitance	DS0 = 0 (Mode2) maximum frequency = 20 MHz transmission line delay = 1340 ps	5		35	pF
		DS0 = 0 (Mode2) maximum frequency = 48 MHz transmission line delay = 670 ps	2		5	
		DS0 = 0 (Mode2) maximum frequency = 60 MHz transmission line delay = 335 ps	2		5	
		DS0 = 0 (Mode2) maximum frequency = 75 MHz transmission line delay = 402 ps	2		5	
		DS0 = 1 (Mode1) maximum frequency = 100 MHz transmission line delay = 203 ps	2		5	

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Table 3-15. USB DC Electrical Characteristics (continued)

PARAMETER			MIN	NOM	MAX	UNIT
t_{OT}	Output transition time (rise time, t_R or fall time, t_F), minimum at the minimum load and maximum at the maximum load	DS0 = 0 (Mode2) maximum frequency = 20 MHz transmission line delay = 1340 ps			15[1]	ns
		DS0 = 0 (Mode2) maximum frequency = 48 MHz transmission line delay = 670 ps			3[1]	
		DS0 = 0 (Mode2) maximum frequency = 60 MHz transmission line delay = 335 ps			3[2]	
		DS0 = 0 (Mode2) maximum frequency = 75 MHz transmission line delay = 402 ps			4[3]	
		DS0 = 1 (Mode1) maximum frequency = 100 MHz transmission line delay = 203 ps			2[3]	
1.2-V Mode						
V_{IH}	Input high-level threshold		0.65 * vdds_dv_bank6		vdds_dv_bank6 + 0.3	V
V_{IL}	Input low-level threshold		–0.3		0.35 * vdds_dv_bank6	V
V_{HYS}[11]	Input hysteresis voltage		135			mV
V_{OH}	Output high-level threshold (I_{OH} = 4 mA for 50Ω mode, I_{OH} = 8 mA for 25Ω mode)		0.75 * vdds_dv_bank6			V
V_{OL}	Output low-level threshold (I_{OL} = 4 mA for 50Ω mode, I_{OL} = 8 mA for 25Ω mode)				0.25 * vdds_dv_bank6	V
1.8-V Mode						
V_{IH}	Input high-level threshold		0.65 * vdds_dv_bank6		vdds_dv_bank6 + 0.3	V
V_{IL}	Input low-level threshold		–0.3		0.35 * vdds_dv_bank6	V
V_{HYS}[11]	Input hysteresis voltage		150			mV
V_{OH}	Output high-level threshold (I_{OH} = 4 mA for 50Ω mode, I_{OH} = 8 mA for 25Ω mode)		vdds_dv_bank6 – 0.45			V
V_{OL}	Output low-level threshold (I_{OL} = 4 mA for 50Ω mode, I_{OL} = 8 mA for 25Ω mode)				0.45	V
Signals in Mode 0: usbb[2:1]_hsic_data, usbb[2:1]_hsic_strobe (**Bottom Balls**: AF14 / AE14 / AF13 / AE13[5])						
V_{IH}	High-level input threshold		0.5 * vdds_1p2v + 0.13		vdds_1p2v + 0.2	V
V_{IL}	Low-level input threshold		–0.2		0.5 * vdds_1p2v – 0.13	V
V_{HYS}[11]	Input hysteresis voltage		NA	NA	NA	mV
C_{IN}	Input capacitance				3	pF
V_{OH}	High-level output threshold (I_{OH} = 0.1 mA)		0.9 * vdds_1p2v			V
V_{OL}	Low-level output threshold (I_{OL} = 0.1 mA)				0.1 * vdds_1p2v	V
Z_O	Output impedance	i[2:0] = 000 (Drv5)		1.66 * R_{REF}		Ω
		i[2:0] = 001 (Drv6)		1.33 * R_{REF}		
		i[2:0] = 010 (Drv7)		1.14 * R_{REF}		
		i[2:0] = 011 (Drv8)		R_{REF}[6]		
		i[2:0] = 100 (Drv9)		0.88 * R_{REF}		
		i[2:0] = 101 (Drv10)		0.8 * R_{REF}		
		i[2:0] = 110 (Drv11)		0.73 * R_{REF}		
		i[2:0] = 111 (Drv12)		0.67 * R_{REF}		
t_{OT}	Output transition time/ turn-on time (rise time, t_R or fall time, t_F) measured between 10% to 90% of PAD voltage[7][8][10]	sr[1:0] = 00 (Fastest)		250		ps
		sr[1:0] = 01 (Faster)		315		
		sr[1:0] = 10 (Fast)		340		
		sr[1:0] = 11 (Slow)		390		

Table 3-15. USB DC Electrical Characteristics (continued)

PARAMETER			MIN	NOM	MAX	UNIT
	Maximum noise on the IO supply voltage(7)(9)(10)	sr[1:0] = 00 (Fastest)			215	mV_{PP}
		sr[1:0] = 01 (Faster)			110	
		sr[1:0] = 10 (Fast)			108	
		sr[1:0] = 11 (Slow)			110	
Signal in Mode 0: usba0_otg_ce (**Bottom Ball**: C3)						
USB Low-Speed / Full-Speed Differential Transmitter						
V_{OH}	Output high-level threshold (Pulldown R = 15kΩ on both DP and DM)		2.8	3.3	3.6	V
V_{OL}	Output low-level threshold (Pullup R = 1.5kΩ @3.6V on both DP and DM)		0	0.1	0.3	V
Z_{DRV}	Driver output resistance		28	45	49.5	Ω
t_{LSOT}	Output transition time (rise time, t_R or fall time, t_F), measured between 10% to 90% of PAD voltage, C_L = 200 to 600 pF on both DP and DM, pullup R = 1.5kΩ @3.6V for DM only		75		300	ns
t_{FSOT}	Output transition time (rise time, t_R or fall time, t_F), measured between 10% to 90% of PAD voltage, C_L = 50 pF on both DP and DM		4		20	ns
USB High-Speed Differential Transmitter						
t_{OT}	Output transition time (rise time, t_R or fall time, t_F) measured between 10% to 90% of PAD voltage		500			ps
Z_{HSDRV}	Driver output resistance		40.5	45	49.5	Ω
V_{HSOI}	High-speed output idle level		–10	0	10	mV
V_{HSOH}	High-speed output data signaling high		360	400	440	mV
V_{HSOL}	High-speed output data signaling low		–10	0	10	mV
V_{CHIRPJ}	Chirp J level		700	800	1100	mV
V_{CHIRPK}	Chirp K level		–900	–800	–500	mV
Signals in Mode 0: usba0_otg_dp, usba0_otg_dm (**Bottom Balls**: B5 / B4)						
USB Low-Speed / Full-Speed Single-Ended Receiver						
V_{IH}	Input high-level threshold		2			V
V_{IL}	Input low-level threshold				0.8	V
Z_{INP}	Input impedance exclusive of pullup / pulldown (pullup / pulldown are disabled, DP/DM are in HiZ state).		300			kΩ
GPI Low-Speed / Full-Speed Receiver(12)						
V_{IH}	Input high-level threshold		2			V
V_{IL}	Input low-level threshold				0.8	V

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Table 3-15. USB DC Electrical Characteristics (continued)

PARAMETER		MIN	NOM	MAX	UNIT
USB Low-Speed / Full-Speed Differential Receiver					
V_{CM}	Differential common mode range	0.8		2.5	V
V_{DI}	Differential Input sensitivity	0.2			V
V_{HYS} (11)	Differential receiver hysteresis	0		0	mV
USB High-Speed Differential Receiver					
V_{HSSQ}	High-speed squelch detection threshold (differential signal amplitude)	100	125	150	mV
V_{HSDISC}	High-speed disconnect detection threshold (differential signal amplitude)	525	600	625	mV
V_{HSCM}	High-speed data signaling common mode voltage range	–50	200	500	mV
Z_{HSDRCV}	Input impedance in high-speed receive mode (or termination impedance)	40.5		49.5	Ω
USB Low-Speed / Full-Speed Differential Transmitter					
V_{OH}	Output high-level threshold (Pulldown R = 15kΩ on both DP and DM)	2.8	3.3	3.6	V
V_{OL}	Output low-level threshold (Pullup R = 1.5kΩ @3.6V on both DP and DM)	0	0.1	0.3	V
Z_{DRV}	Driver output resistance	28	45	49.5	Ω
t_{LSOT}	Output transition time (rise time, t_R or fall time, t_F), measured between 10% to 90% of PAD voltage, C_L = 200 to 600 pF on both DP and DM, pullup R = 1.5kΩ @3.6V for DM only	75		300	ns
t_{FSOT}	Output transition time (rise time, t_R or fall time, t_F), measured between 10% to 90% of PAD voltage, C_L = 50 pF on both DP and DM	4		20	ns
GPO Low-Speed / Full-Speed Driver (12)					
t_{OT}	Output transition time (rise time, t_R or fall time, t_F) measured between 10% to 90% of PAD voltage	4		30	ns
C_{LOAD}	Load capacitance	0		50	pF
V_{OH}	Output high-level threshold (I_{OH} = 4 mA)	2.4	3.3	3.6	V
V_{OL}	Output low-level threshold (I_{OL} = –4 mA)	0	0.1	0.4	V
USB HS Differential Transmitter					
t_{OT}	Output transition time (rise time, t_R or fall time, t_F) measured between 10% to 90% of PAD voltage	500			ps
Z_{HSDRV}	Driver output resistance	40.5	45	49.5	Ω
V_{HSOI}	High-speed output idle level	–10	0	10	mV
V_{HSOH}	High-speed output data signaling high	360	400	440	mV
V_{HSOL}	High-speed output data signaling low	–10	0	10	mV
V_{CHIRPJ}	Chirp J level	700	800	1100	mV
V_{CHIRPK}	Chirp K level	–900	–800	–500	mV
Signals in Mode 0: usbc1_icusb_dp, usbc1_icusb_dm (**Bottom Balls**: H2 / H3)					
1.8-V Mode					
V_{IH}	Input high-level threshold	0.7 * vdds_usim		vdds_usim + 0.3	V
V_{IL}	Input low-level threshold	–0.3		0.3 * vdds_usim	V
V_{HYS} (11)	Input hysteresis voltage	100			mV
V_{OH}	Output high-level threshold with 100-μA sink current at vdds minimum	vdds_usim – 0.2			V
V_{OL}	Output low-level threshold with 100-μA source current at vdds minimum			0.2	V

Table 3-15. USB DC Electrical Characteristics (continued)

PARAMETER			MIN	NOM	MAX	UNIT
t_{OT}	Output transition time at 30-pf load (rise time, t_{ROUT} or fall time, t_{FOUT}), measured between 10% to 90% of PAD voltage	SPEEDCTRL = 1			3	ns
	Output transition time at 30-pf load (rise time, t_{ROUT} or fall time, t_{FOUT}), measured between 30% to 70% of PAD voltage	SPEEDCTRL = 0			8	ns
C_{LOAD}	Load capacitance		10		30	pF
3.0-V Mode						
V_{IH}	Input high-level threshold		0.625 * vdds_usim		vdds_usim + 0.3	V
V_{IL}	Input low-level threshold		–0.3		0.25 * vdds_usim	V
V_{HYS} (11)	Input hysteresis threshold		50			mV
V_{OH}	Output high-level threshold with 100-μA sink current at vdds minimum		0.75 * vdds_usim			V
V_{OL}	Output low-level threshold with 100-μA source current at vdds minimum				0.125 * vdds_usim	V
t_{OT}	Output transition time at 30-pf load (rise time, t_{ROUT} or fall time, t_{FOUT}), measured between 10% to 90% of PAD voltage	SPEEDCTRL = 1			3	ns
	Output transition time at 30-pf load (rise time, t_{ROUT} or fall time, t_{FOUT}), measured between 30% to 70% of PAD voltage	SPEEDCTRL = 0			8	ns
C_{LOAD}	Load capacitance		10		30	pF

(1) Output transition time measured between 20% to 70% of PAD voltage

(2) Output transition time measured between 20% to 80% of PAD voltage

(3) Output transition time measured between 10% to 90% of PAD voltage

(4) In vdds_dv_y, y can have the value: bank0 or bank6 depending on the ball used. For more information on a ball and the corresponding power, see Table 2-1, POWER [9] column.

(5) Buffer is designed for high-speed application where input slew rates are more than 1 V/ns. It is fast enough to not have any noise on the signal during transition and hysteresis is not required.

(6) R_{REF} (reference output impedance) is considered to be the production trim setting for Drv8 mode, with R_{REF} = 50 Ω, which corresponds to Z_O = 50 Ω (I_{OUT} = 8 mA). For a full description of the output impedance setting, see the the Control Module / Control Module Functional Description / Functional Register Description / Signal Integrity Parameter Control Registers With Pad Group Assignment section of the OMAP4430 TRM.

(7) To achieve optimal noise/speed trade off, the slew rate (turn-on time) of the output signal can be programmed using the slew rate control bits sr[1:0]. Please note that the control bits sr[1:0] do not affect the driver DC drive-strength. They only control the driver turn-on time. It is to be noted that turn-on time and maximum supply noise are the parameter defined to help user make relative comparison and correlate the driver operation at different turn-on time settings.

(8) Output transition time/turn-on time for Drv8 setting, i[2:0] = 011. For a full description of this setting, see the Control Module / Control Module Functional Description / Functional Register Description / Signal Integrity Parameter Control Registers With Pad Group Assignment section of the OMAP4430 TRM.

(9) Maximum noise (peak-peak) on the IO supply voltage for Drv8 setting, i[2:0] = 011.

(10) The measurement setup (see Figure 3-1 and Figure 3-2) is not intended as a precise representation of any particular system environment or a depiction of the actual load presented. Maximum output supply noise, (see Figure 3-2, L*di/dt) on the IO supply is measured with 1 nH of inductance on the IO supply.

(11) V_{HYS} is the magnitude of the difference between the positive-going threshold voltage V_{T+} and the negative-going threshold voltage V_{T-}.

(12) The GPIO modes are only available through multiplexing mode 1 or 2. For more information, see Table 2-1.

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3.3.11 MMC/SDIO DC Electrical Characteristics

Table 3-16 summarizes the MMC/SDIO dc electrical characteristics in multiplexing mode 0.

NOTE

For more information on the IO cell configurations (SPEEDCTRL, MB[1:0] and LB0), see the Control Module / Control Module Functional Description / Functional Register Description / Signal Integrity Parameter Control Registers With Pad Group Assignment section of the OMAP4430 TRM.

Table 3-16. MMC/SDIO DC Electrical Characteristics

PARAMETER			MIN	NOM	MAX	UNIT
Signals in Mode 0: sdmmc1_clk, sdmmc1_cmd, sdmmc1_dat[7:0] (**Bottom Balls**: D2 / E3 / E4 / E2 / E1 / F4 / F3 / F1 / G4 / G3)						
1.8-V Mode						
V_{IH}	Input high-level threshold		0.7 * vdds_sdmmc1		vdds_sdmmc1 + 0.3	V
V_{IL}	Input low-level threshold		–0.3		0.3 * vdds_sdmmc1	V
V_{HYS} (2)	Input hysteresis voltage		100			mV
V_{OH}	Output high-level threshold with 100-µA sink current at vdds_sdmmc1 minimum		vdds_sdmmc1 – 0.2			V
V_{OL}	Output low-level threshold with 100-µA source current at vdds_sdmmc1 minimum				0.2	V
t_{OT}	Output transition time at 30-pf load (rise time, t_{ROUT} or fall time, t_{FOUT}), measured between 10% to 90% of PAD voltage	SPEEDCTRL = 1			3	ns
	Output transition time at 30-pf load (rise time, t_{ROUT} or fall time, t_{FOUT}), measured between 30% to 70% of PAD voltage	SPEEDCTRL = 0			8	ns
C_{LOAD}	Load capacitance		10		30	pF
3.0-V Mode						
V_{IH}	Input high-level threshold		0.625 * vdds_sdmmc1		vdds_sdmmc1 + 0.3	V
V_{IL}	Input low-level threshold		–0.3		0.25 * vdds_sdmmc1	V
V_{HYS} (2)	Input hysteresis threshold		50			mV
V_{OH}	Output high-level threshold with 100-µA sink current at vdds_sdmmc1 minimum		0.75 * vdds_sdmmc1			V
V_{OL}	Output low-level threshold with 100-µA source current at vdds_sdmmc1 minimum				0.125 * vdds_sdmmc1	V
t_{OT}	Output transition time at 30-pf load (rise time, t_{ROUT} or fall time, t_{FOUT}), measured between 10% to 90% of PAD voltage	SPEEDCTRL = 1			3	ns
	Output transition time at 30-pf load (rise time, t_{ROUT} or fall time, t_{FOUT}), measured between 30% to 70% of PAD voltage	SPEEDCTRL = 0			8	ns
C_{LOAD}	Load capacitance		10		30	pF

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Table 3-16. MMC/SDIO DC Electrical Characteristics (continued)

PARAMETER			MIN	NOM	MAX	UNIT
Signals in Mode 0: sdmmc5_clk, sdmmc5_cmd, sdmmc5_dat[3:0] (**Bottom Balls**: AE5 / AF5 / AE4 / AF4 / AG3 / AF3)						
C_{LOAD} (3)	Load capacitance	MB[1:0] = 11 LB0 = 1 (Mode1) maximum frequency = 24 MHz transmission line delay = 670 ps	20		25	pF
		MB[1:0] = 11 LB0 = 1 (Mode1) maximum frequency = 60 MHz transmission line delay = 335 ps	2		5	
		MB[1:0] = 01 LB0 = 0 (Mode2) maximum frequency = 25 MHz transmission line delay = 335 ps	14		17	
		MB[1:0] = 01 LB0 = 0 (Mode2) maximum frequency = 48 MHz transmission line delay = 536 ps	2		5	
		MB[1:0] = 10 LB0 = 1 (Mode3) maximum frequency = 20 MHz transmission line delay = 838 ps	23		28	
		MB[1:0] = 10 LB0 = 1 (Mode3) maximum frequency = 24 MHz transmission line delay = 670 ps	16		20	
		MB[1:0] = 10 LB0 = 0 (Mode4) maximum frequency = 4 MHz transmission line delay = 1675 ps	16		20	
		MB[1:0] = 10 LB0 = 0 (Mode4) maximum frequency = 25 MHz transmission line delay = 670 ps	2		5	
		MB[1:0] = 10 LB0 = 0 (Mode4) maximum frequency = 25 MHz transmission line delay = 670 ps	5		7	
		MB[1:0] = 10 LB0 = 0 (Mode4) maximum frequency = 25 MHz transmission line delay = 536 ps	2		11	

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Table 3-16. MMC/SDIO DC Electrical Characteristics (continued)

PARAMETER			MIN	NOM	MAX	UNIT
t_{OT} (3)	Output transition time (rise time, t_R or fall time, t_F) measured between 10% to 90% of PAD voltage, the maximum at the maximum load	MB[1:0] = 11 LB0 = 1 (Mode1) maximum frequency = 24 MHz transmission line delay = 670 ps			10	ns
		MB[1:0] = 11 LB0 = 1 (Mode1) maximum frequency = 60 MHz transmission line delay = 335 ps			4	
		MB[1:0] = 01 LB0 = 0 (Mode2) maximum frequency = 25 MHz transmission line delay = 335 ps			5.6 (1)	
		MB[1:0] = 01 LB0 = 0 (Mode2) maximum frequency = 48 MHz transmission line delay = 536 ps			6.3	
		MB[1:0] = 10 LB0 = 1 (Mode3) maximum frequency = 20 MHz transmission line delay = 838 ps			10.5 (1)	
		MB[1:0] = 10 LB0 = 1 (Mode3) maximum frequency = 24 MHz transmission line delay = 670 ps			12.5	
		MB[1:0] = 10 LB0 = 0 (Mode4) maximum frequency = 4 MHz transmission line delay = 1675 ps			16.8 (1)	
		MB[1:0] = 10 LB0 = 0 (Mode4) maximum frequency = 25 MHz transmission line delay = 670 ps			10	
		MB[1:0] = 10 LB0 = 0 (Mode4) maximum frequency = 25 MHz transmission line delay = 670 ps			12.2	
		MB[1:0] = 10 LB0 = 0 (Mode4) maximum frequency = 25 MHz transmission line delay = 536 ps			8 (1)	
1.2-V Mode						
V_{IH}	Input high-level threshold		0.65 * vdds_dv_bank4		vdds_dv_bank4 + 0.3	V
V_{IL}	Input low-level threshold		–0.3		0.35 * vdds_dv_bank4	V
V_{HYS} (2)	Input hysteresis voltage		135			mV
V_{OH}	Output high-level threshold (I_{OH} = 4 mA)		0.75 * vdds_dv_bank4			V
V_{OL}	Output low-level threshold (I_{OL} = 4 mA)				0.25 * vdds_dv_bank4	V
1.8-V Mode						
V_{IH}	Input high-level threshold		0.65 * vdds_dv_bank4		vdds_dv_bank4 + 0.3	V
V_{IL}	Input low-level threshold		–0.3		0.35 * vdds_dv_bank4	V
V_{HYS} (2)	Input hysteresis voltage		150			mV
V_{OH}	Output high-level threshold (I_{OH} = 4 mA)		vdds_dv_bank4 – 0.45			V
V_{OL}	Output low-level threshold (I_{OL} = 4 mA)				0.45	V

(1) Output transition time measured between 20% to 80% of PAD voltage.

(2) V_{HYS} is the magnitude of the difference between the positive-going threshold voltage V_{T+} and the negative-going threshold voltage V_{T-}.

(3) Depending on the programming mode, different output load and transition time are available following the targeted maximum frequency, transmission line or output transition time.

3.3.12 JTAG DC Electrical Characteristics

Table 3-17 summarizes the JTAG dc electrical characteristics in multiplexing mode 0.

Table 3-17. JTAG DC Electrical Characteristics

PARAMETER	MIN	NOM	MAX	UNIT
Signals in Mode 0: jtag_ntrst, jtag_tck, jtag_rtck, jtag_tms_tmsc, jtag_tdi, jtag_tdo (**Bottom Balls**: AH2 / AG1 / AE3 / AH1 / AE1 / AE2)				

Table 3-17. JTAG DC Electrical Characteristics (continued)

PARAMETER		MIN	NOM	MAX	UNIT
C_{LOAD}	Load capacitance		30		pF
t_{OR}	Output rise time		5.5		ns
t_{OF}	Output fall time		5.7		ns
1.8-V Mode					
V_{IH}	High-level input voltage	0.65 * vdds_1p8v		vdds_1p8v + 0.3	V
V_{IL}	Low-level input voltage	–0.3		0.35 * vdds_1p8v	V
V_{OH}	High-level output voltage (I_{OH} = –4 mA)	vdds_1p8v – 0.45			V
V_{OL}	Low-level output voltage (I_{OL} = 4 mA)			0.45	V
V_{HYS} (1)	Hysteresis voltage at an input	150			mV

(1) V_{HYS} is the magnitude of the difference between the positive-going threshold voltage V_{T+} and the negative-going threshold voltage V_{T-}.

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3.3.13 DPM DC Electrical Characteristics

Table 3-18 summarizes the DPM dc electrical characteristics in multiplexing mode 0.

NOTE

For more information on the IO cell configurations (DS0), see the Control Module / Control Module Functional Description / Functional Register Description / Signal Integrity Parameter Control Registers With Pad Group Assignment section of the OMAP4430 TRM.

Table 3-18. DPM DC Electrical Characteristics

PARAMETER			MIN	NOM	MAX	UNIT
Signals in Mode 0: dpm_emu[1:0], dpm_emu3, dpm_emu[19:5] (**Bottom Balls**: M2 / N2 / V1 / W1 / W2 / W3 / W4 / Y2 / Y3 / Y4 / AA1 / AA2 / AA3 / AA4 / AB2 / AB3 / AB4 / AC4)						
C_{LOAD}	Load capacitance	DS0 = 0 (Mode2) maximum frequency = 20 MHz transmission line delay = 1340 ps	5		35	pF
		DS0 = 0 (Mode2) maximum frequency = 48 MHz transmission line delay = 670 ps	2		5	
		DS0 = 0 (Mode2) maximum frequency = 60 MHz transmission line delay = 335 ps	2		5	
		DS0 = 0 (Mode2) maximum frequency = 75 MHz transmission line delay = 402 ps	2		5	
		DS0 = 1 (Mode1) maximum frequency = 100 MHz transmission line delay = 203 ps	2		5	
t_{OT}	Output transition time (rise time, t_R or fall time, t_F), the maximum at the maximum load	DS0 = 0 (Mode2) maximum frequency = 20 MHz transmission line delay = 1340 ps			15(1)	ns
		DS0 = 0 (Mode2) maximum frequency = 48 MHz transmission line delay = 670 ps			3(1)	
		DS0 = 0 (Mode2) maximum frequency = 60 MHz transmission line delay = 335 ps			3(2)	
		DS0 = 0 (Mode2) maximum frequency = 75 MHz transmission line delay = 402 ps			4(3)	
		DS0 = 1 (Mode1) maximum frequency = 100 MHz transmission line delay = 203 ps			2(3)	
1.8-V Mode						
V_{IH}	Input high-level threshold		0.65 * vdds_1p8v		vdds_1p8v + 0.3	V
V_{IL}	Input low-level threshold		–0.3		0.35 * vdds_1p8v	V
V_{HYS}(4)	Input hysteresis voltage		150			mV
V_{OH}	Output high-level threshold (I_{OH} = 4 mA for 50Ω mode, I_{OH} = 8 mA for 25Ω mode)		vdds_1p8v – 0.45			V
V_{OL}	Output low-level threshold (I_{OL} = 4 mA for 50Ω mode, I_{OL} = 8 mA for 25Ω mode)				0.45	V

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Table 3-18. DPM DC Electrical Characteristics (continued)

PARAMETER			MIN	NOM	MAX	UNIT
Signals in Mode 0: dpm_emu2, dpm_emu4 (**Bottom Balls**: P2 / V2)						
C_{LOAD}	Load capacitance	DS0 = 0 (Mode2) maximum frequency = 20 MHz transmission line delay = 1340 ps	5		35	pF
		DS0 = 0 (Mode2) maximum frequency = 48 MHz transmission line delay = 670 ps	2		5	
		DS0 = 0 (Mode2) maximum frequency = 60 MHz transmission line delay = 335 ps	2		5	
		DS0 = 0 (Mode2) maximum frequency = 75 MHz transmission line delay = 402 ps	2		5	
		DS0 = 1 (Mode1) maximum frequency = 100 MHz transmission line delay = 203 ps	2		5	
t_{OT}	Output transition time (rise time, t_R or fall time, t_F), the maximum at the maximum load	DS0 = 0 (Mode2) maximum frequency = 20 MHz transmission line delay = 1340 ps			15[(1)]	ns
		DS0 = 0 (Mode2) maximum frequency = 48 MHz transmission line delay = 670 ps			3[(1)]	
		DS0 = 0 (Mode2) maximum frequency = 60 MHz transmission line delay = 335 ps			3[(2)]	
		DS0 = 0 (Mode2) maximum frequency = 75 MHz transmission line delay = 402 ps			4[(3)]	
		DS0 = 1 (Mode1) maximum frequency = 100 MHz transmission line delay = 203 ps			2[(3)]	
1.8-V Mode						
V_{IH}	Input high-level threshold		0.65 * vdds_1p8v		vdds_1p8v + 0.3	V
V_{IL}	Input low-level threshold		–0.3		0.35 * vdds_1p8v	V
V_{HYS}[(4)]	Input hysteresis voltage		70			mV
V_{OH}	Output high-level threshold (I_{OH} = 4 mA for 50Ω mode, I_{OH} = 8 mA for 25Ω mode)		vdds_1p8v – 0.45			V
V_{OL}	Output low-level threshold (I_{OL} = 4 mA for 50Ω mode, I_{OL} = 8 mA for 25Ω mode)				0.45	V

(1) Output transition time measured between 20% to 70% of PAD voltage.

(2) Output transition time measured between 20% to 80% of PAD voltage.

(3) Output transition time measured between 10% to 90% of PAD voltage.

(4) V_{HYS} is the magnitude of the difference between the positive-going threshold voltage V_{T+} and the negative-going threshold voltage V_{T-}.

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3.3.14 Keypad DC Electrical Characteristics

Table 3-19 summarizes the keypad dc electrical characteristics in multiplexing mode 0.

NOTE

For more information on the IO cell configurations (SC[1:0]), see the Control Module / Control Module Functional Description / Functional Register Description / Signal Integrity Parameter Control Registers With Pad Group Assignment section of the OMAP4430 TRM.

Table 3-19. Keypad DC Electrical Characteristics

PARAMETER			MIN	NOM	MAX	UNIT
Signals in Mode 0: kpd_col[5:0], kpd_row[5:0] (**Bottom Balls**: G26 / G25 / H26 / H25 / J27 / H27 / J26 / J25 / K26 / K25 / L27 / K27)						
C_{LOAD}	Load capacitance	SC[1:0] = 00	4		60	pF
		SC[1:0] = 01	2		21	
		SC[1:0] = 10	7		33	
t_{OT}	Output transition time (rise time, t_R or fall time, t_F) measured between 10% to 90% of PAD voltage, minimum at the minimum load and maximum at the maximum load	SC[1:0] = 00	1		15	ns
		SC[1:0] = 01	0.4		5	
		SC[1:0] = 10	0.6		7	
1.2-V Mode						
V_{IH}	Input high-level threshold		0.65 * vdds_dv_bank7		vdds_dv_bank7 + 0.3	V
V_{IL}	Input low-level threshold		–0.3		0.35 * vdds_dv_bank7	V
V_{HYS}(1)	Input hysteresis voltage		135			mV
V_{OH}	Output high-level threshold (I_{OH} = –4 mA)		0.75 * vdds_dv_bank7			V
V_{OL}	Output low-level threshold (I_{OL} = 4 mA)				0.25 * vdds_dv_bank7	V
1.8-V Mode						
V_{IH}	Input high-level threshold		0.65 * vdds_dv_bank7		vdds_dv_bank7 + 0.3	V
V_{IL}	Input low-level threshold		–0.3		0.35 * vdds_dv_bank7	V
V_{HYS}(1)	Input hysteresis voltage		150			mV
V_{OH}	Output high-level threshold (I_{OH} = –4 mA)		vdds_dv_bank7 – 0.45			V
V_{OL}	Output low-level threshold (I_{OL} = 4 mA)				0.45	V

(1) V_{HYS} is the magnitude of the difference between the positive-going threshold voltage V_{T+} and the negative-going threshold voltage V_{T-}.

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3.3.15 System DC Electrical Characteristics

Table 3-20 summarizes the system dc electrical characteristics in multiplexing mode 0.

NOTE

For more information on the IO cell configurations (SC[1:0], MB[1:0] and LB0), see the Control Module / Control Module Functional Description / Functional Register Description / Signal Integrity Parameter Control Registers With Pad Group Assignment section of the OMAP4430 TRM.

Table 3-20. System DC Electrical Characteristics

PARAMETER			MIN	NOM	MAX	UNIT
Signals in Mode 0: sys_nrespwron, sys_nreswarm (**Bottom Balls**: AE7, AF7)						
1.8-V Mode						
V_{IH}	Input high-level threshold		0.65 * vdds_1p8v		vdds_1p8v + 0.3	V
V_{IL}	Input low-level threshold		–0.3		0.35 * vdds_1p8v	V
V_{HYS}(4)	Input hysteresis voltage		150			mV
V_{OH}	Output high-level threshold (I_{OH} = –4 mA)		vdds_1p8v – 0.45			V
V_{OL}	Output low-level threshold (I_{OL} = 4 mA)				0.45	V
Signals in Mode 0: fref_clk_ioreq, sys_32k, sys_pwr_req, sys_pwron_reset_out, sys_boot[7:6] (**Bottom Balls**: AD1 / AG7 / AH7 / AG6 / AF8 / AE8)						
C_{LOAD}	Load capacitance	SC[1:0] = 00	4		60	pF
		SC[1:0] = 01	2		21	
		SC[1:0] = 10	7		33	
t_{OT}	Output transition time (rise time, t_R or fall time, t_F) measured between 10% to 90% of PAD voltage, minimum at the minimum load and maximum at the maximum load	SC[1:0] = 00	1		15	ns
		SC[1:0] = 01	0.4		5	
		SC[1:0] = 10	0.6		7	
1.8-V Mode						
V_{IH}	Input high-level threshold		0.65 * vdds_y(1)		vdds_y(1) + 0.3	V
V_{IL}	Input low-level threshold		–0.3		0.35 * vdds_y(1)	V
V_{HYS}(4)	Input hysteresis voltage		150			mV
V_{OH}	Output high-level threshold (I_{OH} = –4 mA)		vdds_y(1) – 0.45			V
V_{OL}	Output low-level threshold (I_{OL} = 4 mA)				0.45	V
Signals in Mode 0: sys_nirq[2:1], sys_boot[5:0] (**Bottom Balls**: AE6 / AF6 / F26 / E27 / E26 / E25 / D28 / D27)						
C_{LOAD}	Load capacitance	SC[1:0] = 00	4		60	pF
		SC[1:0] = 01	2		21	
		SC[1:0] = 10	7		33	
t_{OT}	Output transition time (rise time, t_R or fall time, t_F) measured between 10% to 90% of PAD voltage, minimum at the minimum load and maximum at the maximum load	SC[1:0] = 00	1		15	ns
		SC[1:0] = 01	0.4		5	
		SC[1:0] = 10	0.6		7	
1.8-V Mode						
V_{IH}	Input high-level threshold		0.65 * vdds_1p8v		vdds_1p8v + 0.3	V
V_{IL}	Input low-level threshold		–0.3		0.35 * vdds_1p8v	V
V_{HYS}(4)	Input hysteresis voltage		150			mV
V_{OH}	Output high-level threshold (I_{OH} = –4 mA)		vdds_1p8v – 0.45			V
V_{OL}	Output low-level threshold (I_{OL} = 4 mA)				0.45	V

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Table 3-20. System DC Electrical Characteristics (continued)

PARAMETER			MIN	NOM	MAX	UNIT
Signals in Mode 0: fref_clk[4:0]_out, fref_clk[4:3]_req (**Bottom Balls**: AD2 / AA28 / Y28 / AD4 / AC3 / AD3 / AC2)						
C_{LOAD}[(5)]	Load capacitance	MB[1:0] = 11 LB0 = 1 (Mode1) maximum frequency = 24 MHz transmission line delay = 670 ps	20		25	pF
		MB[1:0] = 11 LB0 = 1 (Mode1) maximum frequency = 60 MHz transmission line delay = 335 ps	2		5	
		MB[1:0] = 01 LB0 = 0 (Mode2) maximum frequency = 25 MHz transmission line delay = 335 ps	14		17	
		MB[1:0] = 01 LB0 = 0 (Mode2) maximum frequency = 48 MHz transmission line delay = 536 ps	2		5	
		MB[1:0] = 10 LB0 = 1 (Mode3) maximum frequency = 20 MHz transmission line delay = 838 ps	23		28	
		MB[1:0] = 10 LB0 = 1 (Mode3) maximum frequency = 24 MHz transmission line delay = 670 ps	16		20	
		MB[1:0] = 10 LB0 = 0 (Mode4) maximum frequency = 4 MHz transmission line delay = 1675 ps	16		20	
		MB[1:0] = 10 LB0 = 0 (Mode4) maximum frequency = 25 MHz transmission line delay = 670 ps	2		5	
		MB[1:0] = 10 LB0 = 0 (Mode4) maximum frequency = 25 MHz transmission line delay = 670 ps	5		7	
		MB[1:0] = 10 LB0 = 0 (Mode4) maximum frequency = 25 MHz transmission line delay = 536 ps	2		11	

Table 3-20. System DC Electrical Characteristics (continued)

PARAMETER			MIN	NOM	MAX	UNIT
t_{OT}(5)	Output transition time (rise time, t_R or fall time, t_F) measured between 10% to 90% of PAD voltage, the maximum at the maximum load	MB[1:0] = 11 LB0 = 1 (Mode1) maximum frequency = 24 MHz transmission line delay = 670 ps			10	ns
		MB[1:0] = 11 LB0 = 1 (Mode1) maximum frequency = 60 MHz transmission line delay = 335 ps			4	
		MB[1:0] = 01 LB0 = 0 (Mode2) maximum frequency = 25 MHz transmission line delay = 335 ps			5.6(3)	
		MB[1:0] = 01 LB0 = 0 (Mode2) maximum frequency = 48 MHz transmission line delay = 536 ps			6.3	
		MB[1:0] = 10 LB0 = 1 (Mode3) maximum frequency = 20 MHz transmission line delay = 838 ps			10.5(3)	
		MB[1:0] = 10 LB0 = 1 (Mode3) maximum frequency = 24 MHz transmission line delay = 670 ps			12.5	
		MB[1:0] = 10 LB0 = 0 (Mode4) maximum frequency = 4 MHz transmission line delay = 1675 ps			16.8(3)	
		MB[1:0] = 10 LB0 = 0 (Mode4) maximum frequency = 25 MHz transmission line delay = 670 ps			10	
		MB[1:0] = 10 LB0 = 0 (Mode4) maximum frequency = 25 MHz transmission line delay = 670 ps			12.2	
		MB[1:0] = 10 LB0 = 0 (Mode4) maximum frequency = 25 MHz transmission line delay = 536 ps			8(3)	
1.2-V Mode						
V_{IH}	Input high-level threshold		0.65 * vdds_w(2)		vdds_w(2) + 0.3	V
V_{IL}	Input low-level threshold		–0.3		0.35 * vdds_w(2)	V
V_{HYS}(4)	Input hysteresis voltage		135			mV
V_{OH}	Output high-level threshold (I_{OH} = 4 mA)		0.75 * vdds_w(2)			V
V_{OL}	Output low-level threshold (I_{OL} = 4 mA)				0.25 * vdds_w(2)	V
1.8-V Mode						
V_{IH}	Input high-level threshold		0.65 * vdds_w(2)		vdds_w(2) + 0.3	V
V_{IL}	Input low-level threshold		–0.3		0.35 * vdds_w(2)	V
V_{HYS}(4)	Input hysteresis voltage		150			mV
V_{OH}	Output high-level threshold (I_{OH} = 4 mA)		vdds_w(2) – 0.45			V
V_{OL}	Output low-level threshold (I_{OL} = 4 mA)				0.45	V
Signals in Mode 0: fref_xtal_in, fref_xtal_out (**Bottom Balls**: AH6 / AH5)						
V_{IH}	Input high-level threshold		0.65 * vdds_1p8_fref			V
V_{IL}	Input low-level threshold				0.35 * vdds_1p8_fref	V
V_{HYS}(4)	Input hysteresis voltage		250			mV
C_{IN}	Input capacitance		1	1.15	1.35	pF
t_{IT}	Input transition time (rise time, t_R or fall time, t_F measured between 10% and 90% of PAD voltage)				5	ns
V_{OH}	Output high-level threshold		0.7 * vdds_1p8_fref			V
V_{OL}	Output low-level threshold				0.3 * vdds_1p8_fref	V
C_{LOAD}	Load capacitance		12		24	pF
Signal in Mode 0: fref_slicer_in (**Bottom Ball**: AG8)						

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Table 3-20. System DC Electrical Characteristics (continued)

PARAMETER		MIN	NOM	MAX	UNIT
Single-ended Application Mode (single-ended sine clock)					
V_{SWING}	Input voltage swing(6)	500		1600	mV_{PP}
R_{IN}	Input resistance		18.3		kΩ
C_{IN}	Input capacitance			2.5	pF
Single–ended High-Voltage CMOS Application Mode (single-ended square clock)					
V_{IH}	Input high-level threshold	0.65 * vdds_1p8_fref		2.00	V
V_{IL}	Input low-level threshold	–0.2		0.35 * vdds_1p8_fref	V
R_{IN}	Input resistance		18.3		kΩ
C_{IN}	Input capacitance			2.5	pF
t_{IT}	Input transition time (rise time, t_R or fall time, t_F) measured between 10% to 90% of PAD voltage	1.5		10	ns

(1) In vdds_y, y can have the value: vdds_1p8_fref or vdds_1p8v depending on the ball used. For more information on a ball and the corresponding power, see Table 2-1, POWER [9] column.

(2) In vdds_w, w can have the value: vdds_1p8_fref or vdds_dv_fref depending on the ball used. For more information on a ball and the corresponding power, see Table 2-1, POWER [9] column.

(3) Output transition time measured between 20% to 80% of PAD voltage.

(4) V_{HYS} is the magnitude of the difference between the positive-going threshold voltage V_{T+} and the negative-going threshold voltage V_{T-}.

(5) Depending on the programming mode, different output load and transition time are available following the targeted maximum frequency, transmission line or output transition time.

(6) Minimum input common mode voltage – input voltage swing/2 > 0 V
Maximum input common mode voltage + input voltage swing/2 < 1.6 V

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3.4 External Capacitors

3.4.1 Voltage Decoupling Capacitors

To improve module performance, decoupling capacitors are required to suppress the switching noise generated by high frequency and to stabilize the supply voltage. A decoupling capacitor is most effective when it is close to the device, because this minimizes the inductance of the circuit board wiring and interconnects.

NOTE

The TWL6030 PMIC supports the following output bulk capacitors:

- 10μF maximum close to the TWL6030 PMIC
- The additional mid-frequency decoupling capacitors are described in Table 3-21. Note that a maximum of 10μF is supported at OMAP side.
- The SMPS feedback sense line must remain closed to the PMIC

For other PMICs which can support more than 10μF at OMAP side, then a bulk capacitor of, at least, 20μF is recommended.

3.4.1.1 Core, MPU, IVA, Audio Voltage Decoupling

3.4.1.1.1 Core, MPU, IVA, Audio Voltage Decoupling Values

Table 3-21 summarizes the core voltage decoupling characteristics.

CAUTION

PCB guideline between the power IC (PMIC) balls and the OMAP balls:

- Maximum recommended inductance by power supply rail less than 2 nH (VDD + VSS).
- Maximum recommended static IR-drop by power supply rail less than 1.5% (with rise on ground accounted for).
- For more information on maximum peak-peak noise on the supply, see Table 3-3, *Recommended Operating Conditions*.
- Decoupling bypass capacitors main characteristics:
  - Size code:
    - 10 μF: 0603/X5R
    - 4.7 μF: 0603/X5R
    - 1 μF: 0402/X5R
    - 470 nF: 0402/X5R
    - 100 nF: 0201/X5R
  - Minimum value for each PCB capacitor: 100 nF
  - ESL decoupling capacitor must not exceed 0.5 nF
  - The capacitor value is defined at ±50% of the value to take in account the aging effects and the voltage impact.
  - Among the different capacitors, 470 nF is recommended (not required) to filter at 5-MHz to 10-MHz frequency range

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Table 3-21. Core, MPU, IVA, Audio Voltage Decoupling Characteristics(1)

PARAMETER		PDN IMPEDANCE CHARACTERISTICS(4)		PCB RESISTANCE BETWEEN SPMS and OMAP (mΩ)(5)	MAXIMUM LOOP INDUCTANCE PER CAPACITOR (WITHOUT ESL)(2) (nH)	DECOUPLING CAPACITOR VALUES(3)			
		IMPEDANCE TARGET (mΩ)	FREQUENCY OF INTEREST (MHz)			100nF	470nF	1μF	4.7μF
C_{vdd_core}	CORE @1.1 V, (transient 0.6 A)	91	40	13.75	0.7	6	1	3	1
C_{vdd_mpu}	MPU @1000 MHz @1.35 V (transient 0.725 A)	93	40	14	0.7	5	1	3	1
	MPU @1200 MHz @1.35 V (transient 0.95 A)	71	28	10	0.7	5	1	3	1
$C_{vdd\_iva\_audio}$ (@1.26 V, transient 0.325 A)		194	46	29	1.0	5	0	1	0

(1) See Table 3-3 for more information on peak-to-peak noise values
(2) ESL must be as low as possible and must not exceed 0.5 nH.
(3) To take into account the aging effects and voltage impact on capacitance, their values, as described in Table 3-21, are specified at ± 50%.
(4) The PDN (Power Delivery Network) impedance characteristics are defined versus the device activity (that runs at different frequency) based on Table 3-3, *Recommended Operating Conditions*, peak-peak noise values.
(5) The static drop requirement drives the maximum acceptable PCB resistance between the PMIC or the external SMPS and the OMAP4 power balls.

3.4.1.2 IO Voltage Decoupling

Table 3-22 summarizes the IO voltage decoupling characteristics.

CAUTION

PCB guideline between the power IC (PMIC) balls and the OMAP balls:

- Maximum recommended static ir-drop by power supply rail less than 1% of the supplied voltage.
- For more information on maximum peak-peak noise on the supply, see see Table 3-3, *Recommended Operating Conditions*.
- Decoupling bypass capacitors main characteristics:
  - TCC size code:
    - 470 nF: 0402/X5R
    - 220 nF: 0402/X5R
    - 100 nF: 0201/X5R
  - Minimum value for each PCB capacitor: 100 nF
  - The capacitor value is defined at ±50% of the value to take in account the aging effects, and the voltage impact.

Table 3-22. IO Voltage Decoupling Characteristics(1)(2)

PARAMETER	MIN(4)	TYP	MAX(4)	UNIT
1.2-V Supply Voltage IOs				

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Table 3-22. IO Voltage Decoupling Characteristics[(1)(2)] (continued)

PARAMETER	MIN[(4)]	TYP	MAX[(4)]	UNIT
C_{vdds_1p2v}	50	100	150	nF
1.8-V Supply Voltage IOs				
C_{vdds_1p8v}	100	220	300	nF
$C_{vdds\_1p8\_fref}$	50	100	150	
1.2-V, 1.8-V Supply Voltage IOs				
$C_{vdds\_dv\_gpmc}$	300	6 x 100	900	nF
$C_{vdds\_dv\_sdmmc2}$				
$C_{vdds\_dv\_c2c}$				
$C_{vdds\_dv\_cam}$				
$C_{vdds\_dv\_bank0}$				
$C_{vdds\_dv\_bank1}$				
$C_{vdds\_dv\_bank2}$				
$C_{vdds\_dv\_bank3}$				
$C_{vdds\_dv\_bank4}$				
$C_{vdds\_dv\_bank5}$				
$C_{vdds\_dv\_bank6}$				
$C_{vdds\_dv\_bank7}$				
$C_{vdds\_dv\_fref}$				
1.8-V, 3.3-V SDMMC1 and SIM Supply Voltage IOs				
C_{vdds_usim}	50	100	150	nF
C_{vdds_sdmmc1}	50	100	150	nF
1.2-V LPDDR2 Supply Voltage IOs				
C_{vddq_lpddr2}	800	2 x 470 + 6 x 100	2400	nF
$C_{vddq\_vref\_lpddr2}$[(3)]	50	100	150	nF
C_{vddca_lpddr2}	285	1 x 100 + 1 x 470	855	nF
$C_{vddca\_vref\_lpddr2}$[(3)]	50	100	150	nF
Other				
vpp_cust[(5)]		100		nF

(1) All capacitor values described in this table are based on capacitors of 100 nF.

(2) See Table 3-3 for more information on peak-to-peak noise values.

(3) vddq_vref_lpddr2 and vddca_vref_lpddr2 are dedicated power supplies for OMAP embedded VREF generator.

(4) To take into account the aging effects and voltage impact on capacitance, their values, as described in Table 3-22, are specified at ± 50%.

(5) vpp_cust is only powered when programming CPFROM eFuses. Otherwise, it is recommended to leave vpp_cust turned off (floating). Note that if the TWL6030 PMIC is used then the vpp pull-down resistor inside the TWL6030 must be disabled when vpp_cust is turned off.

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3.4.1.3 Analog Voltage Decoupling

3.4.1.3.1 Analog Voltage Decoupling Values

Table 3-23 summarizes the analog voltage decoupling characteristics.

CAUTION

PCB guidelines between the power IC (PMIC) balls and the OMAP balls:

- Maximum recommended inductance (V_{DDA} + V_{SSA}) by power supply rail less than 30 nH.
- The capacitors must be placed as closed as possible to the balls. Maximum loop inductance for the decoupling capacitances must not exceed:
  - 1.0 nH maximum for DLLs
  - 1.5 nH maximum for complex IOs (HDMI) and DPLLs
  - 2.0 nH maximum for SRAM LDOs, BodyBias (BB) LDOs, WakeUp (WKUP) LDO, BandGap (BG) LDO, Video DAC, CSI2, CCPV2, and DSI
- Maximum recommended resistance (V_{DDA} + V_{SSA}) by power supply rail between 0.1 Ω to 0.3 Ω.
- For more information on Video DAC and HDMI routing guidelines, see Figure 3-3, *VDAC / HDMI Power PCB Routing Topology*.
- For more information on DPLLs and complex IOs routing guidelines, see Figure 3-4, *DPLLs / Complex I/O VDDA Power PCB Routing Topology*.
- For more information on OMAP4 embedded LDOs and BandGap routing guidelines, see Figure 3-5, *OMAP Embedded LDO / Bandgap Power PCB Routing Topology*.

Table 3-23. Analog Voltage Decoupling Characteristics(1)(2)

PARAMETER	MIN(3)	TYP	MAX(3)	UNIT
$C_{vdda\_dpll\_mpu}$	50	100	150	nF
$C_{vdda\_dpll\_core\_audio}$	50	100	150	nF
$C_{vdda\_dpll\_iva\_per}$	50	100	150	nF
$C_{vdda\_dll0\_lpddr21}$(4)	150	3 x 100	450	nF
$C_{vdda\_dll1\_lpddr21}$(4)				nF
$C_{vdda\_dll0\_lpddr22}$(4)				nF
$C_{vdda\_dll1\_lpddr22}$(4)				nF
$C_{vdda\_ldo\_sram\_mpu}$	110	220	330	nF
$C_{vdda\_ldo\_sram\_iva\_audio}$	110	220	330	nF
$C_{vdda\_ldo\_sram\_core}$	110	220	330	nF
$C_{vdda\_ldo\_emu\_wkup}$	50	100	150	nF
$C_{vdda\_bdgp\_vbb}$	50	100	150	nF
C_{vdda_dsi1}	110	220	330	nF
C_{vdda_dsi2}	110	220	330	nF
C_{vdda_csi21}	110	220	330	nF
C_{vdda_csi22}	110	220	330	nF
$C_{vdda\_hdmi\_vdac}$	235	470	705	nF
$C_{vdda\_usba0otg\_1p8v}$	110	220	330	nF
$C_{vdda\_usba0otg\_3p3v}$	110	220	330	nF

(1) Decoupling capacitance side code (TCC): 0402/X5R.
(2) See Table 3-3 for more information on peak-to-peak noise values.
(3) To take into account the aging effects and voltage impact on capacitance, their values, as described in Table 3-23, are specified at ± 50%.
(4) In Figure 3-7, *External Capacitors,* the three DLL decoupling capacitors have the names: Cvdda_dll1/3, Cvdda_dll2/3, and Cvdda_dll3/3 to represent the three decoupling capacitors above the four power rails: vdda_dll0_lpddr21, vdda_dll1_lpddr21, vdda_dll0_lpddr22, and vdda_dll1_lpddr22.

3.4.1.3.2 Analog Voltage Decoupling—Example Of Video DAC / HDMI Routing Guidelines

The VDAC LDO within the TWL6030 PMIC device supplies the Video DAC and HDMI (vdda_hdmi_vdac OMAP4 power pin) circuitry within the OMAP4 device. This power rail must be routed as a power trace from the LDO where it is star-routed to OMAP as shown in Figure 3-3, *VDAC / HDMI Power PCB Routing Topology*.

For each power trace between the TWL6030 PMIC device and OMAP4 vdda_hdmi_vdac:

- Maximum recommended resistance (VDDA + VSSA) by power supply rail must be 0.3 Ω.
- Maximum recommended inductance by power supply rail less than 2 nH (VDD + VSS) must be 30 nH

Each decoupling capacitor must be located as close as possible to the OMAP4 power balls to reduce the decoupling capacitor loop inductance:

- Maximum loop inductance for the decoupling capacitors must not exceed:
  – Video DAC: less than 2 nH between their location on trace and the device power balls
  – HDMI: less than 1.5 nH between their location on trace and the devices power balls

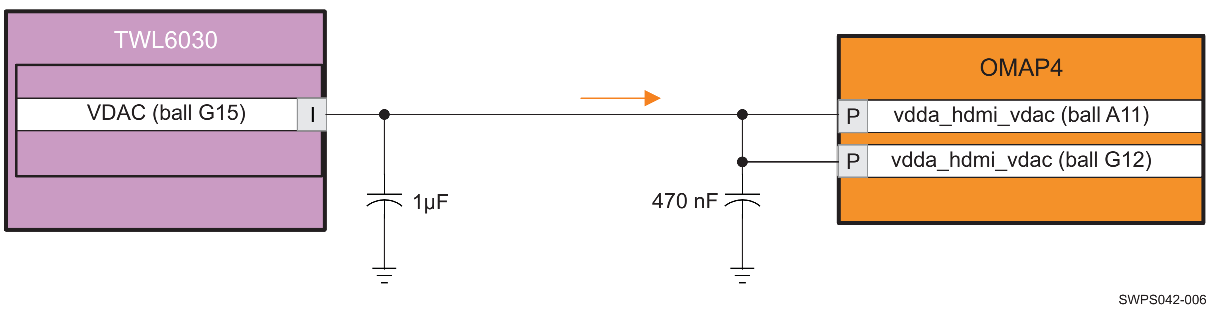

Figure 3-3. VDAC / HDMI Power PCB Routing Topology

3.4.1.3.3 Analog Voltage Decoupling—Example Of VCXIO and VUSB Routing Guidelines

This section provides an example of VCXIO and VUSB routing guidelines based on a TWL6030 PMIC.

The TWL6030 PMIC power companion provides an LDO (VCXIO) that is used to power the DPLLs within the OMAP4 device, as well as the VDDA inputs to the complex I/O cells (except VDAC and HDMI) used within the OMAP4.

Another LDO VUSB provides the 3.3-V supply for the USBPHY (to the OMAP4 vdda_usba0otg_3p3v power pin).

Both LDOs must be routed as a power trace and star-routed to the OMAP4 as shown in Figure 3-4, *DPLLs / Complex I/Os VDDA Power PCB Routing Topology*.

For each power trace between TWL6030 PMIC device and the DPLLs, complex IOs power balls:

- Maximum recommended resistance (VDDA + VSSA) by power supply rail must be 0.3 Ω.
- Maximum recommended inductance by power supply rail less than 2 nH (VDD + VSS) must be 30 nH

Each decoupling capacitor must be located as close as possible to the OMAP4 power balls to reduce the decoupling capacitor loop inductance:

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- Maximum loop inductance for the decoupling capacitors must not exceed:
  - Complex IOs: less than 2 nH between their location on trace and the device power balls
  - DPLLs: less than 1.5 nH between their location on trace and the devices power balls

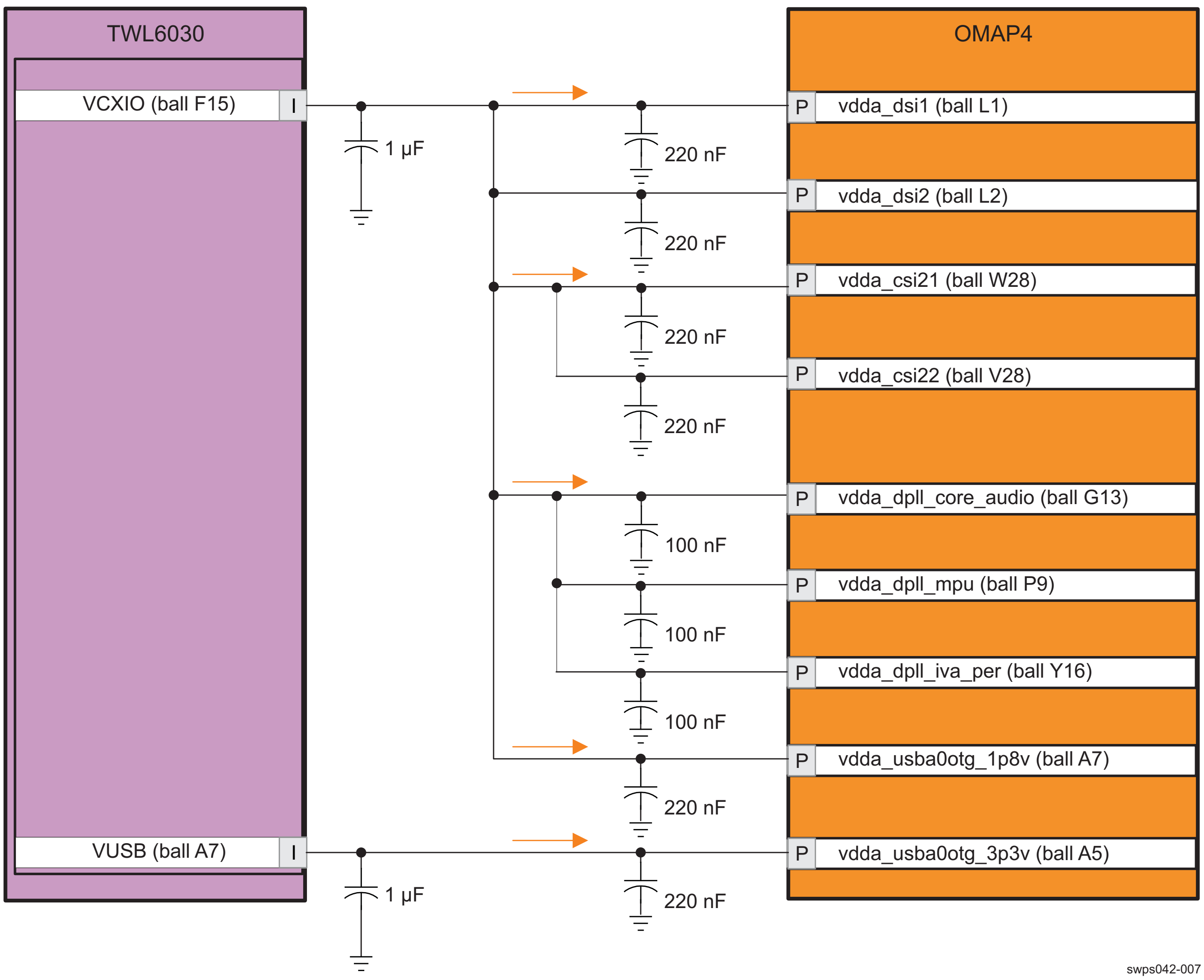

Figure 3-4. DPLLs / Complex I/Os VDDA Power PCB Routing Topology

3.4.1.3.4 Analog Voltage Decoupling—Example Of OMAP4 Embedded LDOs / BandGap Routing Guidelines

This section provides an example of OMAP4 embedded LDOs / BandGap routing guidelines based on a TWL6030 PMIC.

The TWL6030 PMIC power companion provides an SMPS that supplies the IOs and the power management IPs within the OMAP4 device.

This section describes only PCB requirements for embedded OMAP4 LDOs and Bandgap that supply the memories inside the OMAP4.

Both LDOs must be routed as a power trace and star-routed to the OMAP4 as shown in Figure 3-5, *OMAP Embedded LDO / Bandgap Power PCB Routing Topology*. For each power trace between TWL6030 PMIC device and the DPLLs, complex IOs power balls:

- Maximum recommended resistance (VDDA + VSSA) by power supply rail must be 0.3 Ω.
- Maximum recommended inductance by power supply rail less than 2 nH (VDD + VSS) must be 30 nH

Each decoupling capacitor must be located as close as possible to the OMAP4 power balls to reduce the decoupling capacitor loop inductance:

- Maximum loop inductance for the decoupling capacitors must not exceed:
  - Complex IOs: less than 2 nH between their location on trace and the device power balls
  - DPLLs: less than 1.5 nH between their location on trace and the devices power balls

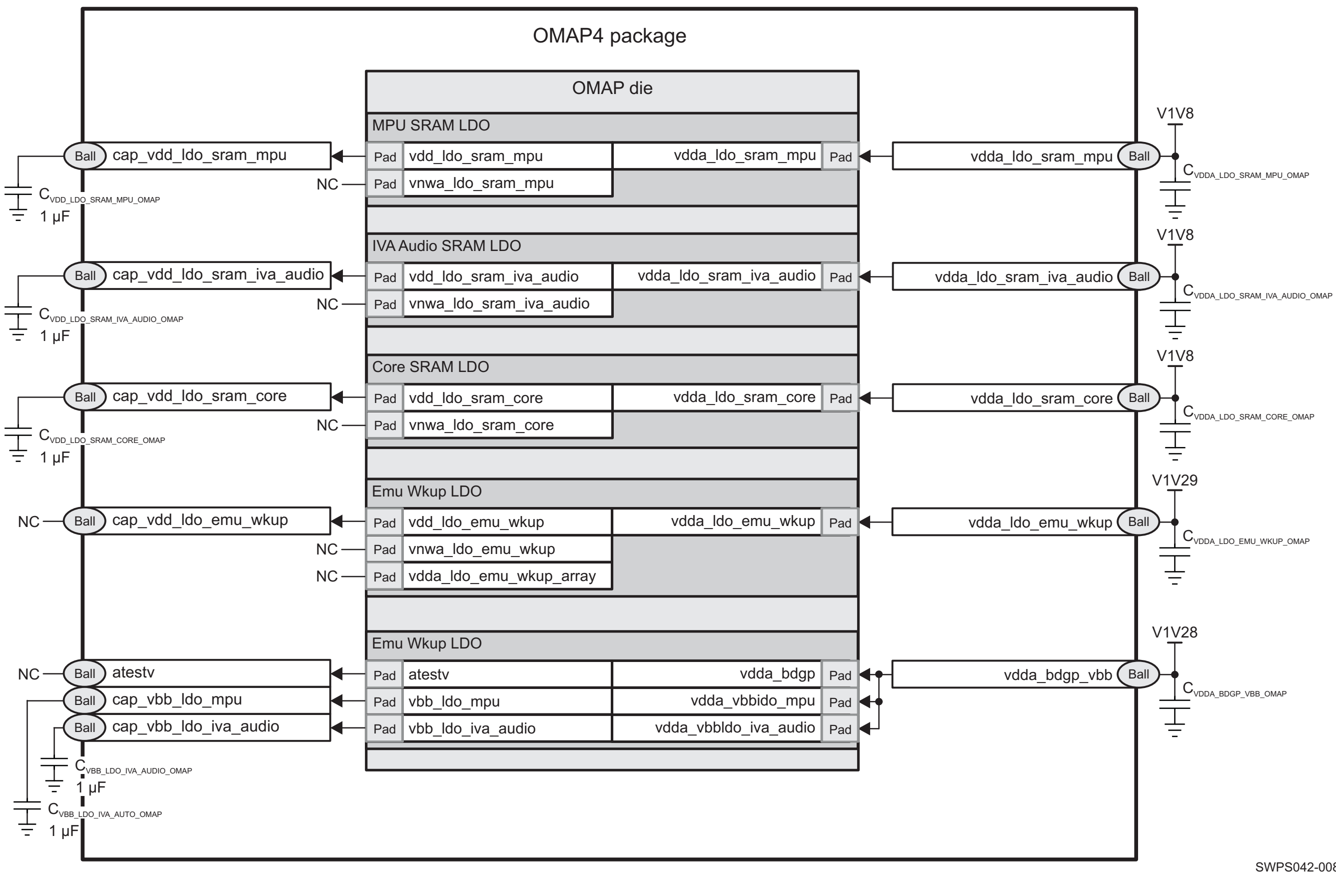

Figure 3-5. OMAP Embedded LDO / Bandgap Power PCB Routing Topology

3.4.1.3.4.1 Analog Voltage Decoupling—Example Of Routing Guidelines For Power Supplies

The SMPS must be routed as a power trace and star-routed to the OMAP4 balls.

Dedicated power traces are star connected from the V1V8 power ball to OMAP4 power balls vdda_ldo_sram_mpu, vdda_ldo_sram_iva_ audio, vdda_ldo_sram_core, vdda_ldo_emu_wkup, and vdda_bdgp_vbb:

- Maximum recommended resistance (VDDA + VSSA) by power supply rail must be 0.3 Ω.
- Maximum recommended inductance by power supply rail less than 2 nH (VDD + VSS) must be 30 nH.

Each decoupling capacitor must be located as close as possible to the OMAP4 power balls to reduce the decoupling capacitor loop inductance.

Maximum loop inductance for the decoupling capacitors must not exceed 2 nH.

3.4.1.3.4.2 Analog Voltage Decoupling—Guidelines For Embedded DLLs

The total capacitors for the 4 DLL power supplies balls (vdda_dll0_lpddr21, vdda_dll1_lpddr21, vdda_dll0_lpddr22, vdda_dll1_lpddr22) must be 3 x 100 nF.

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The capacitors must be placed as closed as possible to the balls.

Maximum loop inductance for the decoupling capacitances must not exceed 1 nH.

3.4.1.3.4.3 Analog Voltage Decoupling—Guidelines For Top LPDDR2 Memories Core Power Supplies

The OMAP4 device supports two LPDDR2 channels. Each of these channels supports up to two chip selects and up to four LPDDR2 memory dies can be connected on top of OMAP4 package in a Package on Package [POP] implementation. Power for LPDDR2 memory is connected via feedthrough in the OMAP4 package.

Depending upon the LPDDR2 memory configuration, TI recommends contacting Memory Vendors for the proper decoupling scheme. As a reference point based on TI board, LPDDR2 VDD1 has 3 x 100 nF and LPDDR2 VDD2 has 2 x 470 nF + 3 x 100 nF.

3.4.2 Output Capacitors

The capacitors at outputs are required to stabilize the internal LDO supply voltages. The capacitors must be placed as closed as possible to the balls.

Table 3-24 summarizes the output capacitor characteristics.

CAUTION

PCB guidelines:

- The capacitors must be placed as closed as possible to the balls. Maximum loop inductance for the decoupling capacitances must not exceed:
  - 1 nH maximum for output SRAM LDOs.
  - 3 nH maximum for output BodyBias (BB) LDOs.

Table 3-24. Output Capacitor Characteristics(1)

PARAMETER	MIN(3)	TYP	MAX(3)	UNIT
$C_{cap\_vbb\_ldo\_mpu}$	0.7	1.0	1.3	μF
$C_{cap\_vbb\_ldo\_iva\_audio}$	0.7	1.0	1.3	μF
$C_{cap\_vdd\_ldo\_sram\_mpu}$	0.7	1.0	1.3	μF
$C_{cap\_vdd\_ldo\_sram\_iva\_audio}$	0.7	1.0	1.3	μF
$C_{cap\_vdd\_ldo\_sram\_core}$	0.7	1.0	1.3	μF
$C_{cap\_vdd\_ldo\_emu\_wkup}$	NA(2)	NA(2)	NA(2)	NA(2)

(1) Output capacitors side code (TCC): 0402/X5R

(2) Caution: It is recommended to avoid adding any external capacitor.

(3) To take into account the aging effects and voltage impact on capacitance, their values, as described in Table 3-24, are specified at ± 50%.

Figure 3-6 and Figure 3-7 illustrate an example of external capacitors.

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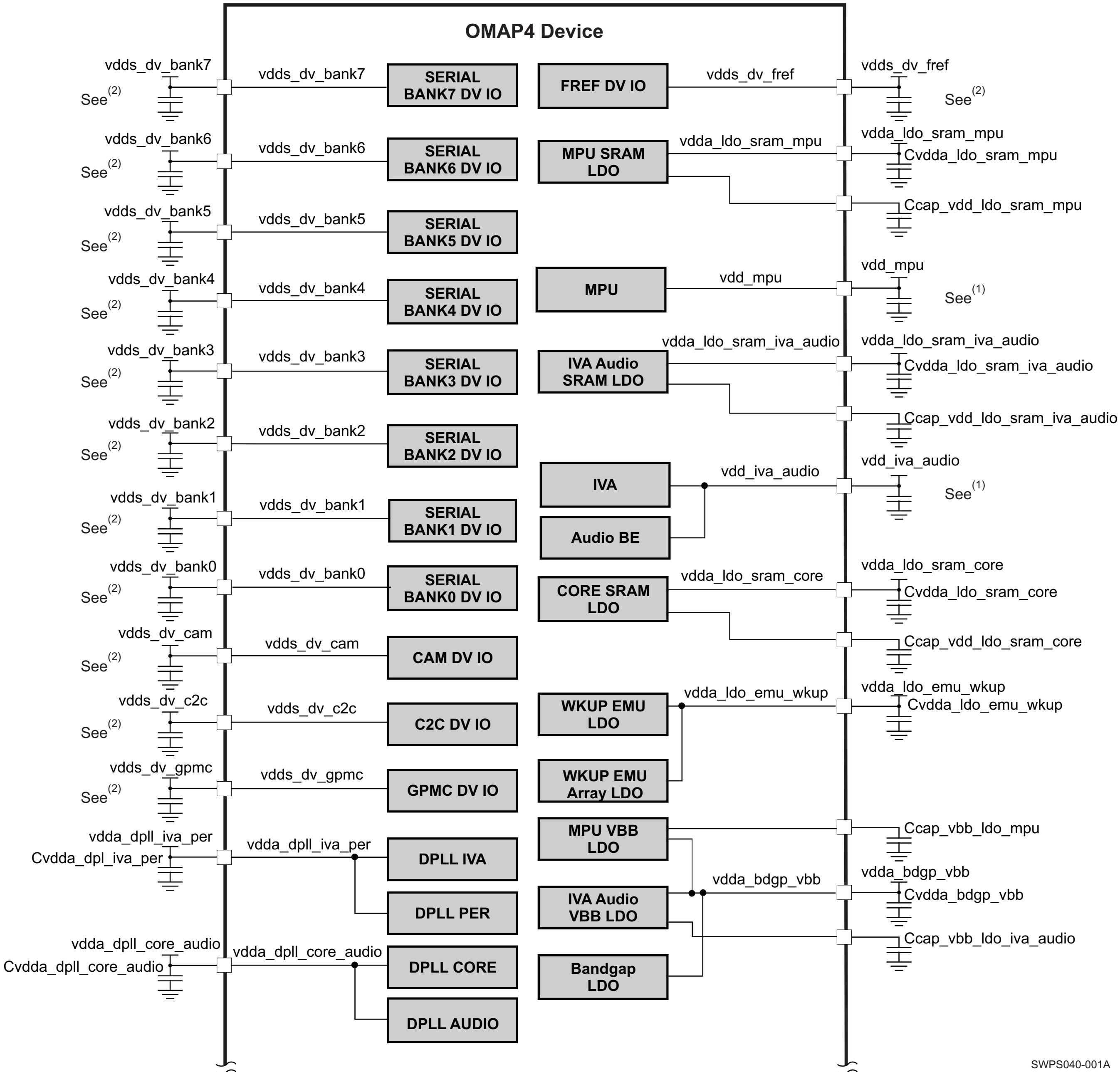

Figure 3-6. External Capacitors—Page 1 of 2(1)(2)

(1) The vdd_mpu, vdd_iva_audio and vdd_core decoupling capacitors placement depends on the board layout. The recommended number of decoupling capacitors is described in Table 3-21, *Core, MPU, IVA, Audio Voltage Decoupling Characteristics.*

(2) The decoupling capacitors placement of the gpmc, sdmmc2, c2c, cam, bank[7:0], fref VDDS dual voltages (dv) depends on the board layout. The number of decoupling capacitors to be used is described in Table 3-22, *IO Voltage Decoupling Characteristics.* Regarding the vddq_vref_lpddr2 and vddca_vref_lpddr2 decoupling capacitors requirement, see also Table 3-22, *IO Voltage Decoupling Characteristics.*

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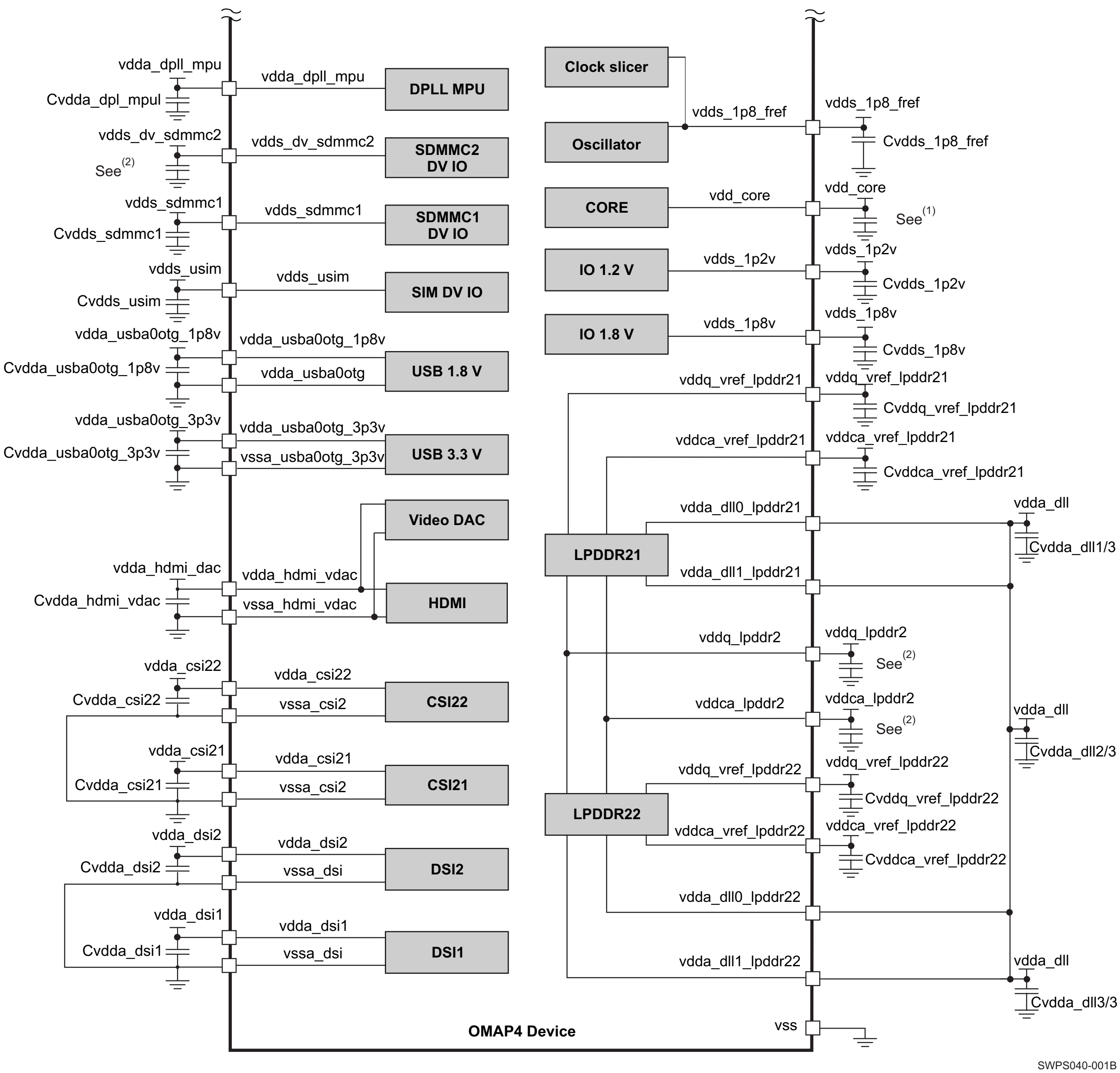

Figure 3-7. External Capacitors—Page 2 of 2(1)(2)

(1) The vdd_mpu, vdd_iva_audio and vdd_core decoupling capacitors placement depends on the board layout. The recommended number of decoupling capacitors is described in Table 3-21, *Core, MPU, IVA, Audio Voltage Decoupling Characteristics.*

(2) The decoupling capacitors placement of the gpmc, sdmmc2, c2c, cam, bank[7:0], fref VDDS dual voltages (dv) depends on the board layout. The number of decoupling capacitors to be used is described in Table 3-22, *IO Voltage Decoupling Characteristics.* Regarding the vddq_vref_lpddr2 and vddca_vref_lpddr2 decoupling capacitors requirement, see also Table 3-22, *IO Voltage Decoupling Characteristics.*

NOTE

vddq_vref_lpddr21 and vddq_vref_lpddr22 are the supply voltage for LPDDR2 DQ VREF:

- Channel 1 on ball G15
- Channel 2 on ball T8

vddca_vref_lpddr21 and vddca_vref_lpddr22 are the supply voltage for LPDDR2 CA VREF:

- Channel 1 on ball Y14
- Channel 2 on ball R27

3.5 Power-up and Power-down Sequences

3.5.1 Power-Up Sequence

NOTE

For more information, see Power, Reset and Clock Management / Reset Management Functional Description / Reset Sequences / PRCM Module Power-On Reset Sequence section of OMAP4430 TRM.

Figure 3-8 shows the power-up sequence.

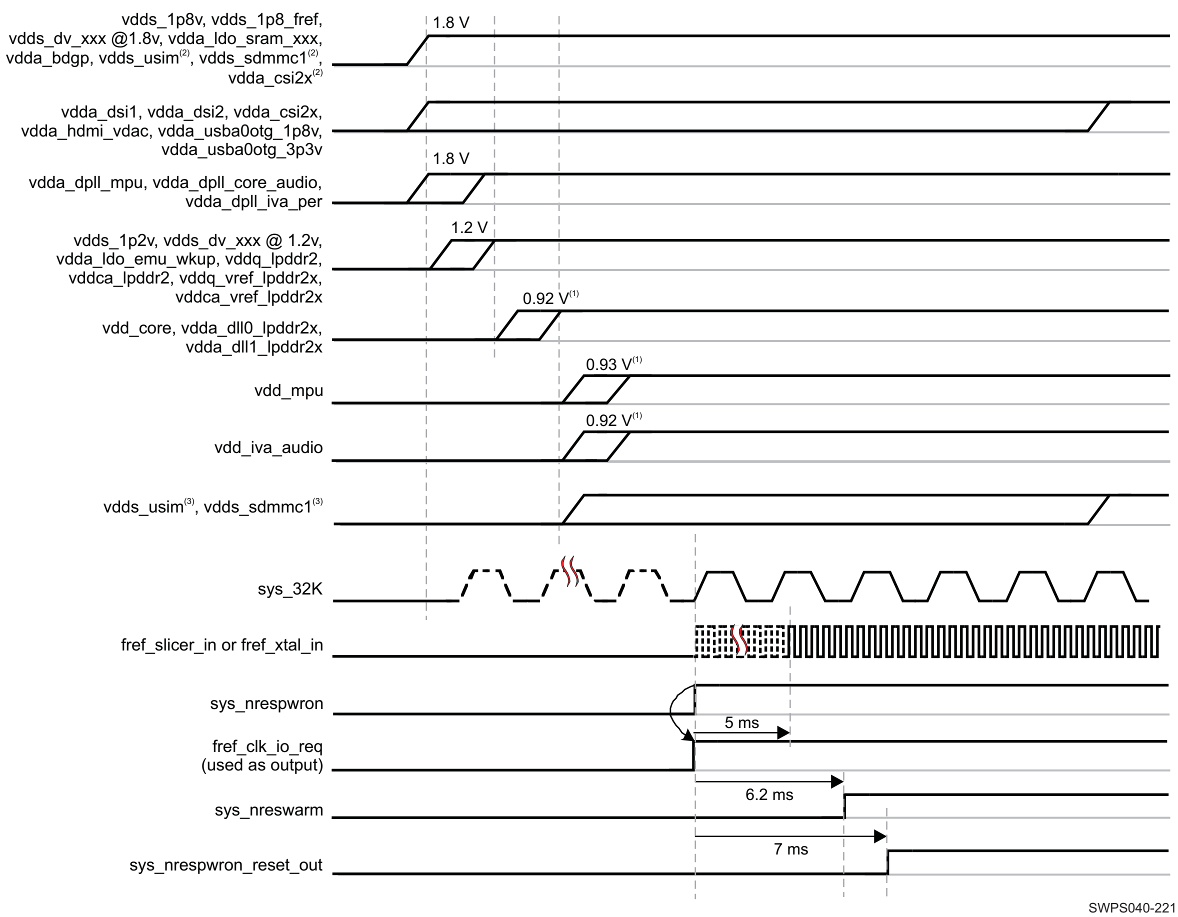

Figure 3-8. Power-Up Sequence

(1) For power saving, the OMAP4430 device boots up with vdd_core, vdd_mpu, and vdd_iva_audio @OPP50. See the operating condition addendum for values. OPP voltage values may change following the silicon characterization result.

(2) In case the USIM, USBC1 interfaces are used at 1.8 V only (for example, USIM and/or USBC1 pads as GPIOs...) or the SDMMC1

interface is used at 1.8 V only (for example, as GPIOs or for SDIO device or eMMC device…) or the CSI2 interfaces are used as GPIs.
(3) In case the USIM, USBC1, SDMMC1 functional signals are used at 1.8 V / 3.0 V.

NOTE

When supplied at 1.8 V, the vdds_dv_xxx dual-voltage supplies (xxx represents bank[7:0], gpmc, sdmmc2, c2c, cam, fref) must be turned on before the one supplied at 1.2 V. Only exception is vdds_dv_c2c that can be turned on at any time (including after OMAP boot), whatever its voltage.

Inside a vdds_dv group @1.8 V or @ 1.2 V, each vdds_dv_xxx supply voltage can be turned on any time compared with the other vdds_dv_xxx supplies voltage.

The vdda_dpll_xxx voltage supplies can be turned on at the same time as the other 1.8-V voltage supplies.

The 1.8-V and 3.3-V PHY voltage supplies can be turned on at the same time as the other 1.8-V voltage supplies or only when the corresponding applications are needed.

Once vdda_ldo_emu_wkup is turned on, vdd_core can be turned on. Once vdd_core is turned on, vdd_mpu and vdd_iva_audio can be turned on.

If the USIM, USBC1, SDMMC1 functional signals are used at 1.8-V / 3.0-V, the vdds_usim, vdds_sdmmc1 voltage supplies can be turned on any time after vdd_core ramp-up or only when the applications are needed.

sys_32k can be turned on any time between vdds_1p8v ramp-up and sys_nrespwron release.

Once the sys_nrespwron is released, OMAP4430 activates the fref_clk_ioreq signal. Therefore, the fref_slicer_in or fref_xtal_in clock can be turned on. (Nevertheless, the system can turn on the fref_slicer_in or fref_xtal_in clock before the fref_clk_ioreq activation provided the vdds_1p8v supply is on.)

5 ms after the sys_nrespwron release, the clock is considered as stabilized on the OMAP4430 slicer input or crystal input. The clock may be supplied later provided it is perfectly stabilized when supplied.

1.2 ms (about 40 additional 32-kHz clock cycles) after the clock is considered as stabilized, OMAP4430 releases its sys_nreswarm.

2 ms after the clock is considered as stabilized, OMAP4430 activates the sys_pwron_reset_out signal.

3.5.2 Power-Down Sequence

The following steps give two examples of power-down sequence supported by the OMAP4430 device.

1. Put the OMAP4430 device under reset (sys_nrespwron)
2. Stop all signals driven to its balls (sys_32k, fref_slicer_in or fref_xtal_in)
3. Either:
   (a) Shutdown all power domains at once. This sequence is described in black color in Figure 3-9.
   (b) Or, if the shutdown is sequenced, you must follow these steps (described in dashed blue color in Figure 3-9):
      (i) Turn off all PHY power supplies and SIM/SDMMC1 IO power supplies
      (ii) Turn off the IVA and AUDIO domains power supplies
      (iii) Turn off the MPU domain power supply
      (iv) Turn off the CORE domain power supply and all DLL power supplies
      (v) Turn off all DPLL power supplies
      (vi) Turn off all 1.2-V IO power supplies
      (vii) Turn off all 1.8-V IO power supplies

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Figure 3-9 shows both power-down sequences: one of them is described in black color, and the other one in dashed blue color.

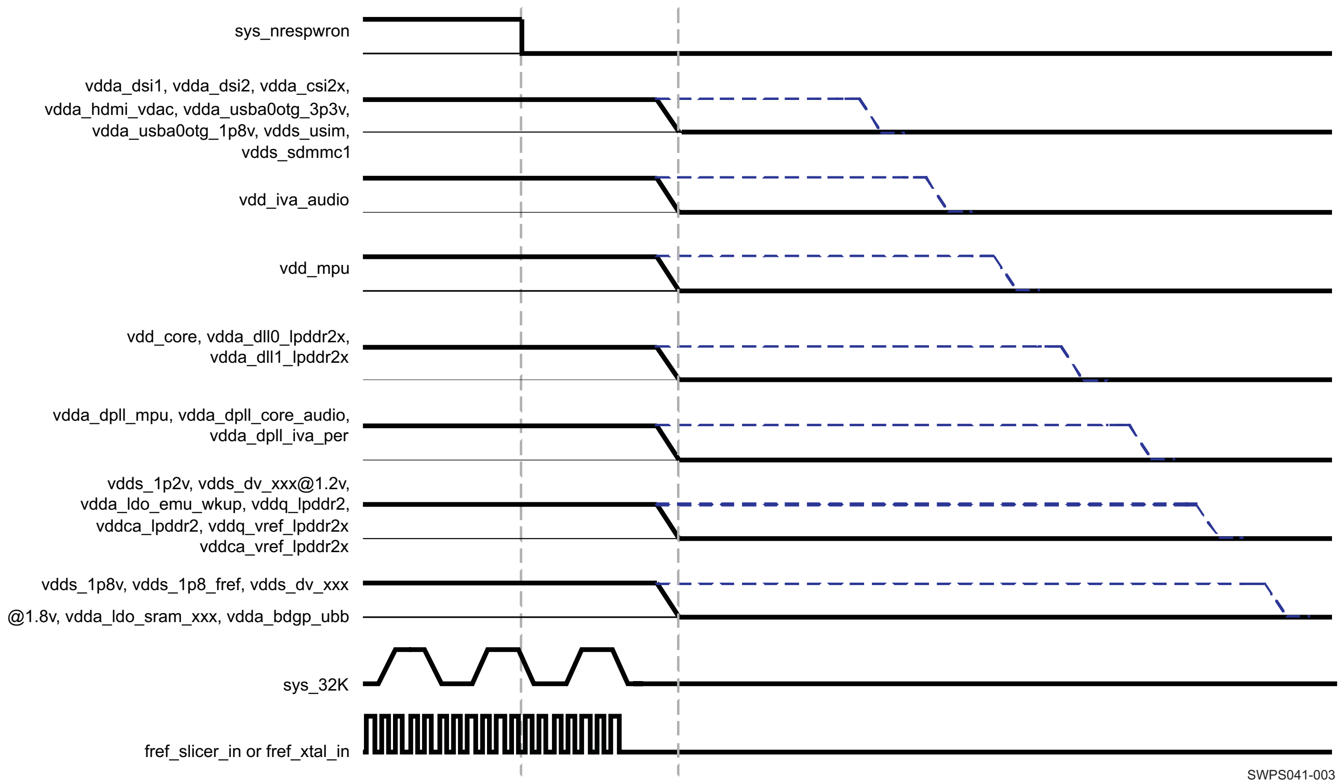

Figure 3-9. Power-Down Sequence

NOTE

sys_32k can be turned off any time between sys_nrespwron assertion and vdds_1p8v shutdown.

fref_slicer_in or fref_xtal_in can be turned off any time between sys_nrespwron assertion and vdds_1p8v shutdown.

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4 Clock Specifications

NOTE

For more information, see Power Reset and Clock Management / PRCM Environment / External Clock Signal and Power Reset / PRCM Functional Description / PRCM Clock Manager Functional Description section of the OMAP4430 TRM.

The OMAP4430 device operation requires the following input clocks: 32-kHz clock (sys_32k) and either slicer clock (fref_slicer_in) or crystal clock (fref_xtal_in / fref_xtal_out). fref_slicer_in and fref_xtal_in / fref_xtal_out at the same time is not a possible configuration. Here is the description of the three input clocks:

- The sys_32k input clock (32-kHz) is used for low frequency operation. It supplies the wake-up domain for operation in lowest power mode (off mode) and the clock source for the DPLL audio back-end DPLL.
- The fref_xtal_in input clock (12, 13, 16.8, 19.2, 26, or 38.4 MHz) is used as a system input clock to generate the source clock of the OMAP4430 device. It supplies the DPLLs as well as several OMAP modules. The system input clock can be connected to either:
  - A crystal oscillator clock (12-MHz, 13-MHz, 16.8-MHz, 19.2-MHz) managed by fref_xtal_in and fref_xtal_out. In this case, the fref_clk_ioreq is used as an input (GPIN).
  - A CMOS digital clock through the fref_xtal_in pin. In this case, the fref_clk_ioreq is used as an output to request the external system clock.
  - In these two cases, the fref_slicer_in input can be used to provide the OMAP4430 device with an alternate input clock up to 38.4 MHz (for example, for the 27-MHz VENC clock).
- The fref_slicer_in input clock (12-MHz, 13-MHz, 16.8-MHz, 19.2-MHz, 26-MHz, and 38.4-MHz) is also used as a system input clock to generate the source clock of the OMAP4430 device. It supplies the DPLLs as well as several OMAP4430 modules. The system input clock can be connected to either:
  - A single-ended sine clock, through the fref_slicer_in pin, which is converted by the internal slicer to a digital square clock. In this case, the fref_clk_ioreq is used an output to request the external system clock.
  - A CMOS digital clock through the fref_slicer_in pin. In this case, the fref_clk_ioreq is used as an output to request the external system clock.
  - In these two cases, the fref_xtal_in input can be used to provide the OMAP4430 device with an alternate input clock up to 100 MHz (for example, for the 54-MHz VENC clock).

The OMAP4430 outputs externally six clocks:

- fref_clk1_out is specially targeted for the primary camera sensor functional input clock.
- fref_clk2_out is for the secondary camera sensor functional input clock.
- fref_clk0_out, fref_clk3_out, fref_clk4_out, and fref_clk5_out are also available to supply input clocks for the other peripherals.

After the reset sequence, fref_clk4_out output clock is activated by default whatever the request level from fref_clk4_req signal. fref_clk5_out output clock is active only if fref_clk4_out output clock is deactivated (no request from fref_clk4_req signal). fref_clk1_out and fref_clk2_out output clocks are not always-on clocks.

Figure 4-1 shows the external input clock sources and the output clocks to peripherals.

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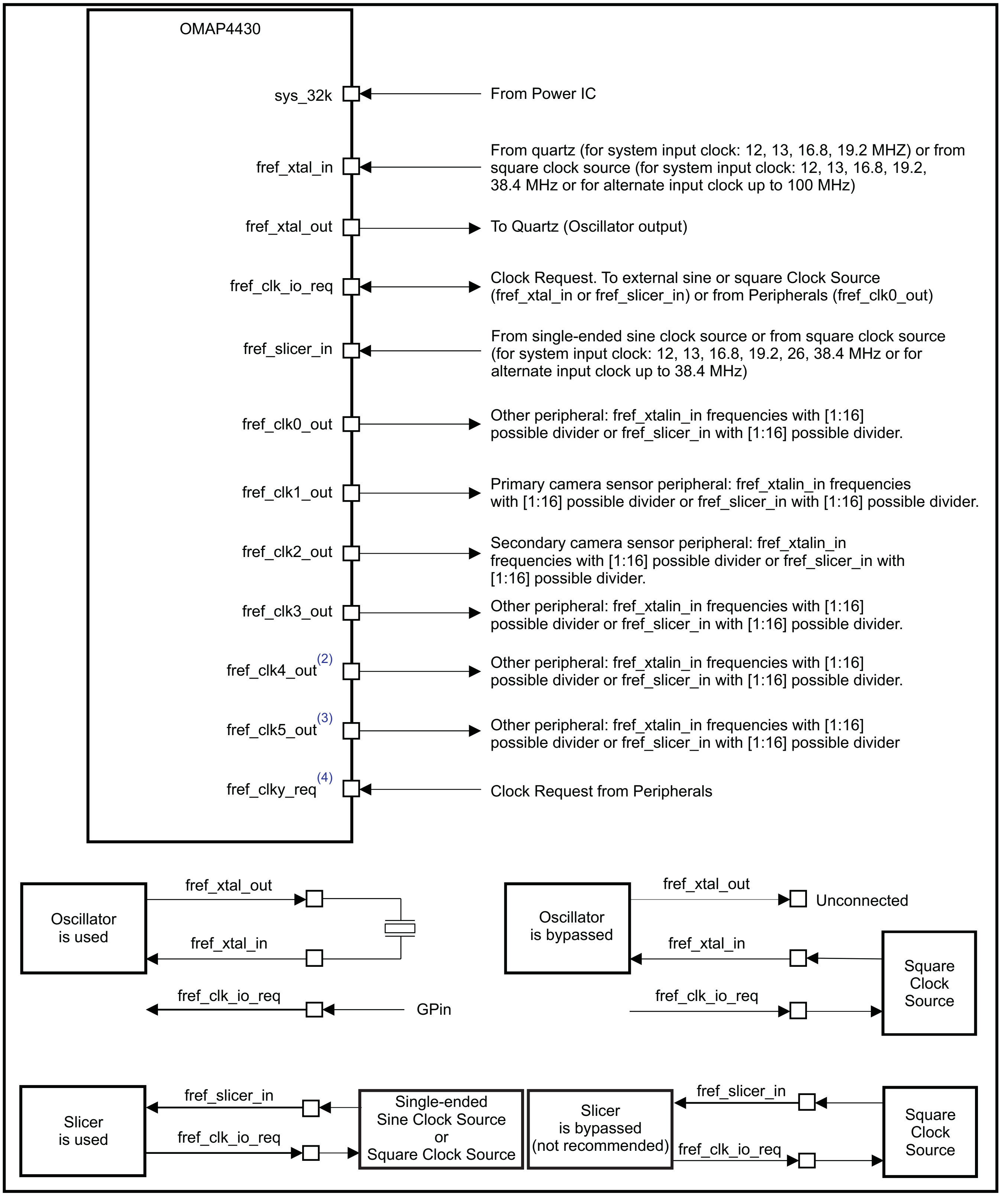

Figure 4-1. Clock Interface[1][2][3][4][5]

(1) After the reset sequence, fref_clk4_out output clock is activated by default whatever the request level from fref_clk4_req signal.

(2) fref_clk5_out output clock is active only if fref_clk4_out output clock is deactivated (no request from fref_clk4_req signal). fref_clk4_out on by default at system boot.

(3) fref_clk1_out and fref_clk2_out output clocks are not Always-On clocks.

(4) In fref_clky_req, y = [4;0]. fref_clk[1:5]_req: fref_clkx_req is clock request associated by default to fref_clkx_out. Can be associated to any fref_clk[1:5]_out by software.

(5) When an oscillator is used, fref_clk_ioreq is associated by default to fref_clk0_out.

4.1 Input Clock Specifications

4.1.1 Input Clock Requirements

Table 4-1 illustrates the requirements to supply an input clock to the device.

Table 4-1. Input Clock Requirements[(4)]

PAD	CLOCK FREQUENCY			STABILITY	DUTY CYCLE	JITTER	TRANSITION
sys_32k	32.768-kHz			± 200 ppm	See [(5)]	See [(5)]	< 30 ns
fref_xtal_in fref_xtal_out	12-, 13-, 16.8-, or 19.2-MHz		Crystal Clock	± 50 (±5) ppm[(3)]	NA	NA	NA
	12-, 13-, 16.8-, 19.2-, 26-, or 38.4-MHz		Square Clock	± 50 (±5) ppm[(3)]	45% to 55%	1% * $t_{c(XTALIN)}$[(2)] (ps) * Xdiv[(1)] – 257.9468 (ps)	< 5 ns
fref_slicer_in fref_clk0_out	12-, 13-, 16.8-, 19.2-, 26-, or 38.4-MHz	Active Mode	Single-ended Sine clock	± 50 (±5) ppm[(3)]	38.5% to 61.5%	1% * $t_{c(SLICER)}$[(2)] (ps) * Xdiv[(1)] – 300 ps	NA
			Square Clock	± 50 (±5) ppm[(3)]	45% to 55%	1% * $t_{c(SLICER)}$[(2)] (ps) * Xdiv[(1)] – 265.7864 (ps)	< 10 ns
		Bypass Mode	Square Clock	± 50 (±5) ppm[(3)]	47% to 53%	1% * $t_{c(SLICER)}$[(2)] (ps) * Xdiv[(1)] – 265.7864 (ps)	< 10 ns

(1) In Xdiv, Xdiv represents the internal DSS DPLLs dividers. [$t_{c(XTALIN)}$ (ps) * Xdiv] or [$t_{c(SLICER)}$ (ps) * Xdiv] represents the input clock cycle coming to the DSS DPLLs (that means after dividing). For the other internal DPLLs, the Xdiv value is equal to 1.
Note that this input jitter limitation comes from the DPLL constraint shifted at ball level. To t clarify this formula, please consider a maximum jitter of 1% of the clock period coming to the internal DPLL (input DPLL).
For more information, see the Power, Reset and Clock Management / Clock Management Functional Description / Internal Clock Sources/Generators / PRM Clock Source section of the OMAP4430 TRM.

(2) $t_{c(SLICER)}$ is the fref_slicer_in cycle time of the clock coming to fref_slicer_in ball.
$t_{c(XTALIN)}$ is the fref_xtal_in cycle time of the clock coming to fref_xtalin_in ball.

(3) ±50 ppm is the clock frequency stability/accuracy and ±5 ppm takes into account the aging effects.

(4) In this table the rise and fall times are calculated for 10% to 90% of VDDS. For more information on the corresponding OMAP4 VDDS power supply name, see Table 2-1, POWER [9] column with the ball name.

(5) sys_32k is a slow clock that means with no stringent duty cycle and jitter requirements. Otherwise, based on the DPLL requirements, you can consider a maximum input duty cycle of [40% to 60%] of the clock period and a maximum jitter at DPLL input of 1% of the clock period coming to the DPLL.

4.1.2 sys_32k CMOS Input Clock

Table 4-2 summarizes the electrical characteristics of the sys_32k input clock.

Table 4-2. sys_32k Input Clock Electrical Characteristics

NAME	DESCRIPTION	MIN	TYP	MAX	UNIT
f	Frequency, sys_32k		32.768		kHz
C_i	Input capacitance			1.3	pF
R_i	Input resistance	3		10	GΩ

Table 4-3 details the input requirements of the sys_32k input clock.

Table 4-3. sys_32k Input Clock Timing Requirements(1)(2)

NAME	DESCRIPTION		MIN	TYP	MAX	UNIT
CK0	$1 / t_{c(32k)}$	Frequency, sys_32k		32.768		kHz
	$t_{R(32k)}$	Rise time, sys_32k			30	ns
	$t_{F(32k)}$	Fall time, sys_32k			30	ns
	$t_{j(32k)}$	Frequency stability, sys_32k			200	ppm

(1) See Table 3-20, *System DC Electrical Characteristics*, SYS (clk32k …) part for sys_32k V_{IH}/V_{IL} parameters.

(2) In this table the rise and fall times are calculated for 10% to 90% of VDDS. For more information on the corresponding OMAP4 VDDS power supply name, see Table 2-1, POWER [9] column with the ball name.

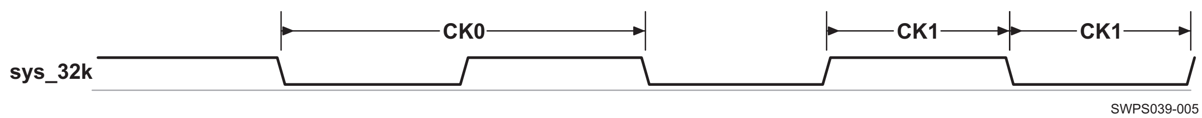

Figure 4-2. sys_32k Input Clock

4.1.3 *fref_xtalin CMOS Input Clock*

4.1.3.1 fref_xtal_in / fref_xtal_out External Crystal

An external crystal is connected to the device pins. Figure 4-3 describes the crystal implementation.

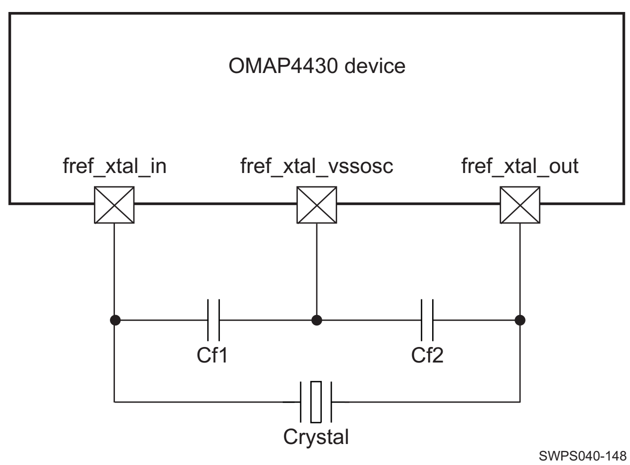

Figure 4-3. Crystal Implementation(1)

(1) When the oscillator is bypassed, the fref_xtal_in ball is connected to a square clock source, the fref_xtal_out ball is not connected and the fref_xtal_vssosc ball is connected to the ground.
When the oscillator is not used, the fref_xtal_in and fref_xtal_out balls can be connected to the ground, or not connected and the fref_xtal_vssosc ball is connected to the ground.

The crystal must be in the fundamental mode of operation and parallel resonant. Table 4-4 summarizes the required electrical constraints.

Table 4-4. Crystal Electrical Characteristics(2)

NAME	DESCRIPTION	MIN	TYP	MAX	UNIT
f_p	Parallel resonance crystal frequency		12, 13, 16.8, or 19.2		MHz
C_{f1}	C_{f1} load capacitance for crystal parallel resonance with $C_{f1} = C_{f2}$	12		24	pF
C_{f2}	C_{f2} load capacitance for crystal parallel resonance with $C_{f1} = C_{f2}$	12		24	pF

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Table 4-4. Crystal Electrical Characteristics[(2)] (continued)

NAME	DESCRIPTION	MIN	TYP	MAX	UNIT
ESR(C_{f1},C_{f2})[(1)]	Frequency 12 MHz, Negative resistor at nominal 500 Ω, Negative resistor at worst case 300 Ω			100	Ω
	Frequency 13 MHz, Negative resistor at nominal 400 Ω, Negative resistor at worst case 240 Ω			80	
	Frequency 16.8 MHz and 19.2 MHz, Negative resistor at nominal 300 Ω, Negative resistor at worst case 180 Ω			60	
C_o	Crystal shunt capacitance			4.5	pF
L_m	Crystal motional inductance for f_p = 12 MHz		16		mH
C_m	Crystal motional capacitance		10.87		fF
DL	Crystal drive level			0.5	mW

(1) Measured with the load capacitance specified by the crystal manufacturer. This load is defined by the foot capacitances tied in series. If C_L = 20 pF, then both foot capacitors will be C_{f1} = C_{f2} = 40 pF. Parasitic capacitance from package and board must also be taken in account.

(2) The crystal motional resistance R_m is related to the equivalent series resistance (ESR) by the following formula: $ESR = R_m * (1 + (C_O * C_{f1} * C_{f2} / (C_{f1} + C_{f2})))^2$.

When selecting a crystal, the system design must take into account the temperature and aging characteristics of a crystal versus the user environment and expected lifetime of the system.

Table 4-5 details the switching characteristics of the oscillator and the requirements of the input clock.

Table 4-5. Oscillator Switching Characteristics—Crystal Mode

NAME	DESCRIPTION	MIN	TYP	MAX	UNIT
f_p	Oscillation frequency	12, 13, 16.8, or 19.2			MHz
t_{sX}	Start-up time[(1)(2)]			1.2	ms

(1) Start-up time is defined as the time the oscillator takes to gain fref_xtal_in amplitude enough to have 45% to 55% duty cycle at the core input from the time power down (PWRDN) is released. Start-up time is a strong function of crystal parameters. At power-on reset, the time is adjustable using the pin itself. The reset must be released when the oscillator or clock source is stable. To switch from bypass mode to crystal or from crystal mode to bypass mode, there is a waiting time about 100 µs; however, if the chip comes from bypass mode to crystal mode the crystal will start-up after time mentioned in the t_{sX} parameter.

(2) Before the processor boots up and the oscillator is set to bypass mode, there is a waiting time when the internal oscillator is in application mode and receives a square wave. The switching time in this case is about 100 µs.

4.1.3.2 fref_xtal_in Squarer Input Clock

Table 4-6 summarizes the base oscillator electrical characteristics.

Table 4-6. Oscillator Electrical Characteristics—Bypass Mode

NAME	DESCRIPTION	MIN	TYP	MAX	UNIT
f	Frequency	12, 13, 16.8, 19.2, 26, or 38.4			MHz
C_I	Input capacitance	1.00	1.15	1.35	pF
R_I	Input resistance	160	216	280	Ω
t_{sX}	Start-up time[(1)]	See [(2)]			ms

(1) To switch from bypass mode to crystal or from crystal mode to bypass mode, there is a waiting time about 100 µs; however, if the chip comes from bypass mode to crystal mode the crystal will start-up after time mentioned in Table 4-5, t_{sX} parameter.

(2) Before the processor boots up and the oscillator is set to bypass mode, there is a waiting time when the internal oscillator is in application mode and receives a square wave. The switching time in this case is about 100 µs.

Table 4-7 details the squarer input clock timing requirements.

Table 4-7. fref_xtal_in Squarer Input Clock Timing Requirements—Bypass Mode[(3)]

NAME	DESCRIPTION		MIN	TYP	MAX	UNIT
OCS0	1 / $t_{c(xtalin)}$	Frequency, fref_xtal_in	12, 13, 16.8, 19.2, 26, or 38.4			MHz

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Table 4-7. fref_xtal_in Squarer Input Clock Timing Requirements—Bypass Mode[(3)] (continued)

NAME	DESCRIPTION		MIN	TYP	MAX	UNIT
OCS1	$t_{w(xtalin)}$	Pulse duration, fref_xtal_in low or high	0.45 * $t_{c(XTALIN)}$		0.55 * $t_{c(XTALIN)}$	ns
	$t_{j(xtalin)}$	Peak-to-peak jitter[(1)], fref_xtal_in			1% * $t_{c(XTALIN)}$[(5)] (ps) * Xdiv[(4)] – 257.9468 (ps)	ps
	$t_{R(xtalin)}$	Rise time, fref_xtal_in			5	ns
	$t_{F(xtalin)}$	Fall time, fref_xtal_in			5	ns
	$t_{j(xtalin)}$	Frequency stability, fref_xtal_in			50 (±5)[(2)]	ppm

(1) Peak-to-peak jitter is meant here as follows:
- – The maximum value is the difference between the longest measured clock period and the expected clock period
- – The minimum value is the difference between the shortest measured clock period and the expected clock period

Maximum and minimum are obtained on a statistical population of 300 period samples and expressed relative to the expected clock period.

(2) ±50 ppm is the clock frequency stability/accuracy and ±5 ppm takes into account the aging effects.

(3) In this table the rise and fall times are calculated for 10% to 90% of VDDS. For more information on the corresponding OMAP4 VDDS power supply name, see Table 2-1, POWER [9] column with the ball name.

(4) In Xdiv, Xdiv represents the internal DSS DPLLs dividers. [$t_{c(XTALIN)}$ (ps) * Xdiv] represents the input clock cycle coming to the DSS DPLLs (that means after dividing). For the other internal DPLLs, the Xdiv value is equal to 1.
Note that this input jitter limitation comes from the DPLL constraint shifted at ball level. To clarify this formula, please consider a maximum jitter of 1% of the clock period coming to the internal DPLL (input DPLL).
For more information, see the Power, Reset and Clock Management Functional Description / Internal Clock Sources/Generators / PRM Clock Source section of the OMAP4430 TRM.

(5) $t_{c(XTALIN)}$ is the fref_xtal_in cycle time of the clock coming to fref_xtalin_in ball.

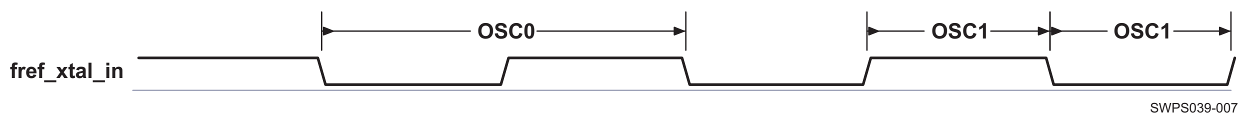

Figure 4-4. fref_xtal_in Squarer Input Clock

4.1.4 *fref_slicer_in Squarer Input Clock*

Table 4-8 summarizes the electrical characteristics of the fref_slicer_in input clock.

Table 4-8. fref_slicer_in Input Clock Electrical Characteristics

NAME	DESCRIPTION	MIN	TYP	MAX	UNIT
f	Frequency, fref_slicer_in	12, 13, 16.8, 19.2, 26, and 38.4			MHz
C_i	Input capacitance			2.5	pF
R_i	Input resistance	14		29	kΩ

Table 4-9 details the input requirements of the fref_slicer_in input clock.

Table 4-9. fref_slicer_in Input Clock Timing Requirements—Bypass Mode[(1)(6)]

NAME	DESCRIPTION			MIN	TYP	MAX	UNIT
SLC0	1 / $t_{c(fref\_slicer\_in)}$	Frequency, fref_slicer_in		12, 13, 16.8, 19.2, 26, and 38.4			MHz
SLC1	$t_{w(fref\_slicer\_in)}$	Pulse duration, fref_slicer_in low or high	Active mode Square clock	0.45 * $t_{c(SLICER)}$		0.55 * $t_{c(SLICER)}$	ns
			Bypass mode Square clock	0.47 * $t_{c(SLICER)}$		0.53 * $t_{c(SLICER)}$	
	$t_{j(fref\_slicer\_in)}$	Peak-to-peak jitter[(2)], fref_slicer_in	Active mode Square clock			1% * $t_{c(SLICER)}$[(4)] (ps) * Xdiv[(3)] – 265.7864 (ps)	ps
			Bypass mode Square clock			1% * $t_{c(SLICER)}$[(4)] (ps) * Xdiv[(3)] – 265.7864 (ps)	

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Table 4-9. fref_slicer_in Input Clock Timing Requirements—Bypass Mode[(1)(6)] (continued)

NAME	DESCRIPTION		MIN	TYP	MAX	UNIT
	$t_{R(fref\_slicer\_in)}$	Rise time, fref_slicer_in	1.5		10	ns
	$t_{F(fref\_slicer\_in)}$	Fall time, fref_slicer_in	1.5		10	ns
	$t_{j(fref\_slicer\_in)}$	Frequency stability, fref_slicer_in			50 (±5)[(5)]	ppm

(1) See Table 3-20, *System DC Electrical Characteristics*, SYS (fref_slicer_in) part for fref_slicer_in V_{IH}/V_{IL} parameters

(2) Peak-to-peak jitter is meant here as follows:
– The maximum value is the difference between the longest measured clock period and the expected clock period
– The minimum value is the difference between the shortest measured clock period and the expected clock period
Maximum and minimum are obtained on a statistical population of 300 period samples and expressed relative to the expected clock period.

(3) In Xdiv, Xdiv represents the internal DSS DPLLs dividers. [$t_{c(SLICER)}$ (ps) * Xdiv] represents the input clock cycle coming to the DSS DPLLs (that means after dividing). For the other internal DPLLs, the Xdiv value is equal to 1.
Note that this input jitter limitation comes from the DPLL constraint shifted at ball level. To clarify this formula, please consider a maximum jitter of 1% of the clock period coming to the internal DPLL (input DPLL).
For more information, see the Power, Reset and Clock Management / Clock Management Functional Description / Internal Clock Sources/Generators / PRM Clock Source section of the OMAP4430 TRM.

(4) $t_{c(SLICER)}$ is the fref_slicer_in cycle time of the clock coming to fref_slicer_in ball.

(5) ±50 ppm is the clock frequency stability/accuracy and ±5 ppm takes into account the aging effects.

(6) In this table the rise and fall times are calculated for 10% to 90% of VDDS. For more information on the corresponding OMAP4 VDDS power supply name, see Table 2-1, POWER [9] column with the ball name.

Table 4-10. fref_slicer_in Input Single-ended Sine Clock Timing Requirements[(1)]

NAME	DESCRIPTION		MIN	TYP	MAX	UNIT
SLC0	1 / $t_{c(fref\_slicer\_in)}$	Frequency, fref_slicer_in	12, 16.8, 19.2, 26, and 38.4			MHz
SLC1	$t_{w(fref\_slicer\_in)}$	Pulse duration, fref_slicer_in low or high	0.385 * $t_{c(SLICER)}$		0.615 * $t_{c(SLICER)}$	ns
	$t_{j(fref\_slicer\_in)}$	Peak-to-peak jitter[(2)], fref_slicer_in			1% * $t_{c(SLICER)}$[(4)] (ps) * Xdiv[(3)] – 300 (ps)	ps
	$t_{j(fref\_slicer\_in)}$	Frequency stability, fref_slicer_in			50 (±5)[(5)]	ppm

(1) See Table 3-5, *DC Electrical Characteristics*, SYS (clk_slicer_in) part for fref_slicer_in V_{IH}/V_{IL} parameters

(2) Peak-to-peak jitter is meant here as follows:
– The maximum value is the difference between the longest measured clock period and the expected clock period
– The minimum value is the difference between the shortest measured clock period and the expected clock period
Maximum and minimum are obtained on a statistical population of 300 period samples and expressed relative to the expected clock period.

(3) In Xdiv, Xdiv represents the internal DSS DPLLs dividers. [$t_{c(SLICER)}$ (ps) * Xdiv] represents the input clock cycle coming to the DSS DPLLs (that means after dividing). For the other internal DPLLs, the Xdiv value is equal to 1.
For more information, see the Power, Reset and Clock Management / Clock Management Functional Description / Internal Clock Sources/Generators / PRM Clock Source section of the OMAP4430 TRM.

(4) $t_{c(SLICER)}$ is the fref_slicer_in cycle time of the clock coming to fref_slicer_in ball.

(5) ±50 ppm is the clock frequency stability/accuracy and ±5 ppm takes into account the aging effects.

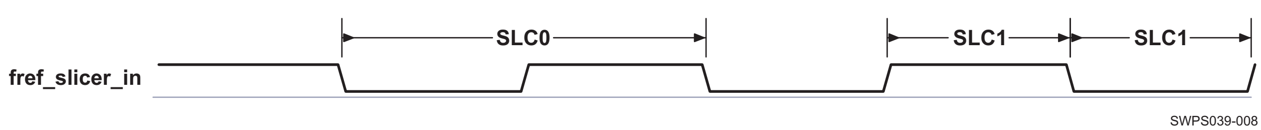

Figure 4-5. fref_slicer_in Input Clock

4.2 Output Clocks Specifications

4.2.1 FREF Output Clocks

Table 4-11 summarizes the electrical characteristics of the fref_clk1_out output clock (specially targeted for the primary camera sensor functional input clock), fref_clk2_out output clock (targeted for the secondary camera sensor functional input clock), and fref_clk0_out, fref_clk3_out, fref_clk4_out, fref_clk5_out output clocks (input clocks for the other peripherals).

Table 4-11. fref_clkx_out Output Clock Electrical Characteristics(1)(3)

NAME	DESCRIPTION	MIN	TYP	MAX	UNIT
f	Frequency, fref_clkx_out	fref_xtal_in clock frequency(2) or fref_slicer_in clock frequency(2)			MHz
MB[0:1] = 11					
LB0 = 1					
C_L	Load capacitance (Transmission line load + Far end load)	20		25	pF
Z_T	Transmission line impedance	30		60	Ω
L_T	Transmission line length	NA		10	cm
D_T	Transmission line delay time	NA		670	ps
LB0 = 0					
C_L	Load capacitance (Transmission line load + Far end load)	14		17	pF
Z_T	Transmission line impedance	30		60	Ω
L_T	Transmission line length	NA		5	cm
D_T	Transmission line delay time	NA		335	ps
MB[0:1] = 01					
LB0 = 1					
C_L	Load capacitance (Transmission line load + Far end load)	23		28	pF
Z_T	Transmission line impedance	30		55	Ω
L_T	Transmission line length	NA		12.5	cm
D_T	Transmission line delay time	NA		838	ps
LB0 = 0					
C_L	Load capacitance (Transmission line load + Far end load)	2		11	pF
Z_T	Transmission line impedance	30		60	Ω
L_T	Transmission line length	NA		8	cm
D_T	Transmission line delay time	NA		536	ps

(1) In fref_clkx_out, x = 0, 1, 2, 3, 4, or 5

(2) Possible clock divisions: [1 to 16]

(3) The modes are configured by 3 bits MB[0:1] and LB0 of the IO cell. For more details, see the OMAP4430 TRM.

Table 4-12 details the fref_clk0_out, fref_clk1_out, fref_clk2_out, fref_clk3_out, fref_clk4_out, and fref_clk5_out output clock switching characteristics.

Table 4-12. fref_clkx_out Output Clock Switching Characteristics(1)(6)

NAME		DESCRIPTION	MIN	TYP	MAX	UNIT
	f	Frequency, fref_clkx_out	fref_xtal_in clock frequency(2) or fref_slicer_in clock frequency(2) or Per/Core DPLL frequency(2)			MHz
FREF0	$t_{c(clkOUT1)}$	Period, fref_clkx_out	fref_xtal_in clock period or fref_slicer_in clock period or Per/Core DPLL period			ns

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Table 4-12. fref_clkx_out Output Clock Switching Characteristics[(1)(6)] (continued)

NAME	DESCRIPTION				MIN	TYP	MAX	UNIT
	t_J	Peak-to-Peak jitter, fref_clkx_out	From fref_xtal_in Core DPLL or Per DPLL bypassed				$t_{J(fref\_xtal\_in)}$[(9)] + 400 ps	ps
			From fref_xtal_in Core DPLL or Per DPLL used				$t_{J(fref\_xtal\_in)}$[(9)] + 340 ps	
			From fref_slicer_in Core DPLL or Per DPLL bypassed				$t_{J(fref\_slicer\_in)}$[(9)] + 440 ps	
			From fref_slicer_in Core DPLL or Per DPLL used				$t_{J(fref\_slicer\_in)}$[(9)] + 310 ps	
	Stability, fref_clkx_out						±50 (±5)[(8)]	ppm
FREF1	$t_{w(clkOUT1)}$	Pulse duration, fref_clkx_out low or high	Divider[(7)] value is even	From fref_xtal_in Core DPLL or Per DPLL bypassed			0.50 * $t_{c(clkOUT1)}$ + [$t_{J(fref\_xtal\_in)}$[(9)] + 400 ps]	ns
				From fref_xtal_in Core DPLL or Per DPLL used			0.50 * $t_{c(clkOUT1)}$ + [$t_{J(fref\_xtal\_in)}$[(9)] + 340 ps]	
				From fref_slicer_in Core DPLL or Per DPLL bypassed			0.50 * $t_{c(clkOUT1)}$ + [$t_{J(fref\_xtal\_in)}$[(9)] + 440 ps]	
				From fref_slicer_in Core DPLL or Per DPLL used			0.50 * $t_{c(clkOUT1)}$ + [$t_{J(fref\_xtal\_in)}$[(9)] + 310 ps]	
			Divider[(7)] value is odd	From fref_xtal_in Core DPLL or Per DPLL bypassed			(divider[(7)] – 1) / (2*divider[(7)]) * $t_{c(clkOUT1)}$ + [$t_{J(fref\_xtal\_in)}$[(9)] + 400 ps]	
				From fref_xtal_in Core DPLL or Per DPLL used			(divider[(7)] – 1) / (2*divider[(7)]) * $t_{c(clkOUT1)}$ + [$t_{J(fref\_xtal\_in)}$[(9)] + 340 ps]	
				From fref_slicer_in Core DPLL or Per DPLL bypassed			(divider[(7)] – 1) / (2*divider[(7)]) * $t_{c(clkOUT1)}$ + [$t_{J(fref\_xtal\_in)}$[(9)] + 440 ps]	
				From fref_slicer_in Core DPLL or Per DPLL used			(divider[(7)] – 1) / (2*divider[(7)]) * $t_{c(clkOUT1)}$ + [$t_{J(fref\_xtal\_in)}$[(9)] + 310 ps]	
MB[0:1] = 11								
LB0 = 1								
	$t_{R(clkOUT1)}$	Rise time, fref_clkx_out			2[(3)(5)]		10.0[(4)]	ns
	$t_{F(clkOUT1)}$	Fall time, fref_clkx_out			2[(3)(5)]		10.0[(4)]	ns
LB0 = 0								
	$t_{R(clkOUT1)}$	Rise time fref_clkx_out			1.5[(3)(5)]		6.7[(4)]	ns
	$t_{F(clkOUT1)}$	Fall time, fref_clkx_out			1.5[(3)(5)]		6.7[(4)]	ns

Table 4-12. fref_clkx_out Output Clock Switching Characteristics[1][6] (continued)

NAME	DESCRIPTION		MIN	TYP	MAX	UNIT
MB[0:1] = 01						
LB0 = 1						
	$t_{R(clkOUT1)}$	Rise time, fref_clkx_out	2.2[3][5]		14.3[4]	ns
	$t_{F(clkOUT1)}$	Fall time, fref_clkx_out	2.2[3][5]		14.3[4]	ns
LB0 = 0						
	$t_{R(clkOUT1)}$	Rise time, fref_clkx_out	0.7[3][5]		10.4[4]	ns
	$t_{F(clkOUT1)}$	Fall time, fref_clkx_out	0.7[3][5]		10.4[4]	ns

(1) In fref_clkx_out, x = 0, 1, 2, 3, 4, or 5

(2) Possible clock divisions: [1 to 16]

(3) At minimum load

(4) At maximum load (maximum frequency: 104 MHz)

(5) **Caution**: this creates EMI parasitics up to 1.2 ns.

(6) In this table the rise and fall times are calculated for 10% to 90% of VDDS. For more information on the corresponding OMAP4 VDDS power supply name, see Table 2-1, POWER [9] column with the ball name.

(7) FREF1 pulse duration varies depending on divider configured in AUXCLK[0:5] register, CLKDIV bitfield.

(8) ±50 ppm is the clock frequency stability/accuracy and ±5 ppm takes into account the aging effects.

(9) $t_{J(fref\_xtal\_in)}$ or $t_{J(fref\_slicer\_in)}$ corresponds to the external jitter coming to the fref_xtal_in or fref_slicer_in input PAD.

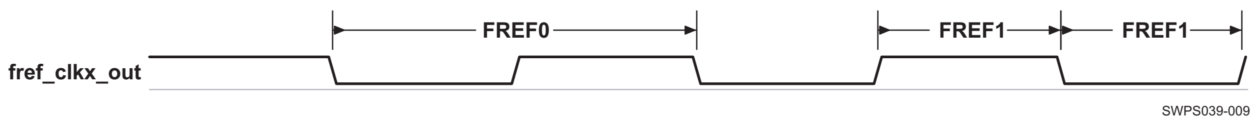

Figure 4-6. fref_clkx_out Output Clocks[1]

(1) In fref_clkx_out, x = 0, 1, 2, 3, 4, or 5

4.3 DPLLs, DLLs Specifications

NOTE

For more information, see:

- Power, Reset and Clock Management / Clock Management Functional / Internal Clock Sources/Generators / Generic DPLL Overview section

  and

- Display Subsystem / Display Subsystem Overview section of the OMAP4430 ES2.x TRM.

The applicative subsystem integrates nine DPLLs and four DLLs. The PRM and CM drive six of them, while the display subsystem controls three other DPLLs (DSI1 DPLL, DSI2 DPLL, and HDMI DPLL).

The six main DPLLs are:

- DPLL1 (MPU)
- DPLL2 (IVA)
- DPLL3 (CORE)
- DPLL4 (PER)
- DPLL5 (ABE)
- DPLL6 (USB)

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NOTE

Of the nine DPLLs embedded in the OMAP4430 device, the DSI1 DPLL, DSI2 DPLL, and HDMI DPLL are controlled directly by the display subsystem.

4.3.1 DPLLs Characteristics

Table 4-13 and Table 4-14 summarize the DPLL characteristics and assume testing over recommended operating conditions.

Table 4-13. DPLL1 / DPLL2 / DPLL3 / DPLL4 / DPLL5 / DSI1 DPLL / DSI2 DPLL Characteristics

NAME	DESCRIPTION	MIN	TYP	MAX	UNIT	COMMENTS
vdda_dpll_iva_per	Supply voltage for DPLLs (IVA and PER)	1.71	1.80	1.89	V	
vdda_dpll_mpu	Supply voltage for DPLL MPU	1.71	1.80	1.89	V	
vdda_dpll_core_audio	Supply voltage for DPLLs (CORE and AUDIO)	1.71	1.80	1.89	V	
vdda_dsi1	Supply voltage for DSI1 DPLL	1.71	1.80	1.89	V	
vdda_dsi2	Supply voltage for DSI2 DPLL	1.71	1.80	1.89	V	
f_{input}	CLKINP input frequency	0.032		52	MHz	FINP
f_{REF}	Internal reference clock frequency	0.032		52	MHz	REFCLK
$f_{CLKINPHIF}$	CLKINPHIF input frequency	10		1000	MHz	FINPHIF
$f_{CLKINPULOW}$	CLKINPULOW input frequency	0.001		800	MHz	
f_{CLKOUT}	CLKOUT output frequency	10[1]		1000[2]	MHz	[M / (N + 1)] * FINP * [1 / M2]
$f_{CLKOUTx2}$	CLKOUTx2 output frequency	20[1]		2000[2]	MHz	2 * [M / (N + 1)] * FINP * [1 / M2]
$f_{CLKOUTHIF}$	CLKOUTHIF output frequency	10[3]		1000[4]	MHz	FINPHIF / M3
		20[3]		2000[4]		2 * [M / (N + 1)] * FINP * [1 / M3]
$f_{CLKDCOLDO}$	Digital controlled oscillator (DCO) output clock frequency	20		2000	MHz	2 * [M / (N + 1)] * FINP
	CLKOUT period jitter	–2.5%		2.5%		The period jitter at the output clocks is ±2.5% peak to peak for REFCLK above or equal to 1 MHz. If REFCLK < 1 MHz, the output jitter is up to ±3%.
	CLKOUTx2 period jitter	–2.5%		2.5%		
	CLKOUTHIF period jitter	–2.5%		2.5%		
	CLKDCOLDO period jitter	–2.5%		2.5%		
t_{lock}	Frequency lock time			1.9 + 350 * REFCLK	µs	
p_{lock}	Phase lock time			1.9 + 500 * REFCLK	µs	
$t_{relock-L}$	Relock time—Frequency lock[5] (Low power bypass)			1.9 + 70 * REFCLK	µs	DPLL in low-power mode: lowcurrstdby = 1
$p_{relock-L}$	Relock time—Phase lock[5] (Low power bypass)			1.9 + 120 * REFCLK	µs	DPLL in low-power mode: lowcurrstdby = 1
$t_{relock-F}$	Relock time—Frequency lock[5] (Fast relock bypass)			0.05 + 70 * REFCLK	µs	DPLL in normal mode: lowcurrstdby = 0
$p_{relock-F}$	Relock time—Phase lock[5] (Fast relock bypass)			0.05 + 120 * REFCLK	µs	DPLL in normal mode: lowcurrstdby = 0

(1) The minimum frequencies on CLKOUT and CLKOUTX2 are assuming M2 = 1.
For M2 > 1, the minimum frequency on these clocks will further scale down by factor of M2.

(2) The maximum frequencies on CLKOUT and CLKOUTX2 are assuming M2 = 1.

(3) The minimum frequency on CLKOUTHIF is assuming M3 = 1. For M3 > 1, the minimum frequency on this clock will further scale down by factor of M3.

(4) The maximum frequency on CLKOUTHIF is assuming M3 = 1.

(5) Relock time assumes typical operating conditions, 10°C maximum temperature drift.

Table 4-14. DPLL6/HDMI DPLL Characteristics

NAME	DESCRIPTION	MIN	TYP	MAX	UNIT	COMMENTS
vdda_usba0otg_1p8v	Supply voltage for USB DPLL	1.71	1.8	1.89	V	
vdda_hdmi_vdac	Supply voltage for HDMI DPLL	1.71	1.8	1.89	V	
f_{input}	Input clock frequency	0.5		60	MHz	FINP
f_{REF}	Internal reference clock frequency	0.5		2.5	MHz	REFCLK = [1 / (N + 1)] * FINP
$f_{CLKINPULOW}$	CLKINPULOW bypass input clock frequency	0.001		800	MHz	Bypass mode (supported by DPLL6): $f_{CLKOUT} = f_{CLKINPULOW}$
$f_{CLKOUTLDO}$	CLKOUTLDO output clock frequency	500(1)		2000(2)	MHz	[M / (N + 1)] * FINP * [1 / M2]
f_{CLKOUT}	CLKOUT output clock frequency	500(1)		2000(2)	MHz	[M / (N + 1)] * FINP * [1 / M2]
$f_{CLKDCOLDO}$	Digital controlled oscillator (DCO) output clock frequency	500		2000	MHz	[M / (N + 1)] * FINP
	CLKOUT period jitter	–2.5%		2.5%		The period jitter at the output clocks is ±2.5% peak to peak
	CLKDCOLDO period jitter	–2.5%		2.5%		
t_{lock}	Frequency lock time			350 * REFCLKs	µs	
p_{lock}	Phase lock time			500 * REFCLKs	µs	
$t_{relock-L}$	Relock time—Frequency lock(3) (Low power bypass)			7.5 + 30 * REFCLKs	µs	
$p_{relock-L}$	Relock time—Phase lock(3) (Low power bypass)			7.5 + 125 * REFCLKs	µs	

(1) The minimum frequency on this clock is assuming M2 = 1.
For M2 > 1, the minimum frequency on this clock will further scale down to 10 MHz by factor of M2.

(2) The maximum frequency on this clock is assuming M2 = 1.

(3) Relock time assumes typical operating conditions, 10°C maximum temperature drift.

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4.3.2 DLLs Characteristics

Table 4-15 summarizes the DLL characteristics and assumes testing over recommended operating conditions.

Table 4-15. DLL Characteristics

NAME	DESCRIPTION	MIN	TYP	MAX	UNIT
vdda_dll0_lpddr21	LPDDR21 power supply providing clocks to bytes 0 and 2		See (2)		V
vdda_dll1_lpddr21	LPDDR21 power supply providing clocks to bytes 1 and 3		See (2)		V
vdda_dll0_lpddr22	LPDDR22 power supply providing clocks to bytes 0 and 2		See (2)		V
vdda_dll1_lpddr22	LPDDR22 power supply providing clocks to bytes 1 and 3		See (2)		V
f_{input}	Input clock frequency(1)	48		400	MHz
t_{lock}	Lock time			400	cycles
t_{relock}	Relock time (a change of the DLL frequency implies that DLL must relock)			400	cycles

(1) Maximum frequency for minimal conditions

(2) The DLL power supplies (vdda_dll0_lpddr21, vdda_dll0_lpddr22, vdda_dll1_lpddr21, vdda_dll1_lpddr22) voltage ranges follow the vdd_core voltage ones. They can be shorted with vdd_core. See the operating condition addendum for values. OPP voltage values may change following the silicon characterization result.

4.3.3 DPLLs and DLLs Noise Isolation

NOTE

For more information on DPLLs and DLLs decoupling capacitors requirements, see Section 3.4.1.3, *Analog Voltage Decoupling.*

4.4 Internal 32-kHz Oscillator

An internal 32-kHz oscillator is implemented in the wake-up domain. Table 4-16 gives the internal 32-kHz oscillator characteristic.

Table 4-16. Internal 32-kHz Oscillator Characteristic

PARAMETER	MIN	TYP	MAX	UNIT
Internal 32-kHz oscillator frequency	16	32	60	kHz

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5 Video DAC Specifications

NOTE

For more information regarding the VideoDAC architecture, see the Display Subsystem / Video Encoder / Video Encoder Functional Description / Video DAC section of the OMAP4430 TRM.

5.1 TVOUT Buffer Mode (DAC + Buffer)

The connection for this TVOUT Buffer Mode (DAC + Buffer) normal mode of operation is shown in Figure 5-1. The default mode of operation is dc coupling. For more information regarding the recommended values of the external components, see Section 5.3, *Electrical Specifications Over Recommended Operating Conditions*.

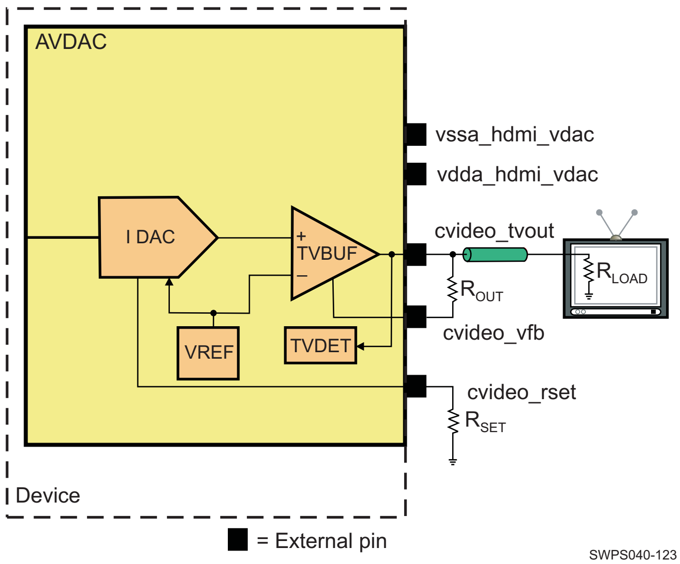

Figure 5-1. Recommended Loading Conditions for TVOUT Buffer Mode

5.2 TVOUT Bypass Mode (DAC Only)

In this case, TVOUT bypass input is high and the TVOUT buffer is bypassed (for more information, see Section 5.4, *TVOUT Bypass Mode Specifications (DAC-Only) Electrical Specifications Over Recommended Operating Conditions*). Figure 5-2 shows the connection. For more information regarding the recommended values of the external components, see Section 5.3, *Electrical Specifications Over Recommended Operating Conditions*.

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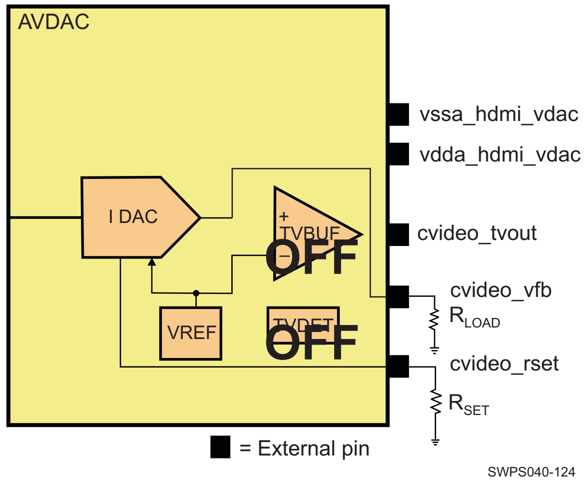

Figure 5-2. Recommended Loading Conditions for TVOUT Bypass Mode

5.3 Electrical Specifications Over Recommended Operating Conditions

- TVOUT dc high swing mode:
  - R_{OUT} = 2.7 kΩ (±1%)
  - R_{SET} = 4.7 kΩ (±1%)
  - R_{LOAD} = 75 Ω (±5%)
  - Z_{CABLE} = 75 Ω (±5%)
- TVOUT ac high swing mode:
  - R_{OUT} = 2.7 kΩ (±1%)
  - R_{SET} = 4.7 kΩ (±1%)
  - R_{LOAD} = 75 Ω (±5%)
  - Z_{CABLE} = 75 Ω (±5%)
  - CAC = 220 µF (±5%)

Table 5-1. DAC—Static Electrical Specifications[8]

PARAMETER		CONDITIONS/ASSUMPTIONS	MIN	TYP	MAX	UNIT
R	Resolution			10		Bits
DC ACCURACY						
INL[1]	Integral nonlinearity (INL)	50 to 111 input code range	–6		6	LSB
	Integral nonlinearity (INL) signal video range	111 to 895 input code range	–4		4	
	Integral nonlinearity (INL) synchronization pulse	783 to 1007 input code range	–5		5	
DNL[2]	Differential nonlinearity	111 to 895 input code range	–2.5		2.5	LSB
ANALOG OUTPUT						
-	Output voltage	0 to 1023 input code range, R_{LOAD} = 75 Ω	1.2	1.3	1.5	V
-	Gain error	-	–10		10	% FS
R_{VOUT}	Output impedance		67.5	75	82.5	Ω
REFERENCE						
V_{REF}	Internal band gap voltage reference			0.55		V
POWER CONSUMPTION						

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Table 5-1. DAC—Static Electrical Specifications[(8)] (continued)

PARAMETER			CONDITIONS/ASSUMPTIONS	MIN	TYP	MAX	UNIT
$I_{vdda\text{-}up}$	Analog supply current[(4)]	DC mode no load	Average current on vdda_hdmi_vdac, no load, 2 channels Input code 50 (maximum output voltage)	4.5	6.5	8.5	mA
		AC mode no load		19	28	37	
		Full load 75-Ω load		19	28	37	
$I_{vdda\text{-}up}$ (peak)	Peak analog supply current		Lasts less than 1 ns		60		mA
$I_{vdd\text{-}up}$	Digital supply current[(5)]		Average current, measured at f_{CLK} = 54 MHz, f_{OUT} = 2 MHz sine wave, vdd = 1.1 V			2	mA
$I_{vdd\text{-}up}$ (peak)	Peak digital supply current[(6)]		Peak current, full-scale transition lasting less than 1 ns		8		mA
$I_{vdda\text{-}down}$[(9)]	Analog supply current, total power down[(9)]		T = 30°C, vdda_hdmi_vdac = 1.8 V, no load			12	μA
$I_{vdda\text{-}stdby}$[(9)]	Analog supply current, standby mode[(9)]		Bandgap and internal LDO are ON, all other analog blocks are OFF, no load, T = 30°C	90	180	270	μA
$I_{vdd\text{-}down(pm)}$[(9)]	Digital supply current, total power down[(9)]		T = 30°C, Full or partial power management			6	μA
$I_{vdd\text{-}down(nopm)}$[(9)]	Digital supply current, total power down (no power management)[(9)]		T = 30°C, VDD = 1.1 V, no power management			60	μA

(1) The INL is measured at the output of the DAC (accessible at an external pin during bypass mode). The INL at code 783 equals 0.

(2) The DNL is measured at the output of the DAC (accessible at an external pin during bypass mode). The INL at code 783 equals 0.

(3) Reference PSR measures the effect of a supply disturbance at cvideo_tvout.

(4) The analog supply current I_{vdda} is directly proportional to the full-scale output current I_{FS} and is insensitive to f_{CLK}.

(5) The digital supply current I_{VDD} is dependent on the digital input waveform, the DAC update rate f_{CLK}, and the digital supply VDD.

(6) The peak digital supply current occurs at full-scale transition for duration less than 1 ns.

(7) See Section 5.5, *Analog Supply (vdda_hdmi_vdac) Noise Requirements*, for actual maximum ripple allowed on vdda_hdmi_vdac.

(8) For more information on code range definition, see Figure 5-3.

(9) For more information on AVDAC power-up, power-down, and standby mode configurations, see Display Subsystem / Video Encoder / Video Encoder Functional Description / Video DAC / Video DAC Power Management section of the OMAP4430 TRM.

Table 5-2. Video DAC—Dynamic Electrical Specifications[(6)]

PARAMETER		CONDITIONS/ASSUMPTIONS		MIN	TYP	MAX	UNIT
f_{CLK}[(1)]	Output update rate	Equal to input clock frequency			54	60	MHz
	Clock jitter	RMS clock jitter required to assure 10-bit accuracy			40	70	ps
	Attenuation at 5.1 MHz	Corner frequency for signal	DC mode			1.5	dB
			AC mode				
BW	Signal bandwidth	3dB	DC mode		6		MHz
			AC mode				
	Differential gain[(2)]	111 to 895 input code range	DC mode	–5%		5%	
			AC mode	–5%		5%	
	Differential phase[(2)]	111 to 895 input code range	DC mode	–3°		3°	
			AC mode	–3°		3°	
SFDR	Within bandwidth 1 kHz to 6 MHz	f_{CLK} = 54 MHz, f_{OUT} = 1 MHz, sine wave input, 111 to 895 input code range	DC mode	40	50	70	dB
			AC mode				
SNR	Within bandwidth 1 kHz to 6 MHz	f_{CLK} = 54 MHz, f_{OUT} = 1 MHz, sine wave input, 256 to 768 input code range	DC mode	50	54	75	dB
			AC mode				
PSR[(4)]	Power supply rejection (up to 6 MHz)	100 mV_{PP} at 6 MHz, input code 895			6[(4)]		dB

Table 5-2. Video DAC—Dynamic Electrical Specifications[6] (continued)

PARAMETER		CONDITIONS/ASSUMPTIONS	MIN	TYP	MAX	UNIT
Crosstalk	Between the two video channels			–50	–40	dB
C_{Load}	TVOUT(cvideo_tvout) stability, TVOUT decoupling capacity	Total decoupling capacity from cvideo_tvout to ground, C_{Load}			300	pF

(1) For internal input clock information, see the Display Subsystem chapter of the OMAP4430 TRM.

(2) The differential gain and phase value is for dc coupling. Note that there is degradation for the ac coupling. The differential gain and phase are measured with respect to the gain and phase of the burst signal (–20 to 20 IRE).

(3) The SNR value is for dc coupling.

(4) PSR measures the effect of a supply disturbance at cvideo_tvout.

(5) The flat band measurement is done at 500 kHz for characterizing the attenuation at 5.1 MHz.

(6) For more information on code range definition, see Figure 5-3.

Figure 5-3 describes the composite video signal levels.

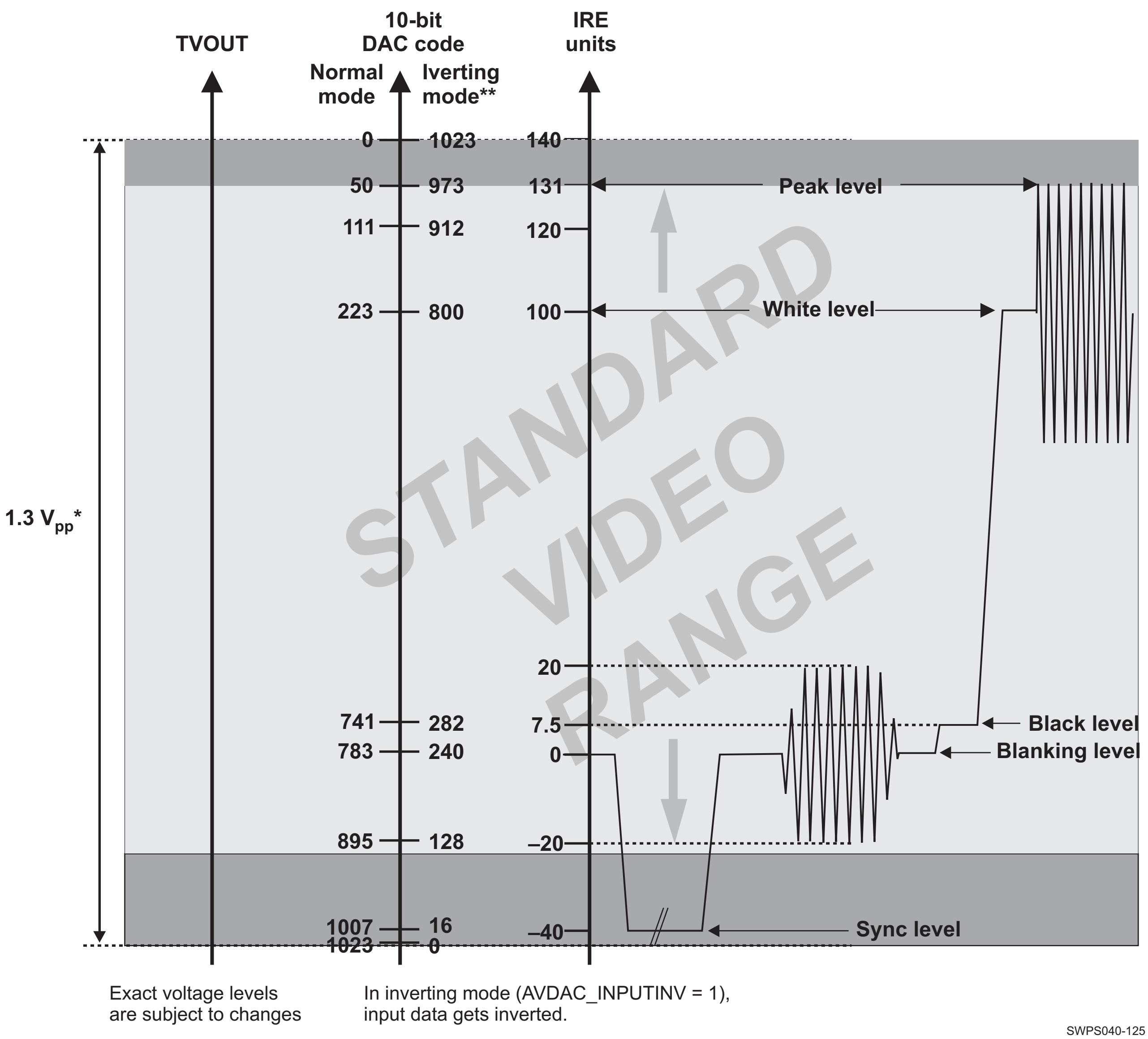

Figure 5-3. Composite Video Signal Levels[1][2]

(1) The 1.3V_{PP} (peak-to-peak) is referring to the output signal at cvideo_tvout in the DAC + Buffer composite-video mode. Note that the 1.3V_{PP} must apply to both cvideo_tvout in DAC + Buffer s-video mode (dual-DAC mode configured for ac or dc coupling). This voltage peak-to-peak value is subject to change.

(2) For more information related to the AVDAC_INPUTINV register configuration, see the Display Subsystem / Video Encoder / Video Encoder Functional Description / Video DAC / Video DAC Normal Mode section of the OMAP4430 TRM. In AVDAC bypass mode (DAC only), higher values of the DAC input code will result in higher output voltage, as the TVOUT buffer path is bypassed.

5.4 TVOUT Bypass Mode Specifications (DAC-Only) Electrical Specifications Over Recommended Operating Conditions

- 1) Bypass Mode
  - R_{LOAD} = 1.5 kΩ (±1%)
  - R_{SET} = 10 kΩ (±1%)

Table 5-3. DAC—Static Electrical Specifications—Bypass Mode[(2)]

PARAMETER		CONDITIONS/ASSUMPTIONS	MIN	TYP	MAX	UNIT
R	Resolution			10		Bits
DC ACCURACY						
INL[(1)]	Integral nonlinearity (INL)	37 to 954 input code range, R_{LOAD} = 1.5 kΩ	–1		1	LSB
DNL[(1)]	Differential nonlinearity	37 to 954 input code range, R_{LOAD} = 1.5 kΩ	–1		1	LSB
ANALOG OUTPUT						
-	Output voltage	R_{LOAD} = 1.5 kΩ	0.60	0.70	0.77	V
-	Output current	R_{LOAD} = 1.5 kΩ	0.60	0.70	0.77	V
-	Gain error	-	–10		10	% FS
POWER CONSUMPTION						
$I_{vdda-up}$	Analog supply current	Average current on vdda_hdmi_vdac, R_{LOAD} = 1.5 kΩ Input code 1023	0.7	1.0	1.4	mA
$I_{vdda-down}$	Analog supply current, total power down	T = 30ºC, vdda_hdmi_vdac = 1.8 V, no load			12	µA
$I_{vdda-stdby}$	Analog supply current, standby mode	Bandgap and internal LDO are ON, all other analog blocks are OFF, no load, T = 30ºC	90	180	270	µA

(1) In bypass mode, output node is cvideo_tvout node. For more information, see Section 5.2, *TVOUT Bypass Mode (DAC Only)*.

(2) For more information on code range definition, see Figure 5-3.

Table 5-4. Video DAC—Dynamic Electrical Specifications—Bypass Mode[(1)]

PARAMETER	CONDITIONS/ASSUMPTIONS		MIN	TYP	MAX	UNIT
f_{CLK}	Output update rate	Equal to input clock frequency		54	60	MHz
	Clock jitter	RMS clock jitter required to assure 10-bit accuracy		40	70	ps
BW	Signal bandwidth	3dB		6		MHz
SFDR	Within bandwidth 1 kHz to 6 MHz	f_{CLK} = 54 MHz, f_{OUT} = 1 MHz, sine wave input, 111 to 895 input code range	40	50	70	dB
SNR	Within bandwidth 1 kHz to 6 MHz	f_{CLK} = 54 MHz, f_{OUT} = 1 MHz, sine wave input, 256 to 768 input code range	50	54	75	dB
PSR	Power supply rejection (up to 6 MHz)	100 mV_{PP} at 6 MHz, input code 895		6		dB

(1) For more information on code range definition, see Figure 5-3.

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5.5 Analog Supply (vdda_hdmi_vdac) Noise Requirements

To assure 10-bit accuracy of the DAC analog output, the analog supply vdda_hdmi_vdac has to meet the noise requirements stated in this section.

The DAC power supply rejection ratio is defined as the relative variation of the full-scale output current divided by the supply variation. Thus, it is expressed in percentage of full-scale range (FSR) per volt of supply variation as shown in the following equation:

$$PSRR_{DAC} = \frac{100 \cdot \dfrac{\Delta I_{OUT}}{I_{OUTFS}}}{V_{AC}} \quad \left[\% \, FSR / V\right]$$

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Depending on frequency, the PSRR is defined in Table 5-5.

Table 5-5. Video DAC—Power Supply Rejection Ratio

SUPPLY NOISE FREQUENCY	PSRR % FSR/V
0 to 100 kHz	1
> 100 kHz	The rejection decreases 20 dB/dec. Example: at 1 MHz the PSRR is 10% of FSR/V

A graphic representation is shown in Figure 5-4.

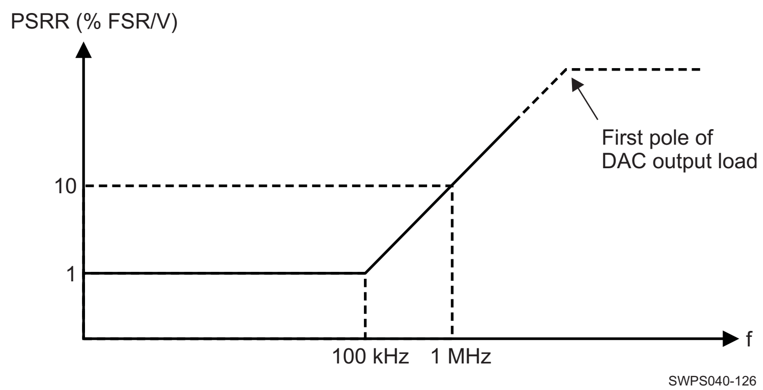

Figure 5-4. Video DAC—Power Supply Rejection Ratio

To ensure that the DAC SFDR specification is met, the PSRR values and the clock jitter requirements translate to the following limits on vdda_hdmi_vdac (for the Video DAC).

The maximum peak-to-peak noise on vdda (ripple) is defined in Table 5-6:

Table 5-6. Video DAC—Maximum Peak-to-Peak Noise on vdda_hdmi_vdac

TONE FREQUENCY	MAXIMUM PEAK-TO-PEAK NOISE on vdda_hdmi_vdac
0 to 100 kHz	< 30 mV_{PP}
> 100 kHz	Decreases 20 dB/dec. Example: at 1 MHz the maximum is 3 mV_{PP}

The maximum noise spectral density (white noise) is defined in Table 5-7:

Table 5-7. Video DAC—Maximum Noise Spectral Density

SUPPLY NOISE BANDWIDTH	MAXIMUM SUPPLY NOISE DENSITY
0 to 100 kHz	< 20 μV / √Hz
> 100 kHz	Decreases 20 dB/dec. Example: at 1 MHz the maximum noise density is 2 μV/ √Hz

Because the DAC PSRR deteriorates at a rate of 20 dB/dec after 100 kHz, it is highly recommended to have vdda_hdmi_vdac low pass filtered (proper decoupling) (see the illustrated application: Section 5.6, *External Component Value Choice*).

5.6 External Component Value Choice

The output current I_{DACOUT} appearing at the output of the 10-bit DAC is a function of both the input code DAC_CODE (ranging from 0 to 1023) and I_{DACMAX} and can be expressed as:

$I_{DACOUT} = I_{REF} * (DAC\_CODE / 120)$ (1)

The maximum output current I_{DACMAX} from the DAC is given by:

$I_{DACMAX} = I_{REF} * 1023 / 120$ (2)

The reference current, I_{REF}, is set by a combination of internal and external resistors in series, R_{REF}, and an internal reference voltage, V_{REF}, and is given by:

$I_{REF} = V_{REF} / R_{REF}$ (3)

Typically, V_{REF} = 0.55 V and R_{REF} = 9.4 kΩ in TVOUT high-swing mode:

$R_{REF} = R_{INTERNAL} + R_{EXTERNAL} = R_{INTERNAL} + R_{SET}$

In TVOUT high-swing mode, $R_{INTERNAL}$ = 4.7 kΩ and R_{SET} = 4.7 kΩ. In bypass mode, $R_{INTERNAL}$ = 0 kΩ and R_{SET} = 10 kΩ

The video signal voltage at cvideo_tvout node can be written as (excluding the offset voltage):

$V_{TVOUT} = 35 * R_{LOAD} * I_{DACMAX} * (1 – DAC\_CODE / 1023)$ (4)

Figure 5-5 shows the cvideo_tvout transfer function. Regarding the typical composite video signal levels versus the DAC input code, For more information on code range definition, see Figure 5-3.

Regarding the typical values for R_{OUT} and R_{SET} resistors, as well for C_{OUT} capacitor, for different modes of the TV display interface, see the Display Subsystem / Video Encoder / Video Encoder Environment section of the OMAP4430 TRM.

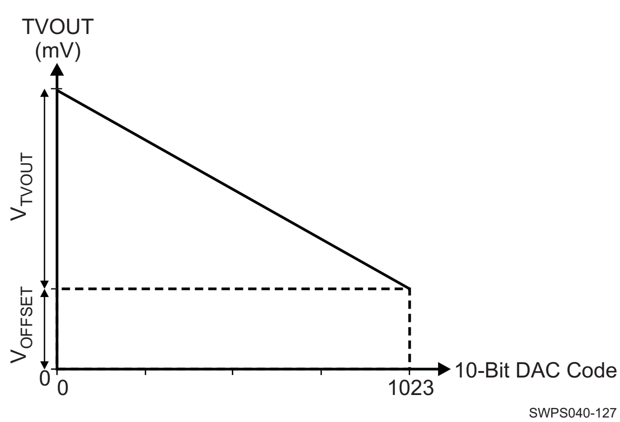

Figure 5-5. cvideo_tvout Transfer Function

NOTE

The dc levels (V_{OFFSET}) will be shifted due to process variations.

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6 Timing Requirements and Switching Characteristics

6.1 Timing Test Conditions

All timing requirements and switching characteristics are valid over the recommended operating conditions unless otherwise specified.

6.2 Interface Clock Specifications

6.2.1 Interface Clock Terminology

The interface clock is used at the system level to sequence the data and/or to control transfers accordingly with the interface protocol.

6.2.2 Interface Clock Frequency

The two interface clock characteristics are:

- The maximum clock frequency
- The maximum operating frequency

The interface clock frequency documented in this document is the maximum clock frequency, which corresponds to the maximum frequency programmable on this output clock. This frequency defines the maximum limit supported by the device IC and doesn't take into account any system consideration (PCB, Peripherals).

The system designer will have to consider these system considerations and the device IC timing characteristics as well to define properly the maximum operating frequency that corresponds to the maximum frequency supported to transfer the data on this interface.

6.2.3 Clock Jitter Specifications

Jitter is a phase noise, which may alter different characteristics of a clock signal. The jitter specified in this document is the time difference between the typical cycle period and the actual cycle period affected by noise sources on the clock. The cycle (or period) jitter terminology will be used to identify this type of jitter.

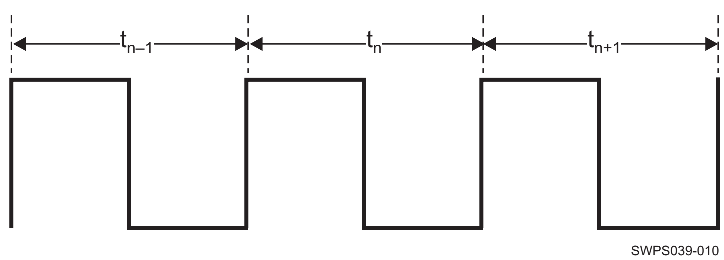

Figure 6-1. Cycle (or Period) Jitter

Jitter values are defined as follows:

- Ideal clock period = t_p
- Maximum Cycle/Period Jitter = Max ($|t_i - t_p|$), with i = n–1, n, n+1, …
- Minimum Cycle/Period Jitter = Min ($|t_i - t_p|$)
- Jitter Standard Deviation (or RMS Jitter) = Standard Deviation ($|t_i - t_p|$)

  Unless otherwise specified, the jitter probability density can be approximated by a Gaussian function and peak-to-peak jitter is defined over a ±7 sigma distribution of this function.

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6.2.4 Clock Duty Cycle Error

The maximum duty cycle error is the difference between the absolute value of the maximum high-level pulse duration or the maximum low-level pulse duration and the typical pulse duration value:

- maximum pulse duration = typical pulse duration + maximum duty cycle error
- minimum pulse duration = typical pulse duration – maximum duty cycle error

In this document, the clock duty cycle can be documented as maximum pulse duration or as maximum duty cycle error. In this case, you can consider:

maximum duty cycle error = maximum [(maximum pulse duration – typical pulse duration) or (typical pulse duration – minimum pulse duration)]

6.3 Timing Parameters

The timing parameter symbols used in the timing requirements and switching characteristics tables are created in accordance with JEDEC Standard 100. To shorten the symbols, some of pin names and other related terminologies have been abbreviated as follows:

Table 6-1. Timing Parameters

SUBSCRIPTS	
Symbol	**Parameter**
c	Cycle time (period)
d	Delay time
dis	Disable time
en	Enable time
h	Hold time
su	Setup time
START	Start bit
t	Transition time
v	Valid time
w	Pulse duration (width)
X	Unknown, changing, or don't care level
F	Fall time
H	High
L	Low
R	Rise time
V	Valid
IV	Invalid
AE	Active Edge
FE	First Edge
LE	Last Edge
Z	High impedance

6.4 External Memory Interface

The OMAP4430 includes the following external memory interfaces:

- General-purpose memory controller (GPMC)
- External memory interface controller (EMIF)

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6.4.1 General-Purpose Memory Controller (GPMC)

NOTE

For more information, see the General-Purpose Memory Controller Overview section of the OMAP4430 TRM.

The GPMC is the OMAP-unified memory controller that interfaces external memory devices such as:

- Asynchronous SRAM-like memories and ASIC devices
- Asynchronous page mode and synchronous burst NOR flash
- NAND flash

6.4.1.1 GPMC/NOR Flash Interface—Synchronous Mode—100 MHz

Table 6-3 and Table 6-4 assume testing over the recommended operating conditions and electrical characteristic conditions below (see Figure 6-2 through Figure 6-5).

Table 6-2. GPMC/NOR Flash Timing Conditions—Synchronous Mode—100 MHz(1)(2)(3)

TIMING CONDITION PARAMETER		VALUE		UNIT
		MIN	MAX	
Input Conditions				
t_R	Input signal rise time	0.32	1.02	ns
t_F	Input signal fall time	0.38	1.07	ns
PCB Conditions				
	Number of external peripherals		1	
	Far end load		10	pF
	Trace length		4	cm
	Characteristics impedance	30	50	Ω

(1) IO settings except gpmc_nwp: LB0 = 1.
For more information, see the Control Module / Control Module Functional Description/ Functional Register Description / Signal Integrity Parameter Control Registers with Pad Group Assignment section of the OMAP4430 TRM.
IO settings for gpmc_nwp: MB[1:0] = 01 and LB0 = 0.
For more information, see the Control Module / Control Module Functional Description/ Functional Register Description / Signal Integrity Parameter Control Registers with Pad Group Assignment / 50-Ω Output Buffer I/Os with Combined Mode and Load Settings section of the OMAP4430 TRM.

(2) In this table the rise and fall times are calculated for 20% to 80% of VDDS. For more information on the corresponding OMAP4 VDDS power supply name, see Table 2-1, POWER [9] column with the ball name.

(3) To have an idea of the output OMAP4 ball load supported for this application, you can consider the following:
Output OMAP4 ball load = Far End load + 1.34 pF/cm typical x trace length (cm).

Table 6-3. GPMC/NOR Flash Timing Requirements—Synchronous Mode—100 MHz(2)

NO.	PARAMETER		OPP100		OPP50		UNIT
			MIN	MAX	MIN	MAX	
F12	$t_{su(dV-clkH)}$	Setup time, input data gpmc_d[15:0] valid before output clock gpmc_clk high	2.2		12		ns
F13	$t_{h(clkH-dV)}$	Hold time, input data gpmc_d[15:0] valid after output clock gpmc_clk high	1.5		1.5		ns
F21	$t_{su(waitV-clkH)}$	Setup time, input wait gpmc_waitx(1) valid before output clock gpmc_clk high	2.2		12		ns
F22	$t_{h(clkH-waitV)}$	Hold time, input wait gpmc_waitx(1) valid after output clock gpmc_clk high	1.5		1.5		ns

(1) In gpmc_waitx, x is equal to 0, 1, 2, or 3.

(2) See DM Operating Condition Addendum for CORE OPP voltages.

Table 6-4. GPMC/NOR Flash Switching Characteristics—Synchronous Mode—100 MHz

NO.	PARAMETER			OPP100		OPP50		UNIT
				MIN	MAX	MIN	MAX	
F0	1 / $t_{c(clk)}$	Frequency[15], output clock gpmc_clk			100		50	MHz
F1	$t_{w(clkH)}$	Typical pulse duration, output clock gpmc_clk high		0.5 P[12]		0.5 P[12]		ns
F1	$t_{w(clkL)}$	Typical pulse duration, output clock gpmc_clk low		0.5 P[12]		0.5 P[12]		ns
	$t_{dc(clk)}$	Duty cycle error, output clk gpmc_clk		–500.00	500.00	–1000.00	1000.00	ps
	$t_{j(clk)}$	Jitter standard deviation[16], output clock gpmc_clk			64.7		64.7	ps
	$t_{R(clk)}$	Rise time, output clock gpmc_clk		0.230	1.430	0.230	1.430	ns
	$t_{F(clk)}$	Fall time, output clock gpmc_clk		0.227	1.550	0.227	1.550	ns
	$t_{R(DO)}$	Rise time, output data gpmc_d[15:0]		0.230	1.430	0.230	1.430	ns
	$t_{F(DO)}$	Fall time, output data gpmc_d[15:0]		0.227	1.550	0.227	1.550	ns
F2	$t_{d(clkH-nCSV)}$	Delay time, gpmc_clk rising edge to gpmc_ncsx[11] transition		F[6] – 1.9	F[6] + 3.1	F[6] – 5.1	F[6] + 8.1	ns
F3	$t_{d(clkH-nCSIV)}$	Delay time, gpmc_clk rising edge to gpmc_ncsx[11] invalid		E[5] – 1.9	E[5] + 3.1	E[5] – 5.1	E[5] + 8.1	ns
F4	$t_{d(ADDV-clk)}$	Delay time, gpmc_a[26:17] / gpmc_a[16:1] /gpmc_a[10:1] address bus valid to gpmc_clk first edge		B[2] – 3.1	B[2] + 2.1	B[2] – 8.1	B[2] + 5.1	ns
F5	$t_{d(clkH-ADDIV)}$	Delay time, gpmc_clk rising edge to gpmc_a[16:1] gpmc address bus invalid		–2.1		–5.1		ns
F8	$t_{d(clkH-nADV)}$	Delay time, gpmc_clk rising edge to gpmc_nadv_ale transition		G[7] – 1.9	G[7] + 3.1	G[7] – 5.1	G[7] + 8.1	ns
F9	$t_{d(clkH-nADVIV)}$	Delay time, gpmc_clk rising edge to gpmc_nadv_ale invalid		D[4] – 1.9	D[4] + 3.1	D[4] – 5.1	D[4] + 8.1	ns
F10	$t_{d(clkH-nOE)}$	Delay time, gpmc_clk rising edge to gpmc_noe transition		H[8] – 2.1	H[8] + 2.1	H[8] – 5.1	H[8] + 4.1	ns
F11	$t_{d(clkH-nOEIV)}$	Delay time, gpcm rising edge to gpmc_noe invalid		E[5] – 2.1	E[5] + 2.1	E[5] – 5.1	E[5] + 4.1	ns
F18	$t_{w(nCSV)}$	Pulse duration, gpmc_ncsi[11] low	Read	A[1]		A[1]		ns
			Write	A[1]		A[1]		ns
F19	$t_{w(nBEV)}$	Pulse duration, gpmc_nbe0_cle, gpmc_nbe1 low	Read	C[3]		C[3]		ns
			Write	C[3]		C[3]		ns
F20	$t_{w(nADVV)}$	Pulse duration, gpmc_nadv_ale low	Read	K[13]		K[13]		ns
			Write	K[13]		K[13]		ns
F23	$t_{d(clkH-IODIR)}$	Delay time, gpmc_clk rising edge to gpmc_io_dir high (IN direction)		H[8] – 2.1	H[8] + 2.1	H[8] – 5.1	H[8] + 4.1	ns
F24	$t_{d(clkH-IODIRIV)}$	Delay time, gpmc_clk rising edge to gpmc_io_dir low (OUT direction)		M[17] – 2.1	M[17] + 2.1	M[17] – 5.1	M[17] + 4.1	ns

(1) For single read: A = (CSRdOffTime – CSOnTime) * (TimeParaGranularity + 1) * GPMC_FCLK period
For burst read: A = (CSRdOffTime – CSOnTime + (n – 1) * PageBurstAccessTime) * (TimeParaGranularity + 1) * GPMC_FCLK period with n the page burst access number.
For burst write: A = (CSWrOffTime – CSOnTime + (n – 1) * PageBurstAccessTime) * (TimeParaGranularity + 1) * GPMC_FCLK period with n the page burst access number.

(2) B = ClkActivationTime * GPMC_FCLK

(3) For single read: C = RdCycleTime * (TimeParaGranularity + 1) * GPMC_FCLK
For burst read: C = (RdCycleTime + (n – 1) * PageBurstAccessTime) * (TimeParaGranularity + 1) * GPMC_FCLK with n the page burst access number.
For Burst write: C = (WrCycleTime + (n – 1) * PageBurstAccessTime) * (TimeParaGranularity + 1) * GPMC_FCLK with n the page burst

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access number.

(4) For single read: D = (RdCycleTime – AccessTime) * (TimeParaGranularity + 1) * GPMC_FCLK
For burst read: D = (RdCycleTime – AccessTime) * (TimeParaGranularity + 1) * GPMC_FCLK
For burst write: D = (WrCycleTime – AccessTime) * (TimeParaGranularity + 1) * GPMC_FCLK

(5) For single read: E = (CSRdOffTime – AccessTime) * (TimeParaGranularity + 1) * GPMC_FCLK
For burst read: E = (CSRdOffTime – AccessTime) * (TimeParaGranularity + 1) * GPMC_FCLK
For burst write: E = (CSWrOffTime – AccessTime) * (TimeParaGranularity + 1) * GPMC_FCLK

(6) For nCS falling edge (CS activated):
Case GpmcFCLKDivider = 0:
- F = 0.5 * CSExtraDelay * GPMC_FCLK

Case GpmcFCLKDivider = 1:
- F = 0.5 * CSExtraDelay * GPMC_FCLK if (ClkActivationTime and CSOnTime are odd) or (ClkActivationTime and CSOnTime are even)
- F = (1 + 0.5 * CSExtraDelay) * GPMC_FCLK otherwise

Case GpmcFCLKDivider = 2:
- F = 0.5 * CSExtraDelay * GPMC_FCLK if ((CSOnTime – ClkActivationTime) is a multiple of 3)
- F = (1 + 0.5 * CSExtraDelay) * GPMC_FCLK if ((CSOnTime – ClkActivationTime – 1) is a multiple of 3)
- F = (2 + 0.5 * CSExtraDelay) * GPMC_FCLK if ((CSOnTime – ClkActivationTime – 2) is a multiple of 3)

(7) For ADV falling edge (ADV activated):
Case GpmcFCLKDivider = 0:
- G = 0.5 * ADVExtraDelay * GPMC_FCLK

Case GpmcFCLKDivider = 1:
- G = 0.5 * ADVExtraDelay * GPMC_FCLK if (ClkActivationTime and ADVOnTime are odd) or (ClkActivationTime and ADVOnTime are even)
- G = (1 + 0.5 * ADVExtraDelay) * GPMC_FCLK otherwise

Case GpmcFCLKDivider = 2:
- G = 0.5 * ADVExtraDelay * GPMC_FCLK if ((ADVOnTime – ClkActivationTime) is a multiple of 3)
- G = (1 + 0.5 * ADVExtraDelay) * GPMC_FCLK if ((ADVOnTime – ClkActivationTime – 1) is a multiple of 3)
- G = (2 + 0.5 * ADVExtraDelay) * GPMC_FCLK if ((ADVOnTime – ClkActivationTime – 2) is a multiple of 3)

For ADV rising edge (ADV deactivated) in Reading mode:
Case GpmcFCLKDivider = 0:
- G = 0.5 * ADVExtraDelay * GPMC_FCLK

Case GpmcFCLKDivider = 1:
- G = 0.5 * ADVExtraDelay * GPMC_FCLK if (ClkActivationTime and ADVRdOffTime are odd) or (ClkActivationTime and ADVRdOffTime are even)
- G = (1 + 0.5 * ADVExtraDelay) * GPMC_FCLK otherwise

Case GpmcFCLKDivider = 2:
- G = 0.5 * ADVExtraDelay * GPMC_FCLK if ((ADVRdOffTime – ClkActivationTime) is a multiple of 3)
- G = (1 + 0.5 * ADVExtraDelay) * GPMC_FCLK if ((ADVRdOffTime – ClkActivationTime – 1) is a multiple of 3)
- G = (2 + 0.5 * ADVExtraDelay) * GPMC_FCLK if ((ADVRdOffTime – ClkActivationTime – 2) is a multiple of 3)

For ADV rising edge (ADV deactivated) in Writing mode:
Case GpmcFCLKDivider = 0:
- G = 0.5 * ADVExtraDelay * GPMC_FCLK

Case GpmcFCLKDivider = 1:
- G = 0.5 * ADVExtraDelay * GPMC_FCLK if (ClkActivationTime and ADVWrOffTime are odd) or (ClkActivationTime and ADVWrOffTime are even)
- G = (1 + 0.5 * ADVExtraDelay) * GPMC_FCLK otherwise

Case GpmcFCLKDivider = 2:
- G = 0.5 * ADVExtraDelay * GPMC_FCLK if ((ADVWrOffTime – ClkActivationTime) is a multiple of 3)
- G = (1 + 0.5 * ADVExtraDelay) * GPMC_FCLK if ((ADVWrOffTime – ClkActivationTime – 1) is a multiple of 3)
- G = (2 + 0.5 * ADVExtraDelay) * GPMC_FCLK if ((ADVWrOffTime – ClkActivationTime – 2) is a multiple of 3)

(8) For OE falling edge (OE activated) / IO DIR rising edge (IN direction):
Case GpmcFCLKDivider = 0:
- H = 0.5 * OEExtraDelay * GPMC_FCLK

Case GpmcFCLKDivider = 1:
- H = 0.5 * OEExtraDelay * GPMC_FCLK if (ClkActivationTime and OEOnTime are odd) or (ClkActivationTime and OEOnTime are even)
- H = (1 + 0.5 * OEExtraDelay) * GPMC_FCLK otherwise

Case GpmcFCLKDivider = 2:

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- H = 0.5 * OEExtraDelay * GPMC_FCLK if ((OEOnTime – ClkActivationTime) is a multiple of 3)
- H = (1 + 0.5 * OEExtraDelay) * GPMC_FCLK if ((OEOnTime – ClkActivationTime – 1) is a multiple of 3)
- H = (2 + 0.5 * OEExtraDelay) * GPMC_FCLK if ((OEOnTime – ClkActivationTime – 2) is a multiple of 3)

For OE rising edge (OE deactivated):
Case GpmcFCLKDivider = 0:
- H = 0.5 * OEExtraDelay * GPMC_FCLK

Case GpmcFCLKDivider = 1:
- H = 0.5 * OEExtraDelay * GPMC_FCLK if (ClkActivationTime and OEOffTime are odd) or (ClkActivationTime and OEOffTime are even)
- H = (1 + 0.5 * OEExtraDelay) * GPMC_FCLK otherwise

Case GpmcFCLKDivider = 2:
- H = 0.5 * OEExtraDelay * GPMC_FCLK if ((OEOffTime – ClkActivationTime) is a multiple of 3)
- H = (1 + 0.5 * OEExtraDelay) * GPMC_FCLK if ((OEOffTime – ClkActivationTime – 1) is a multiple of 3)
- H = (2 + 0.5 * OEExtraDelay) * GPMC_FCLK if ((OEOffTime – ClkActivationTime – 2) is a multiple of 3)

(9) For WE falling edge (WE activated):
Case GpmcFCLKDivider = 0:
- I = 0.5 * WEExtraDelay * GPMC_FCLK

Case GpmcFCLKDivider = 1:
- I = 0.5 * WEExtraDelay * GPMC_FCLK if (ClkActivationTime and WEOnTime are odd) or (ClkActivationTime and WEOnTime are even)
- I = (1 + 0.5 * WEExtraDelay) * GPMC_FCLK otherwise

Case GpmcFCLKDivider = 2:
- I = 0.5 * WEExtraDelay * GPMC_FCLK if ((WEOnTime – ClkActivationTime) is a multiple of 3)
- I = (1 + 0.5 * WEExtraDelay) * GPMC_FCLK if ((WEOnTime – ClkActivationTime – 1) is a multiple of 3)
- I = (2 + 0.5 * WEExtraDelay) * GPMC_FCLK if ((WEOnTime – ClkActivationTime – 2) is a multiple of 3)

For WE rising edge (WE deactivated):
Case GpmcFCLKDivider = 0:
- I = 0.5 * WEExtraDelay * GPMC_FCLK

Case GpmcFCLKDivider = 1:
- I = 0.5 * WEExtraDelay * GPMC_FCLK if (ClkActivationTime and WEOffTime are odd) or (ClkActivationTime and WEOffTime are even)
- I = (1 + 0.5 * WEExtraDelay) * GPMC_FCLK otherwise

Case GpmcFCLKDivider = 2:
- I = 0.5 * WEExtraDelay * GPMC_FCLK if ((WEOffTime – ClkActivationTime) is a multiple of 3)
- I = (1 + 0.5 * WEExtraDelay) * GPMC_FCLK if ((WEOffTime – ClkActivationTime – 1) is a multiple of 3)
- I = (2 + 0.5 * WEExtraDelay) * GPMC_FCLK if ((WEOffTime – ClkActivationTime – 2) is a multiple of 3)

(10) J = GPMC_FCLK period

(11) In gpmc_ncsx, x is equal to 0, 1, 2, 3, 4, 5, 6, or 7.
In gpmc_waitx, x is equal to 0, 1, 2, or 3

(12) P = gpmc_clk period

(13) For read: K = (ADVRdOffTime – ADVOnTime) * (TimeParaGranularity + 1) * GPMC_FCLK
For write: K = (ADVWrOffTime – ADVOnTime) * (TimeParaGranularity + 1) * GPMC_FCLK

(14) GPMC_FCLK is general-purpose memory controller internal functional clock

(15) Related to the gpmc_clk output clock maximum and minimum frequency programmable in I/F module by setting the GPMC_CONFIG1_CSx configuration register bit fields GpmcFCLKDivider.

(16) The jitter probability density can be approximated by a Gaussian function

(17) M = (RdCycleTime – AccessTime) * (TimeParaGranularity + 1) * GPMC_FCLK
Above M parameter expression is given as one example of GPMC programming. IO DIR signal will go from IN to OUT after both RdCycleTime and BusTurnAround completion. Behaviour of IO direction signal does depend on kind of successive read/write accesses performed to memory and multiplexed or nonmultiplexed memory addressing scheme, bus keeping feature enabled or not. IO DIR behaviour is automactically handled by GPMC controller.

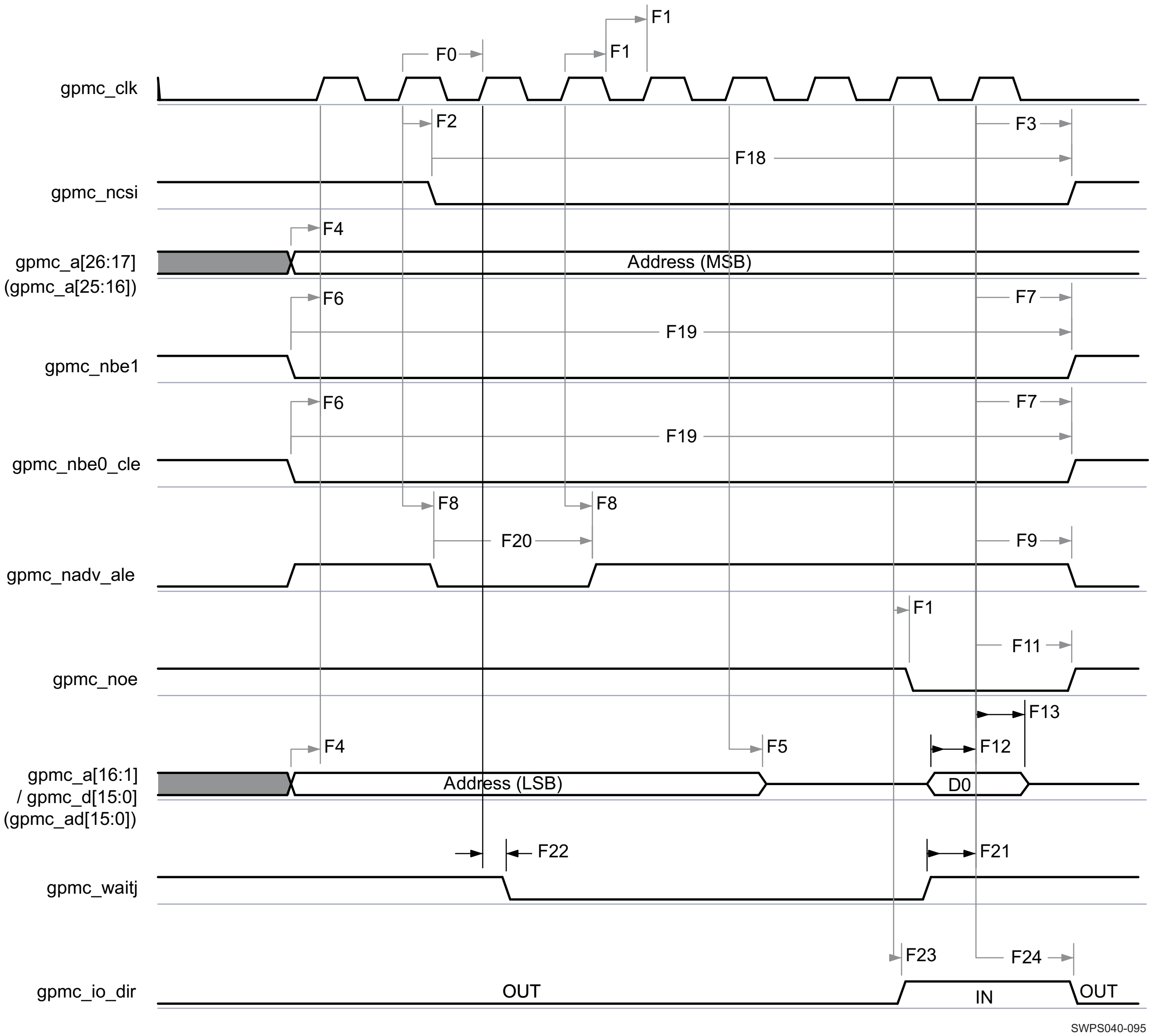

Figure 6-2. GPMC / Multiplexed 16-bit NOR Flash—Synchronous Single Read(1)(2)

(1) In gpmc_ncsi, i is equal to 0, 1, 2, 3, 4, 5, 6, or 7.

(2) In gpmc_waitj, x is equal to 0, 1, 2, or 3.

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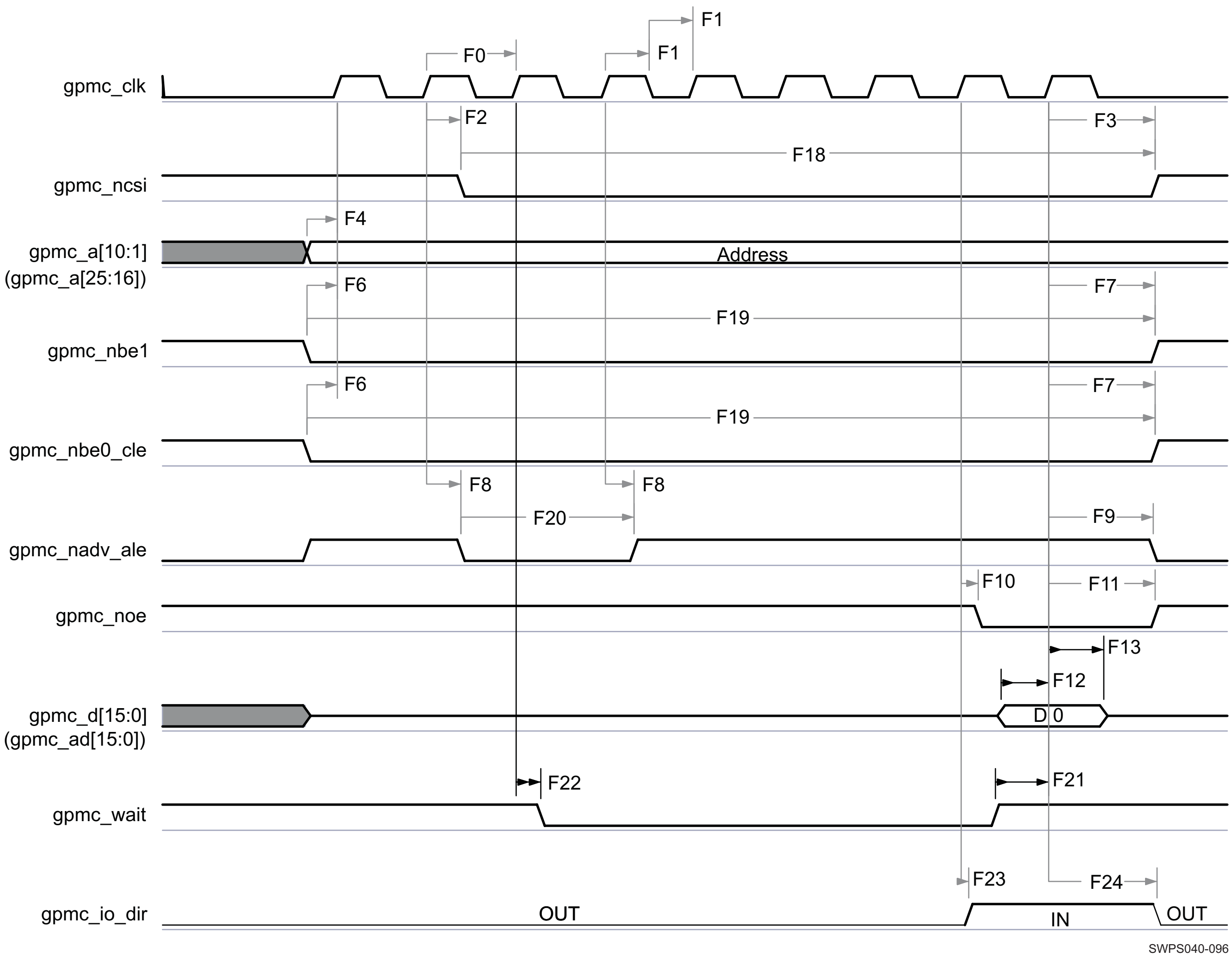

Figure 6-3. GPMC / Nonmultiplexed 16-bit NOR Flash—Synchronous Single Read(1)(2)(3)

(1) In gpmc_ncsi, i is equal to 0, 1, 2, 3, 4, 5, 6, or 7.

(2) In gpmc_waitj, j is equal to 0, 1, 2, or 3.

(3) Nonmultiplexed NOR interface can be used only with a limited address range corresponding to 10 address bits.

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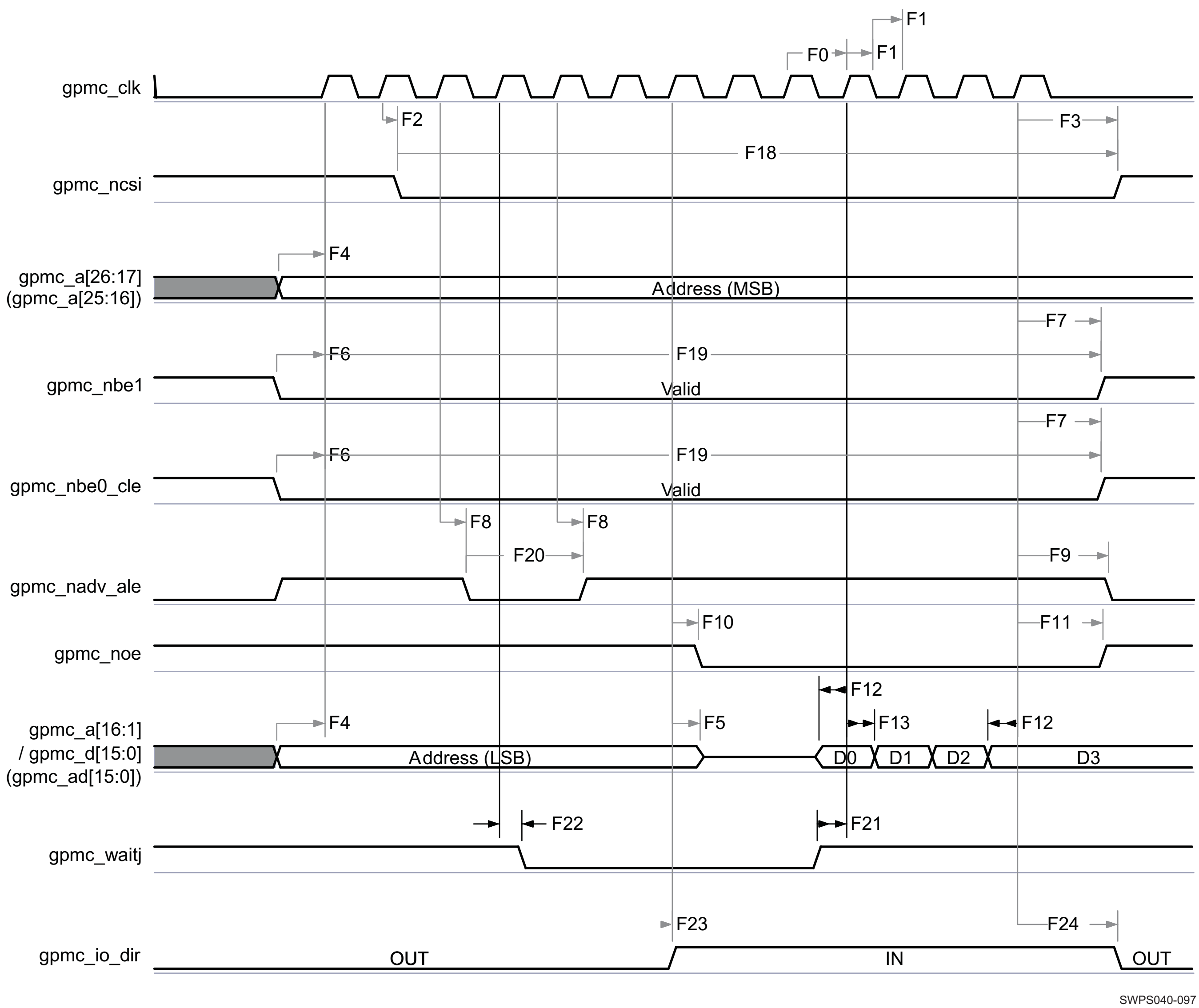

Figure 6-4. GPMC / Multiplexed 16-bit NOR Flash—Synchronous Burst Read 4x16 Bits(1)(2)

(1) In gpmc_ncsi, i is equal to 0, 1, 2, 3, 4, 5, 6, or 7.

(2) In gpmc_waitj, j is equal to 0, 1, 2, or 3.

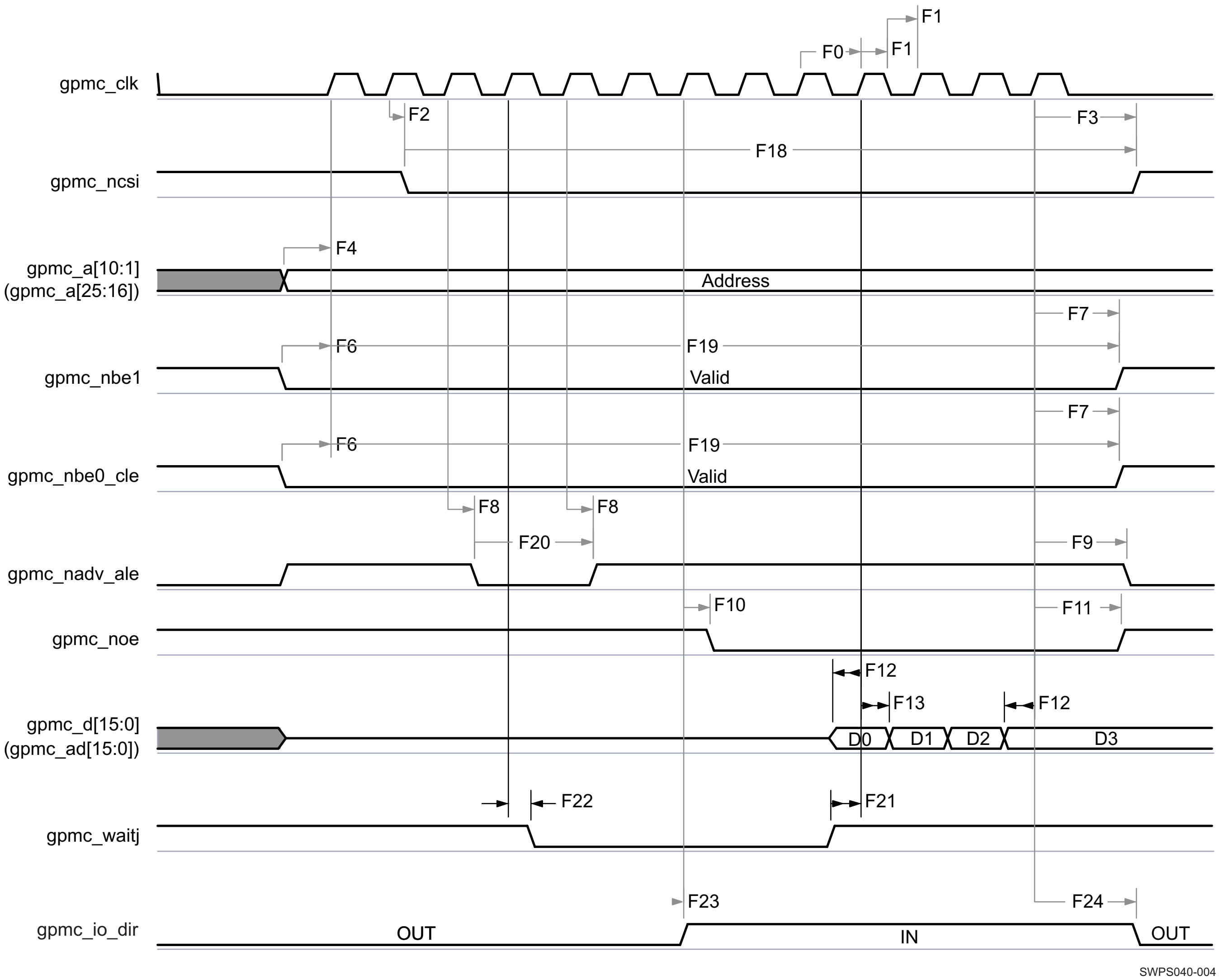

Figure 6-5. GPMC / Nonmultiplexed 16-bit NOR Flash—Synchronous Burst Read 4x16 Bits(1)(2)(3)

(1) In gpmc_ncsi, i is equal to 0, 1, 2, 3, 4, 5, 6, or 7.

(2) In gpmc_waitj, j is equal to 0, 1, 2, or 3.

(3) Nonmultiplexed NOR interface can be used only with a limited address range corresponding to 10 address bits.

6.4.1.2 GPMC/NOR Flash Interface—Synchronous Mode—66 MHz

Table 6-6 and Table 6-7 assume testing over the recommended operating conditions and electrical characteristic conditions below (see Figure 6-6 through Figure 6-11).

Table 6-5. GPMC/NOR Flash Timing Conditions—Synchronous Mode—66 MHz(1)(2)(3)

TIMING CONDITION PARAMETER		VALUE MIN	VALUE MAX	UNIT
Input Conditions				
t_R	Input signal rise time	1.38	2.79	ns
t_F	Input signal fall time	1.14	2.85	ns
PCB Conditions				
	Number of external peripherals		4	
	Far end load		15	pF

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Table 6-5. GPMC/NOR Flash Timing Conditions—Synchronous Mode—66 MHz[(1)(2)(3)] (continued)

TIMING CONDITION PARAMETER		VALUE		UNIT
		MIN	MAX	
	Trace length		5	cm
	Characteristics impedance	40	55	Ω

(1) IO settings except gpmc_nwp: LB0 = 1.
For more information, see the Control Module / Control Module Functional Description/ Functional Register Description / Signal Integrity Parameter Control Registers with Pad Group Assignment section of the OMAP4430 TRM.
IO settings for gpmc_nwp: MB[1:0] = 01 and LB0 = 0.
For more information, see the Control Module / Control Module Functional Description/ Functional Register Description / Signal Integrity Parameter Control Registers with Pad Group Assignment / 50-Ω Output Buffer I/Os with Combined Mode and Load Settings section of the OMAP4430 TRM.

(2) In this table the rise and fall times are calculated for 20% to 80% of VDDS. For more information on the corresponding OMAP4 VDDS power supply name, see Table 2-1, POWER [9] column with the ball name.

(3) To have an idea of the output OMAP4 ball load supported for this application, you can consider the following:
Output OMAP4 ball load = Far End load + 1.34 pF/cm typical x trace length (cm).

Table 6-6. GPMC/NOR Flash Timing Requirements—Synchronous Mode—66 MHz[(2)]

NO.	PARAMETER		OPP100		OPP50		UNIT
			MIN	MAX	MIN	MAX	
F12	$t_{su(dV-clkH)}$	Setup time, input data gpmc_d[15:0] valid before output clock gpmc_clk high	3		17.8		ns
F13	$t_{h(clkH-dV)}$	Hold time, input data gpmc_d[15:0] valid after output clock gpmc_clk high	2.4		2.4		ns
F21	$t_{su(waitV-clkH)}$	Setup time, input wait gpmc_waitx[(1)] valid before output clock gpmc_clk high	3		17.8		ns
F22	$t_{h(clkH-waitV)}$	Hold time, input wait gpmc_waitx[(1)] valid after output clock gpmc_clk high	2.4		2.4		ns

(1) In gpmc_waitx, x is equal to 0, 1, 2 or 3.

(2) See DM Operating Condition Addendum for CORE OPP voltages.

Table 6-7. GPMC/NOR Flash Switching Characteristics—Synchronous Mode—66 MHz

NO.	PARAMETER		OPP100		OPP50		UNIT
			MIN	MAX	MIN	MAX	
F0	$1 / t_{c(clk)}$	Frequency[(15)], output clock gpmc_clk period		66		33	MHz
F1	$t_{w(clkH)}$	Typical pulse duration, output clock gpmc_clk high	0.5 P[(12)]	0.5 P[(12)]	0.5 P[(12)]	0.5 P[(12)]	ns
F1	$t_{w(clkL)}$	Typical pulse duration, output clock gpmc_clk low	0.5 P[(12)]	0.5 P[(12)]	0.5 P[(12)]	0.5 P[(12)]	ns
	$t_{dc(clk)}$	Duty cycle error, output clk gpmc_clk	–758.00	758.00	–1515.00	1515.00	ps
	$t_{j(clk)}$	Jitter standard deviation[(16)], output clock gpmc_clk		64.7		64.7	ps
	$t_{R(clk)}$	Rise time, output clock gpmc_clk	0.9	1.8	0.9	1.8	ns
	$t_{F(clk)}$	Fall time, output clock gpmc_clk	0.9	1.6	0.9	1.6	ns
	$t_{R(DO)}$	Rise time, output data	0.9	1.8	0.9	1.8	ns
	$t_{F(DO)}$	Fall time, output data	0.9	1.6	0.9	1.6	ns
F2	$t_{d(clkH-nCSV)}$	Delay time, gpmc_clk rising edge to gpmc_ncsx[(11)] transition	F[(6)] – 2.1	F[(6)] + 3.1	F[(6)] – 5.1	F[(6)] + 8.1	ns
F3	$t_{d(clkH-nCSIV)}$	Delay time, gpmc_clk rising edge to gpmc_ncsx[(11)] invalid	E[(5)] – 2.1	E[(5)] + 3.1	E[(5)] – 5.1	E[(5)] + 8.1	ns
F4	$t_{d(ADDV-clk)}$	Delay time, gpmc_a[26:17] / gpmc_a[16:1] / gpmc_a[10:1] address bus valid to gpmc_clk first edge	B[(2)] – 3.1	B[(2)] + 2.1	B[(2)] – 8.1	B[(2)] + 5.1	ns

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Table 6-7. GPMC/NOR Flash Switching Characteristics—Synchronous Mode—66 MHz (continued)

NO.	PARAMETER			OPP100		OPP50		UNIT
				MIN	MAX	MIN	MAX	
F5	$t_{d(clkH\text{-}ADDIV)}$	Delay time, gpmc_clk rising edge to gpmc_a[26:17] / gpmc_a[16:1] gpmc address bus invalid		–2.1		–5.1		ns
F6	$t_{d(nBEV\text{-}clk)}$	Delay time, gpmc_nbe0_cle, gpmc_nbe1 valid to gpmc_clk first edge		B(2) – 0.9	B(2) + 3.9	B(2) – 7.4	B(2) + 10.4	ns
F7	$t_{d(clkH\text{-}nBEIV)}$	Delay time, gpmc_clk rising edge to gpmc_nbe0_cle, gpmc_nbe1 invalid		D(4) – 3.9	D(4) + 0.9	D(4) – 10.4	D(4) + 7.4	ns
F8	$t_{d(clkH\text{-}nADV)}$	Delay time, gpmc_clk rising edge to gpmc_nadv_ale transition		G(7) – 1.9	G(7) + 3.1	G(7) – 4.9	G(7) + 8.1	ns
F9	$t_{d(clkH\text{-}nADVIV)}$	Delay time, gpmc_clk rising edge to gpmc_nadv_ale invalid		D(4) – 1.9	D(4) + 3.1	D(4) – 4.9	D(4) + 8.1	ns
F10	$t_{d(clkH\text{-}nOE)}$	Delay time, gpmc_clk rising edge to gpmc_noe transition		H(8) – 2.1	H(8) + 2.1	H(8) – 5.1	H(8) + 4.1	ns
F11	$t_{d(clkH\text{-}nOEIV)}$	Delay time, gpcm rising edge to gpmc_noe invalid		E(5) – 2.1	E(5) + 2.1	E(5) – 5.1	E(5) + 4.1	ns
F14	$t_{d(clkH\text{-}nWE)}$	Delay time, gpmc_clk rising edge to gpmc_nwe transition		I(9) – 1.9	I(9) + 3.1	I(9) – 4.9	I(9) + 8.1	ns
F15	$t_{d(clkH\text{-}Data)}$	Delay time, gpmc_clk rising edge to gpmc_a[26:17] / gpmc_a[16:1] data bus transition		J(10) – 3.9	J(10) + 0.9	J(10) – 10.4	J(10) + 7.4	ns
F17	$t_{d(clkH\text{-}nBE)}$	Delay time, gpmc_clk rising edge to gpmc_nbe0_cle, gpmc_nbe1 transition		J(10) – 3.9	J(10) + 0.9	J(10) – 10.4	J(10) + 7.4	ns
F18	$t_{w(nCSV)}$	Pulse duration, gpmc_ncsi(11) low	Read	A(1)		A(1)		ns
			Write	A(1)		A(1)		ns
F19	$t_{w(nBEV)}$	Pulse duration, gpmc_nbe0_cle, gpmc_nbe1 low	Read	C(3)		C(3)		ns
			Write	C(3)		C(3)		ns
F20	$t_{w(nADVV)}$	Pulse duration, gpmc_nadv_ale low	Read	K(13)		K(13)		ns
			Write	K(13)		K(13)		ns
F23	$t_{d(clkH\text{-}IODIR)}$	Delay time, gpmc_clk rising edge to gpmc_io_dir high (IN direction)		H(8) – 2.1	H(8) + 2.1	H(8) – 5.1	H(8) + 4.1	ns
F24	$t_{d(clkH\text{-}IODIRIV)}$	Delay time, gpcm rising edge to gpmc_io_dir low (OUT direction)		M(17) – 2.1	M(17) + 2.1	M(17) – 5.1	M(17) + 4.1	ns

(1) For single read:
- A = (CSRdOffTime – CSOnTime) * (TimeParaGranularity + 1) * GPMC_FCLK period

For burst read:
- A = (CSRdOffTime – CSOnTime + (n – 1) * PageBurstAccessTime) * (TimeParaGranularity + 1) * GPMC_FCLK period with n the page burst access number.

For burst write:
- A = (CSWrOffTime – CSOnTime + (n – 1) * PageBurstAccessTime) * (TimeParaGranularity + 1) * GPMC_FCLK period with n the page burst access number.

(2) B = ClkActivationTime * GPMC_FCLK

(3) For single read:
- C = RdCycleTime * (TimeParaGranularity + 1) * GPMC_FCLK

For burst read:
- C = (RdCycleTime + (n – 1) * PageBurstAccessTime) * (TimeParaGranularity + 1) * GPMC_FCLK with n the page burst access number.

For burst write:
- C = (WrCycleTime + (n – 1) * PageBurstAccessTime) * (TimeParaGranularity + 1) * GPMC_FCLK with n the page burst access number.

(4) For single read:
- D = (RdCycleTime – AccessTime) * (TimeParaGranularity + 1) * GPMC_FCLK

For burst read:

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- D = (RdCycleTime – AccessTime) * (TimeParaGranularity + 1) * GPMC_FCLK

For burst write:
- D = (WrCycleTime – AccessTime) * (TimeParaGranularity + 1) * GPMC_FCLK

(5) For single read:
- E = (CSRdOffTime – AccessTime) * (TimeParaGranularity + 1) * GPMC_FCLK

For burst read:
- E = (CSRdOffTime – AccessTime) * (TimeParaGranularity + 1) * GPMC_FCLK

For burst write:
- E = (CSWrOffTime – AccessTime) * (TimeParaGranularity + 1) * GPMC_FCLK

(6) For nCS falling edge (CS activated):
Case GpmcFCLKDivider = 0:
- F = 0.5 * CSExtraDelay * GPMC_FCLK

Case GpmcFCLKDivider = 1:
- F = 0.5 * CSExtraDelay * GPMC_FCLK if (ClkActivationTime and CSOnTime are odd) or (ClkActivationTime and CSOnTime are even)
- F = (1 + 0.5 * CSExtraDelay) * GPMC_FCLK otherwise

Case GpmcFCLKDivider = 2:
- F = 0.5 * CSExtraDelay * GPMC_FCLK if ((CSOnTime – ClkActivationTime) is a multiple of 3)
- F = (1 + 0.5 * CSExtraDelay) * GPMC_FCLK if ((CSOnTime – ClkActivationTime – 1) is a multiple of 3)
- F = (2 + 0.5 * CSExtraDelay) * GPMC_FCLK if ((CSOnTime – ClkActivationTime – 2) is a multiple of 3)

(7) For ADV falling edge (ADV activated):
Case GpmcFCLKDivider = 0:
- G = 0.5 * ADVExtraDelay * GPMC_FCLK

Case GpmcFCLKDivider = 1:
- G = 0.5 * ADVExtraDelay * GPMC_FCLK if (ClkActivationTime and ADVOnTime are odd) or (ClkActivationTime and ADVOnTime are even)
- G = (1 + 0.5 * ADVExtraDelay) * GPMC_FCLK otherwise

Case GpmcFCLKDivider = 2:
- G = 0.5 * ADVExtraDelay * GPMC_FCLK if ((ADVOnTime – ClkActivationTime) is a multiple of 3)
- G = (1 + 0.5 * ADVExtraDelay) * GPMC_FCLK if ((ADVOnTime – ClkActivationTime – 1) is a multiple of 3)
- G = (2 + 0.5 * ADVExtraDelay) * GPMC_FCLK if ((ADVOnTime – ClkActivationTime – 2) is a multiple of 3)

For ADV rising edge (ADV deactivated) in Reading mode:
Case GpmcFCLKDivider = 0:
- G = 0.5 * ADVExtraDelay * GPMC_FCLK

Case GpmcFCLKDivider = 1:
- G = 0.5 * ADVExtraDelay * GPMC_FCLK if (ClkActivationTime and ADVRdOffTime are odd) or (ClkActivationTime and ADVRdOffTime are even)
- G = (1 + 0.5 * ADVExtraDelay) * GPMC_FCLK otherwise

Case GpmcFCLKDivider = 2:
- G = 0.5 * ADVExtraDelay * GPMC_FCLK if ((ADVRdOffTime – ClkActivationTime) is a multiple of 3)
- G = (1 + 0.5 * ADVExtraDelay) * GPMC_FCLK if ((ADVRdOffTime – ClkActivationTime – 1) is a multiple of 3)
- G = (2 + 0.5 * ADVExtraDelay) * GPMC_FCLK if ((ADVRdOffTime – ClkActivationTime – 2) is a multiple of 3)

For ADV rising edge (ADV deactivated) in Writing mode:
Case GpmcFCLKDivider = 0:
- G = 0.5 * ADVExtraDelay * GPMC_FCLK

Case GpmcFCLKDivider = 1:
- G = 0.5 * ADVExtraDelay * GPMC_FCLK if (ClkActivationTime and ADVWrOffTime are odd) or (ClkActivationTime and ADVWrOffTime are even)
- G = (1 + 0.5 * ADVExtraDelay) * GPMC_FCLK otherwise

Case GpmcFCLKDivider = 2:
- G = 0.5 * ADVExtraDelay * GPMC_FCLK if ((ADVWrOffTime – ClkActivationTime) is a multiple of 3)
- G = (1 + 0.5 * ADVExtraDelay) * GPMC_FCLK if ((ADVWrOffTime – ClkActivationTime – 1) is a multiple of 3)
- G = (2 + 0.5 * ADVExtraDelay) * GPMC_FCLK if ((ADVWrOffTime – ClkActivationTime – 2) is a multiple of 3)

(8) For OE falling edge (OE activated) / IO DIR rising edge (IN direction):
Case GpmcFCLKDivider = 0:
- H = 0.5 * OEExtraDelay * GPMC_FCLK

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Case GpmcFCLKDivider = 1:
- H = 0.5 * OEExtraDelay * GPMC_FCLK if (ClkActivationTime and OEOnTime are odd) or (ClkActivationTime and OEOnTime are even)
- H = (1 + 0.5 * OEExtraDelay) * GPMC_FCLK otherwise

Case GpmcFCLKDivider = 2:
- H = 0.5 * OEExtraDelay * GPMC_FCLK if ((OEOnTime – ClkActivationTime) is a multiple of 3)
- H = (1 + 0.5 * OEExtraDelay) * GPMC_FCLK if ((OEOnTime – ClkActivationTime – 1) is a multiple of 3)
- H = (2 + 0.5 * OEExtraDelay) * GPMC_FCLK if ((OEOnTime – ClkActivationTime – 2) is a multiple of 3)

For OE rising edge (OE deactivated):
Case GpmcFCLKDivider = 0:
- H = 0.5 * OEExtraDelay * GPMC_FCLK

Case GpmcFCLKDivider = 1:
- H = 0.5 * OEExtraDelay * GPMC_FCLK if (ClkActivationTime and OEOffTime are odd) or (ClkActivationTime and OEOffTime are even)
- H = (1 + 0.5 * OEExtraDelay) * GPMC_FCLK otherwise

Case GpmcFCLKDivider = 2:
- H = 0.5 * OEExtraDelay * GPMC_FCLK if ((OEOffTime – ClkActivationTime) is a multiple of 3)
- H = (1 + 0.5 * OEExtraDelay) * GPMC_FCLK if ((OEOffTime – ClkActivationTime – 1) is a multiple of 3)
- H = (2 + 0.5 * OEExtraDelay) * GPMC_FCLK if ((OEOffTime – ClkActivationTime – 2) is a multiple of 3)

(9) For WE falling edge (WE activated):
Case GpmcFCLKDivider = 0:
- I = 0.5 * WEExtraDelay * GPMC_FCLK

Case GpmcFCLKDivider = 1:
- I = 0.5 * WEExtraDelay * GPMC_FCLK if (ClkActivationTime and WEOnTime are odd) or (ClkActivationTime and WEOnTime are even)
- I = (1 + 0.5 * WEExtraDelay) * GPMC_FCLK otherwise

Case GpmcFCLKDivider = 2:
- I = 0.5 * WEExtraDelay * GPMC_FCLK if ((WEOnTime – ClkActivationTime) is a multiple of 3)
- I = (1 + 0.5 * WEExtraDelay) * GPMC_FCLK if ((WEOnTime – ClkActivationTime – 1) is a multiple of 3)
- I = (2 + 0.5 * WEExtraDelay) * GPMC_FCLK if ((WEOnTime – ClkActivationTime – 2) is a multiple of 3)

For WE rising edge (WE deactivated):
Case GpmcFCLKDivider = 0:
- I = 0.5 * WEExtraDelay * GPMC_FCLK

Case GpmcFCLKDivider = 1:
- I = 0.5 * WEExtraDelay * GPMC_FCLK if (ClkActivationTime and WEOffTime are odd) or (ClkActivationTime and WEOffTime are even)
- I = (1 + 0.5 * WEExtraDelay) * GPMC_FCLK otherwise

Case GpmcFCLKDivider = 2:
- I = 0.5 * WEExtraDelay * GPMC_FCLK if ((WEOffTime – ClkActivationTime) is a multiple of 3)
- I = (1 + 0.5 * WEExtraDelay) * GPMC_FCLK if ((WEOffTime – ClkActivationTime – 1) is a multiple of 3)
- I = (2 + 0.5 * WEExtraDelay) * GPMC_FCLK if ((WEOffTime – ClkActivationTime – 2) is a multiple of 3)

(10) J = GPMC_FCLK period

(11) In gpmc_ncsx, x is equal to 0, 1, 2, 3, 4, 5, 6, or 7.
In gpmc_waitx, x is equal to 0, 1, 2, or 3.

(12) P = gpmc_clk period

(13) For read: K = (ADVRdOffTime – ADVOnTime) * (TimeParaGranularity + 1) * GPMC_FCLK
For write: K = (ADVWrOffTime – ADVOnTime) * (TimeParaGranularity + 1) * GPMC_FCLK

(14) GPMC_FCLK is General Purpose Memory Controller internal functional clock.

(15) Related to the gpmc_clk output clock maximum and minimum frequency programmable in I/F module by setting the GPMC_CONFIG1_CSx configuration register bit fields GpmcFCLKDivider

(16) The jitter probability density can be approximated by a Gaussian function.

(17) M = (RdCycleTime – AccessTime) * (TimeParaGranularity + 1) * GPMC_FCLK
Above M parameter expression is given as one example of GPMC programming. IO DIR signal will go from IN to OUT after both RdCycleTime and BusTurnAround completion. Behaviour of IO direction signal does depend on kind of successive Read/Write accesses performed to Memory and multiplexed or nonmultiplexed memory addressing scheme, bus keeping feature enabled or not. IO DIR behaviour is automactically handled by GPMC controller.

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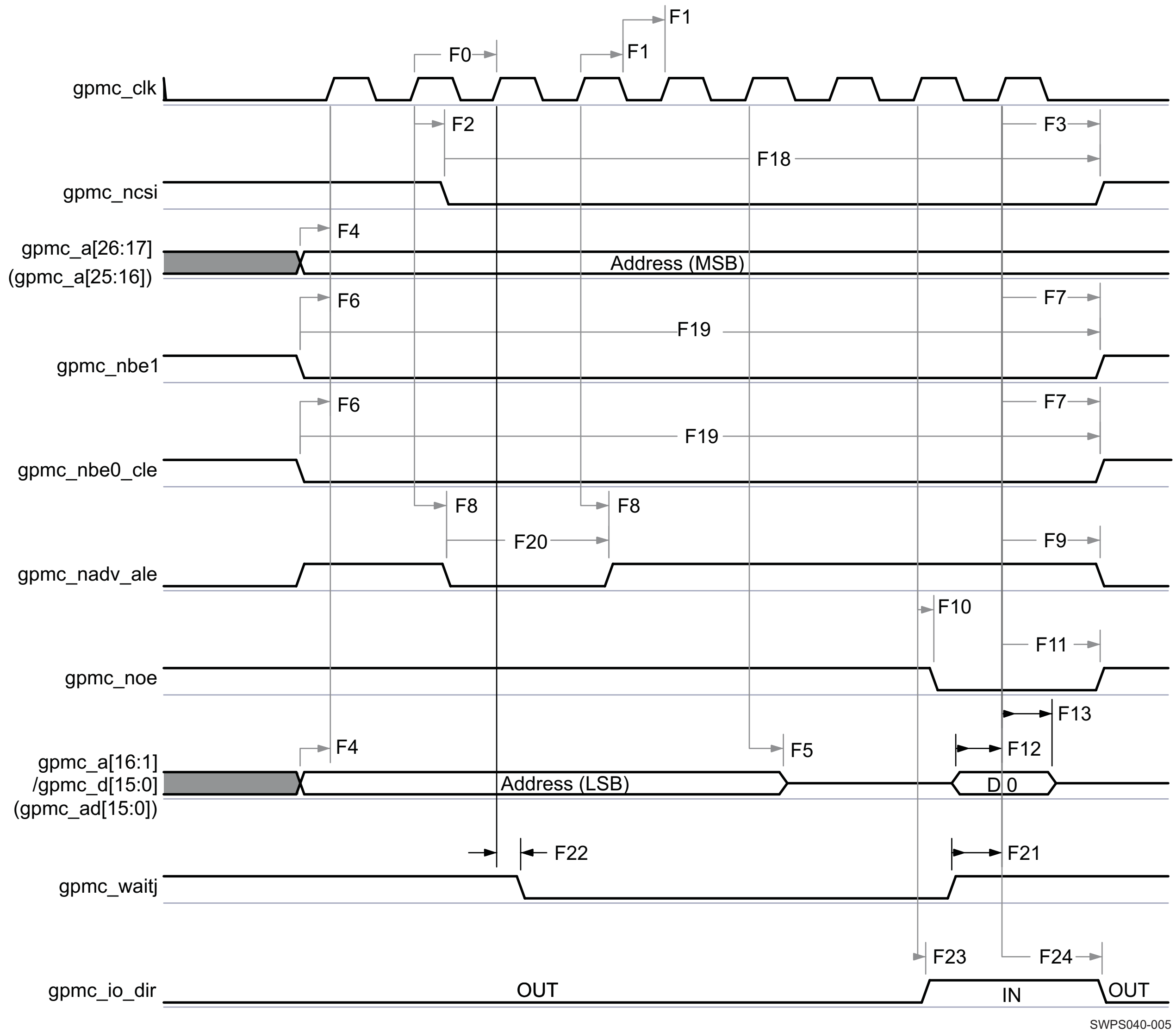

Figure 6-6. GPMC / Multiplexed 16-bit NOR Flash—Synchronous Single Read(1)(2)

(1) In gpmc_ncsi, i is equal to 0, 1, 2, 3, 4, 5, 6, or 7.

(2) In gpmc_waitj, x is equal to 0, 1, 2, or 3.

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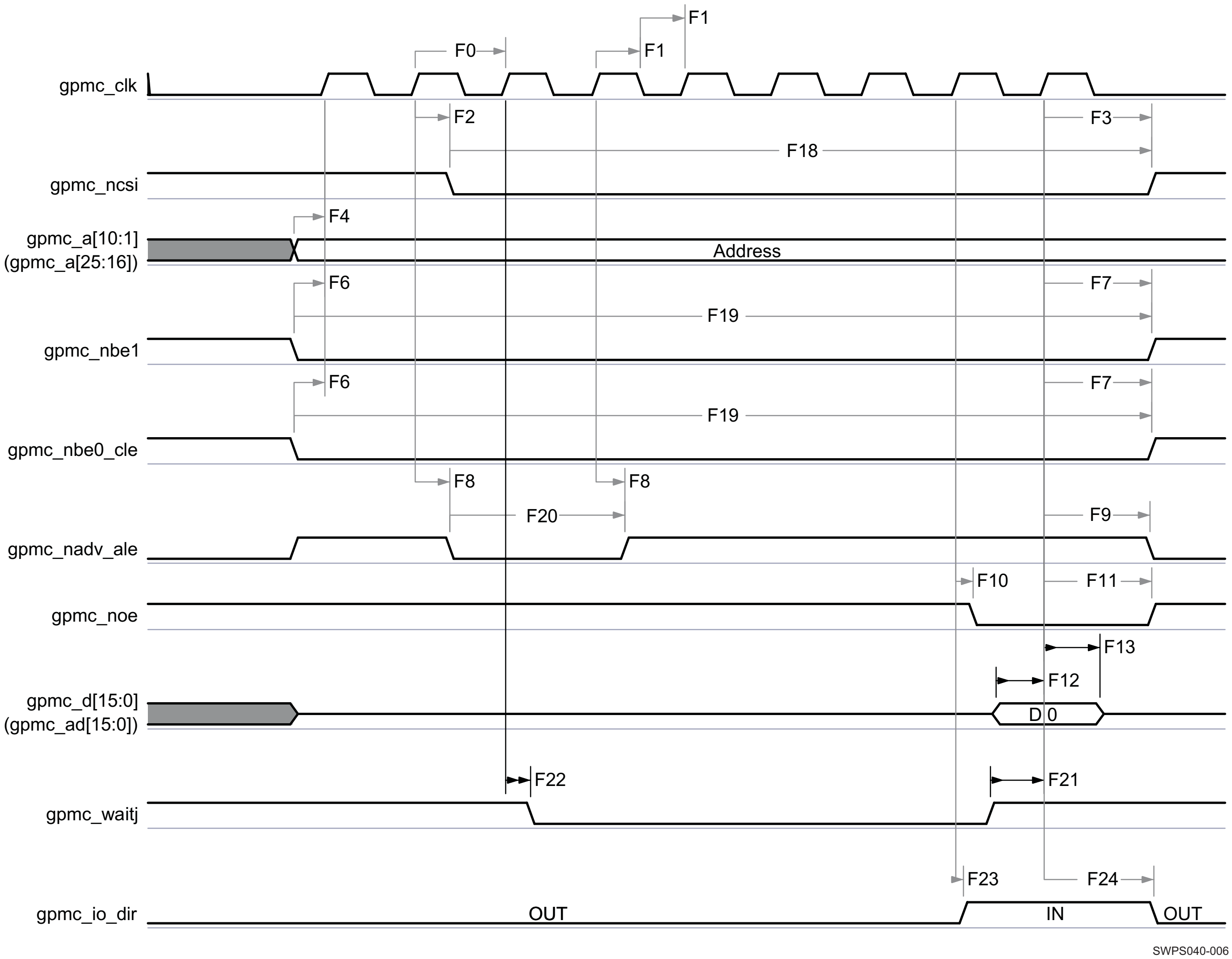

Figure 6-7. GPMC / Nonmultiplexed 16-bit NOR Flash—Synchronous Single Read(1)(2)(3)

(1) In gpmc_ncsi, i is equal to 0, 1, 2, 3, 4, 5, 6, or 7.

(2) In gpmc_waitj, j is equal to 0, 1, 2, or 3.

(3) Nonmultiplexed NOR interface can be used only with a limited address range corresponding to 10 address bits.

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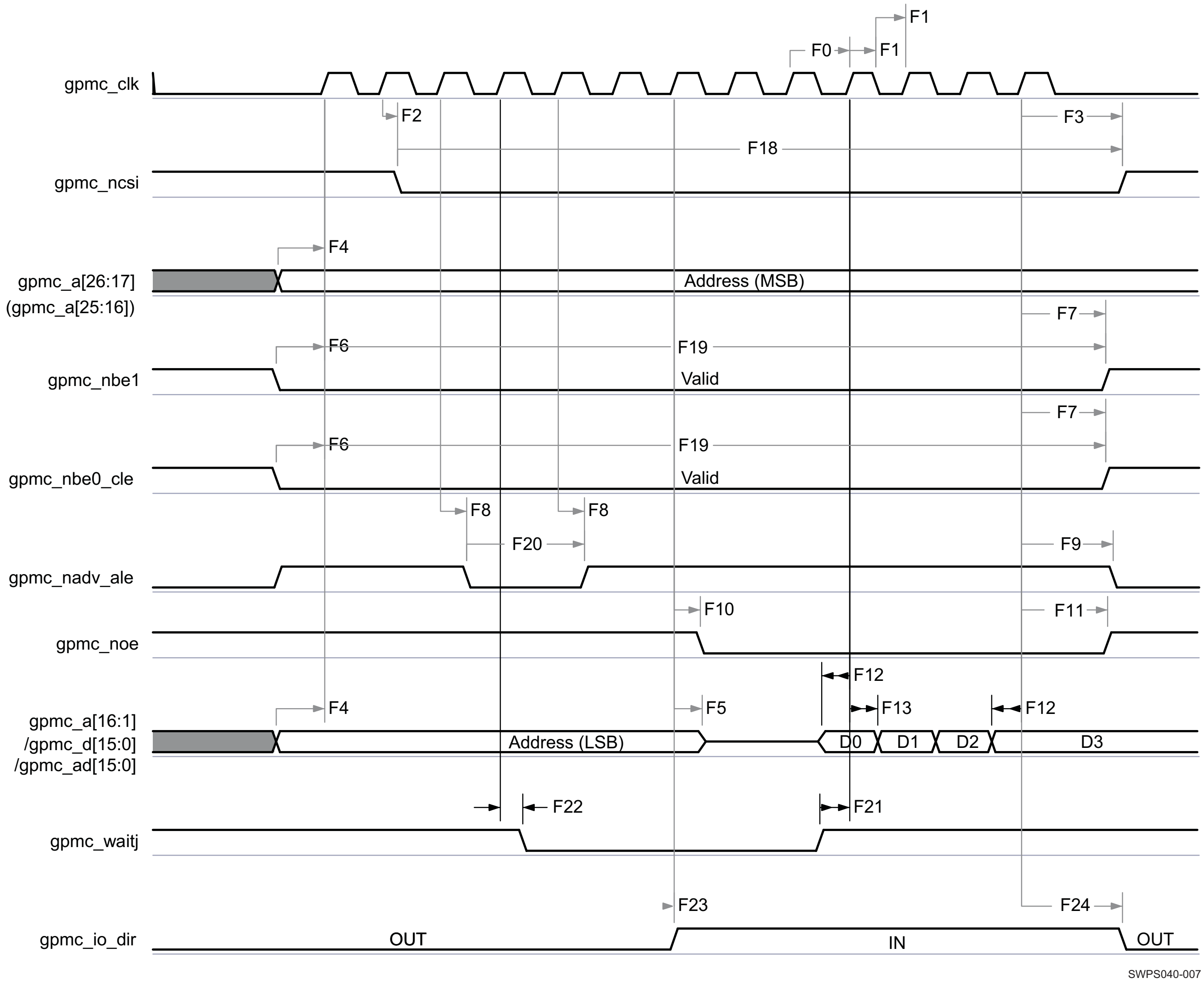

Figure 6-8. GPMC / Multiplexed 16-bit NOR Flash—Synchronous Burst Read 4x16 Bits(1)(2)

(1) In gpmc_ncsi, i is equal to 0, 1, 2, 3, 4, 5, 6, or 7.

(2) In gpmc_waitj, j is equal to 0, 1, 2, or 3.

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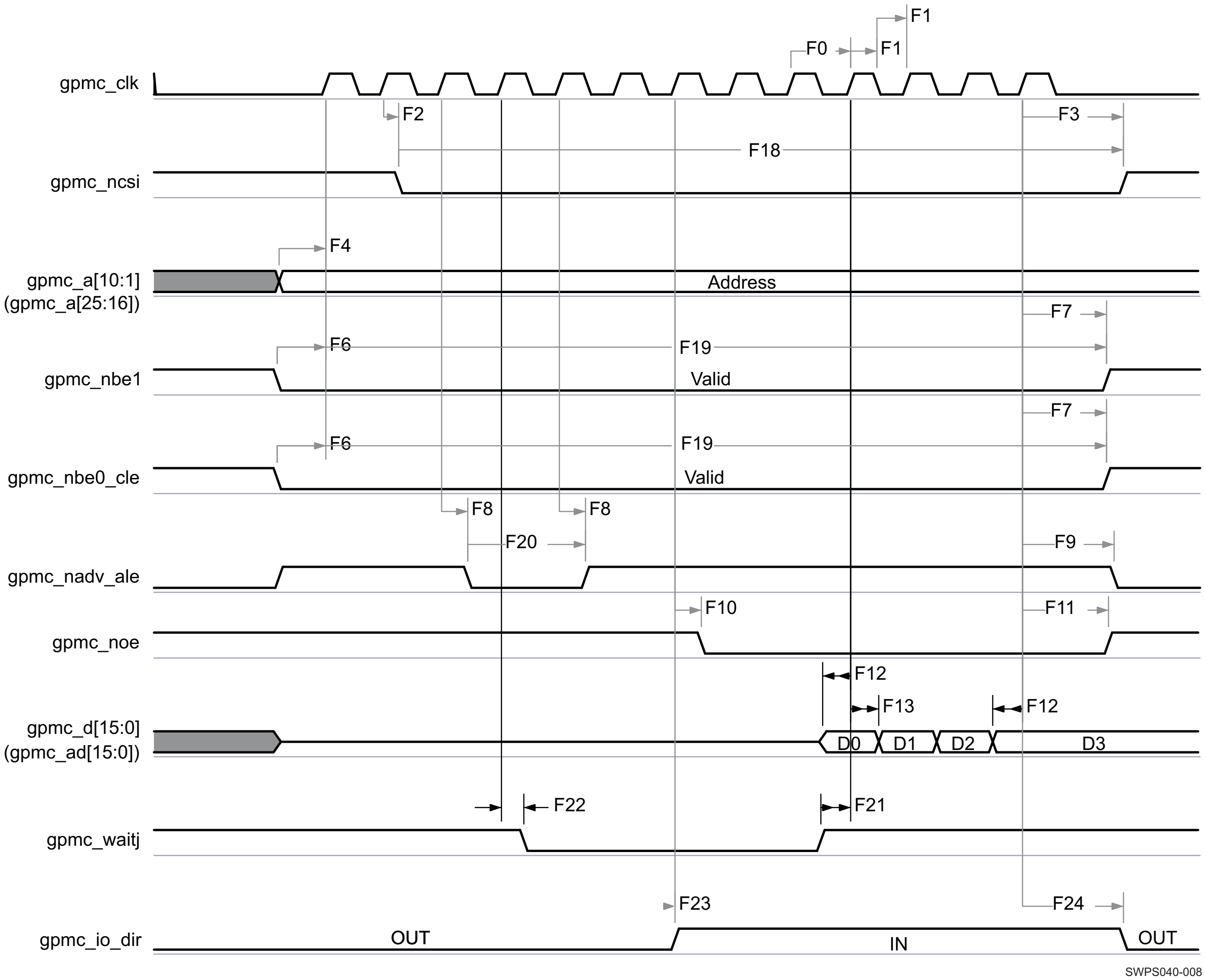

Figure 6-9. GPMC / Nonmultiplexed 16-bit NOR Flash—Synchronous Burst Read 4x16 Bits(1)(2)(3)

(1) In gpmc_ncsi, i is equal to 0, 1, 2, 3, 4, 5, 6, or 7.

(2) In gpmc_waitj, j is equal to 0, 1, 2, or 3.

(3) Nonmultiplexed NOR interface can be used only with a limited address range corresponding to 10 address bits.

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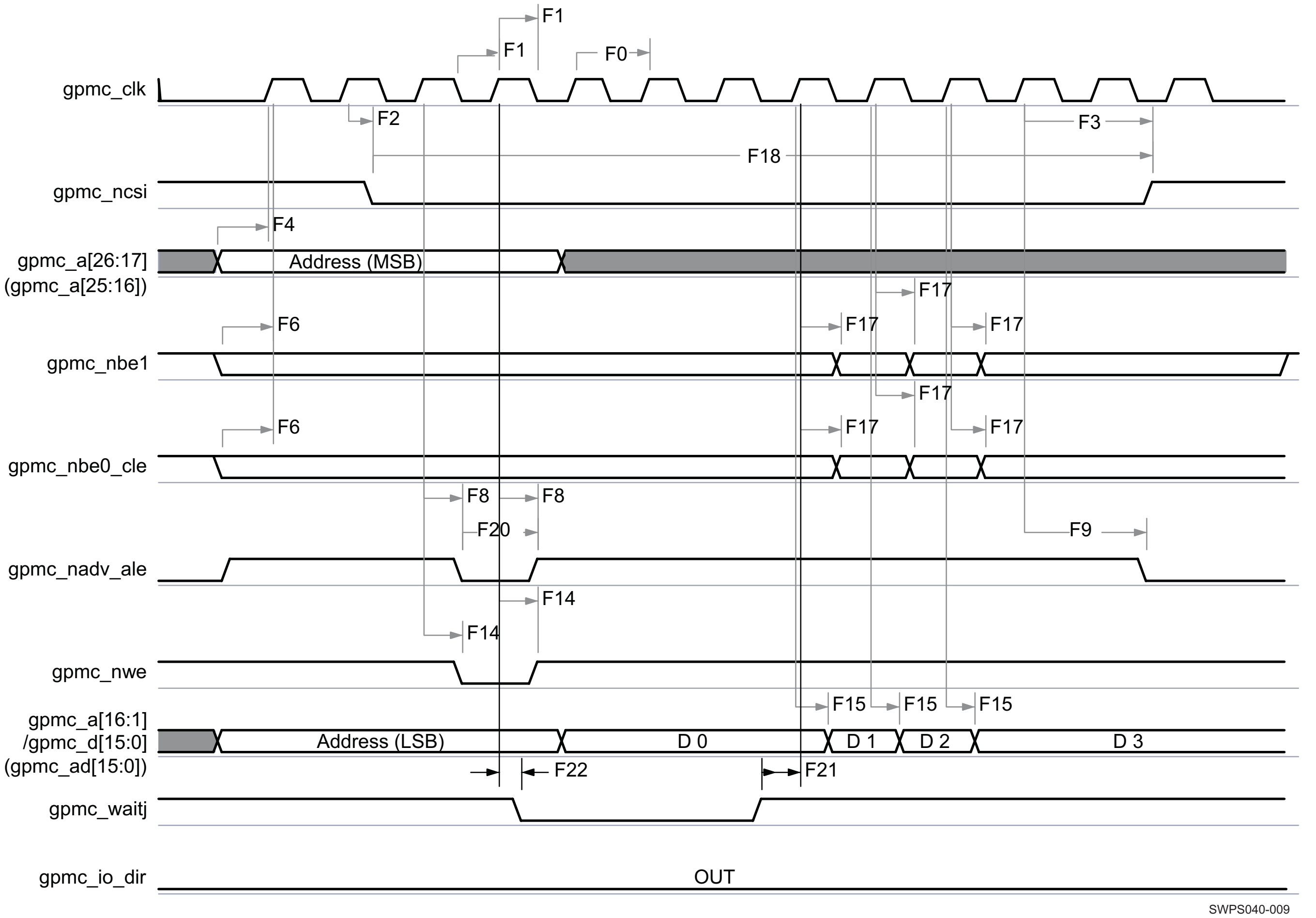

Figure 6-10. GPMC / Multiplexed 16-bit NOR Flash—Synchronous Burst Write 4 x 16 Bits(1)(2)

(1) In gpmc_ncsi, i is equal to 0, 1, 2, 3, 4, 5, 6, or 7.

(2) In gpmc_waitj, j is equal to 0, 1, 2, or 3.

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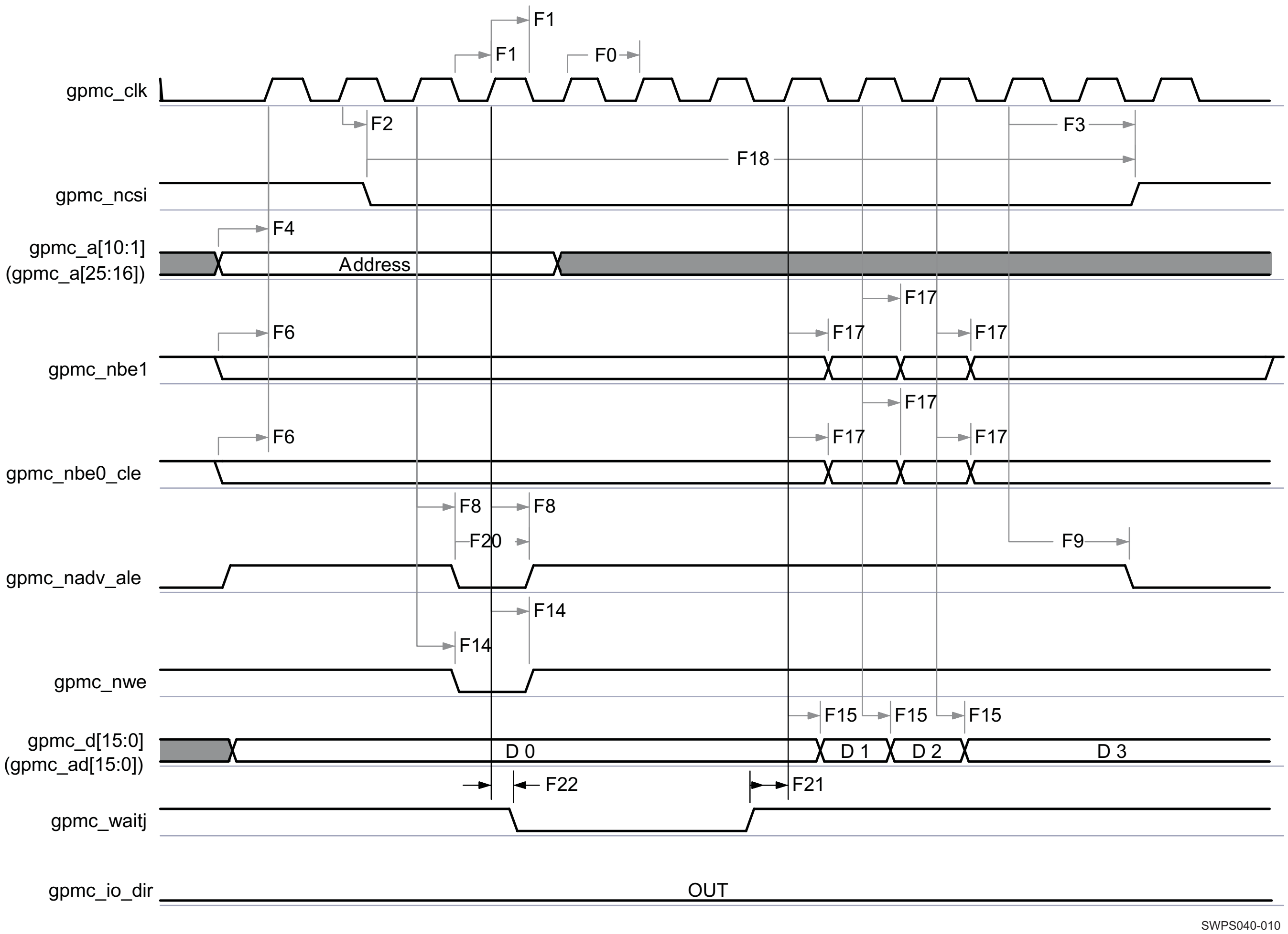

Figure 6-11. GPMC / Nonmultiplexed 16-bit NOR Flash—Synchronous Burst Write 4 x 16 Bits(1)(2)(3)

(1) In gpmc_ncsi, i is equal to 0, 1, 2, 3, 4, 5, 6, or 7.

(2) In gpmc_waitj, j is equal to 0, 1, 2, or 3.

(3) Nonmultiplexed NOR interface can be used only with a limited address range corresponding to 10 address bits.

6.4.1.3 GPMC/NOR Flash Interface—Asynchronous Mode

Table 6-10 and Table 6-11 assume testing over the recommended operating conditions and electrical characteristic conditions below (see Figure 6-12 through Figure 6-17).

Table 6-8. GPMC/NOR Flash Timing Conditions—Asynchronous Mode(1)(2)(3)

TIMING CONDITION PARAMETER		VALUE		UNIT
		MIN	MAX	
Input Conditions				
t_R	Input signal rise time	1.80		ns
t_F	Input signal fall time	1.80		ns
PCB Conditions				
	Number of external peripherals		1	
	Far end load		10	pF
	Trace length		4	cm
	Characteristics impedance	30	50	Ω

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(1) IO settings except gpmc_nwp: LB0 = 1.
For more information, see the Control Module / Control Module Functional Description/ Functional Register Description / Signal Integrity Parameter Control Registers with Pad Group Assignment section of the OMAP4430 TRM.
IO settings for gpmc_nwp: MB[1:0] = 01 and LB0 = 0.
For more information, see the Control Module / Control Module Functional Description/ Functional Register Description / Signal Integrity Parameter Control Registers with Pad Group Assignment / 50-Ω Output Buffer I/Os with Combined Mode and Load Settings section of the OMAP4430 TRM.

(2) In this table the rise and fall times are calculated for 20% to 80% of VDDS. For more information on the corresponding OMAP4 VDDS power supply name, see Table 2-1, POWER [9] column with the ball name.

(3) To have an idea of the output OMAP4 ball load supported for this application, you can consider the following:
Output OMAP4 ball load = Far End load + 1.34 pF/cm typical x trace length (cm).

Table 6-9. GPMC/NOR Flash—Asynchronous Mode—Internal Parameters

NO.	PARAMETER	OPP100		OPP50		UNIT
		MIN	MAX	MIN	MAX	
FI1	Max output data generation delay from internal functional clock		6.5		13.7	ns
FI2	Max input data capture delay by internal functional clock		4.0		8.1	ns
FI3	Max chip select generation delay from internal functional clock		6.5		13.7	ns
FI4	Max address generation delay from internal functional clock		6.5		13.7	ns
FI5	Max address valid generation delay from internal functional clock		6.5		13.7	ns
FI6	Max byte enable generation delay from internal functional clock		6.5		13.7	ns
FI7	Max output enable generation delay from internal functional clock		6.5		13.7	ns
FI8	Max write enable generation delay from internal functional clock		6.5		13.7	ns
FI9	Max functional clock skew		100.0		200.0	ps
FI10	Max IO direction generation delay from internal functional clock		6.5		13.7	ps

Table 6-10. GPMC/NOR Flash Timing Requirements—Asynchronous Mode[1][2][3]

NO.	PARAMETER		OPP100		OPP50		UNIT
			MIN	MAX	MIN	MAX	
FA5	$t_{ACc(DAT)}$	Data max access time		H[8]		H[8]	GPMC_FCLK cycles
FA20	$t_{ACC1-PGMODE(DAT)}$	Page mode successive data max access time		P[15]		P[15]	GPMC_FCLK cycles
FA21	$t_{ACC2-PGMODE(DAT)}$	Page mode first data max access time		H[8]		H[8]	GPMC_FCLK cycles

(1) FA5 parameter illustrates amount of time required to internally sample input Data. It is expressed in number of GPMC functional clock cycles. From start of read cycle and after FA5 functional clock cycles, input Data will be internally sampled by active functional clock edge. FA5 value must be stored inside AccessTime register bits field.

(2) FA21 parameter illustrates amount of time required to internally sample first input Page Data. It is expressed in number of GPMC functional clock cycles. From start of read cycle and after FA21 functional clock cycles, First input Page Data will be internally sampled by active functional clock edge. FA21 value must be stored inside AccessTime register bits field.

(3) FA20 parameter illustrates amount of time required to internally sample successive input Page Data. It is expressed in number of GPMC functional clock cycles. After each access to input Page Data, next input Page Data will be internally sampled by active functional clock edge after FA20 functional clock cycles. FA20 value must be stored in PageBurstAccessTime register bits field.

Table 6-11. GPMC/NOR Flash Switching Characteristics—Asynchronous Mode

NO.	PARAMETER			OPP100		OPP50		UNIT
				MIN	MAX	MIN	MAX	
	$t_{R(DO)}$	Rise time, output data			2		2	ns
	$t_{F(DO)}$	Fall time, output data			2		2	ns
FA0	$t_{w(nBEV)}$	Pulse duration, gpmc_nbe0_cle, gpmc_nbe1 valid time	Read	N[13]		N[13]		ns
			Write	N[13]		N[13]		ns
FA1	$t_{w(nCSV)}$	Pulse duration, gpmc_ncsx low	Read	A[1]		A[1]		ns
			Write	A[1]		A[1]		ns

Table 6-11. GPMC/NOR Flash Switching Characteristics—Asynchronous Mode (continued)

NO.	PARAMETER			OPP100		OPP50		UNIT
				MIN	MAX	MIN	MAX	
FA3	$t_{d(nCSV-nADVIV)}$	Delay time, gpmc_ncsx[14] valid to gpmc_nadv_ale invalid	Read	B[2] – 0.2	B[2] + 2.0	B[2] – 0.2	B[2] + 2.6	ns
			Write	B[2] – 0.2	B[2] + 2.0	B[2] – 0.2	B[2] + 2.6	ns
FA4	$t_{d(nCSV-nOEIV)}$	Delay time, gpmc_ncsx[14] valid to gpmc_noe invalid (Single read)		C[3] – 0.2	C[3] + 2.0	C[3] – 0.2	C[3] + 2.6	ns
FA9	$t_{d(AV-nCSV)}$	Delay time, address bus valid to gpmc_ncsx[14] valid		J[10] – 0.2	J[10] + 2.0	J[10] – 0.2	J[10] + 2.6	ns
FA10	$t_{d(nBEV-nCSV)}$	Delay time, gpmc_nbe0_cle, gpmc_nbe1 valid to gpmc_ncsx[14] valid		J[10] – 0.2	J[10] + 2.0	J[10] – 0.2	J[10] + 2.6	ns
FA12	$t_{d(nCSV-nADVV)}$	Delay time, gpmc_ncsx[14] valid to gpmc_nadv_ale valid		K[11] – 0.2	K[11] + 2.0	K[11] – 0.2	K[11] + 2.6	ns
FA13	$t_{d(nCSV-nOEV)}$	Delay time, gpmc_ncsx[14] valid to gpmc_noe valid		L[12] – 0.2	L[12] + 2.0	L[12] – 0.2	L[12] + 2.6	ns
FA14	$t_{d(nCSV-IODIR)}$	Delay time, gpmc_ncsx[14] valid to gpmc_io_dir high		L[12] – 0.2	L[12] + 2.0	L[12] – 0.2	L[12] + 2.6	ns
FA15	$t_{d(nCSV-IODIR)}$	Delay time, gpmc_ncsx[14] valid to gpmc_io_dir low		M[16] – 0.2	M[16] + 2.0	M[16] – 0.2	M[16] + 2.6	ns
FA16	$t_{w(AIV)}$	Address invalid duration between 2 successive R/W accesses		G[7]		G[7]		ns
FA18	$t_{d(nCSV-nOEIV)}$	Delay time, gpmc_ncsx[14] valid to gpmc_noe invalid (Burst read)		I[9] – 0.2	I[9] + 2.0	I[9] – 0.2	I[9] + 2.6	ns
FA20	$t_{w(AV)}$	Pulse duration, address valid – 2nd, 3rd, and 4th accesses		D[4]		D[4]		ns
FA25	$t_{d(nCSV-nWEV)}$	Delay time, gpmc_ncsx[14] valid to gpmc_nwe valid		E[5] – 0.2	E[5] + 2.0	E[5] – 0.2	E[5] + 2.6	ns
FA27	$t_{d(nCSV-nWEIV)}$	Delay time, gpmc_ncsx[14] valid to gpmc_nwe invalid		F[6] – 0.2	F[6] + 2.0	F[6] – 0.2	F[6] + 2.6	ns
FA28	$t_{d(nWEV-DV)}$	Delay time, gpmc_ nwe valid to data bus valid			2		2.6	ns
FA29	$t_{d(DV-nCSV)}$	Delay time, data bus valid to gpmc_ncsx[14] valid		J[10] – 0.2	J[10] + 2.0	J[10] – 0.2	J[10] + 2.6	ns
FA37	$t_{d(nOEV-AIV)}$	Delay time, gpmc_noe valid to gpmc_a[16:1] address phase end			2		2.6	ns

(1) For single read: A = (CSRdOffTime – CSOnTime) * (TimeParaGranularity + 1) * GPMC_FCLK
For single write: A = (CSWrOffTime – CSOnTime) * (TimeParaGranularity + 1) * GPMC_FCLK
For burst read: A = (CSRdOffTime – CSOnTime + (n – 1) * PageBurstAccessTime) * (TimeParaGranularity + 1) * GPMC_FCLK with n the page burst access number
For burst write: A = (CSWrOffTime – CSOnTime + (n – 1) * PageBurstAccessTime) * (TimeParaGranularity + 1) * GPMC_FCLK with n the page burst access number

(2) For reading: B = ((ADVRdOffTime – CSOnTime) * (TimeParaGranularity + 1) + 0.5 * (ADVExtraDelay – CSExtraDelay)) * GPMC_FCLK
For writing: B = ((ADVWrOffTime – CSOnTime) * (TimeParaGranularity + 1) + 0.5 * (ADVExtraDelay – CSExtraDelay)) * GPMC_FCLK

(3) C = ((OEOffTime – CSOnTime) * (TimeParaGranularity + 1) + 0.5 * (OEExtraDelay – CSExtraDelay)) * GPMC_FCLK

(4) D = PageBurstAccessTime * (TimeParaGranularity + 1) * GPMC_FCLK

(5) E = ((WEOnTime – CSOnTime) * (TimeParaGranularity + 1) + 0.5 * (WEExtraDelay – CSExtraDelay)) * GPMC_FCLK

(6) F = ((WEOffTime – CSOnTime) * (TimeParaGranularity + 1) + 0.5 * (WEExtraDelay – CSExtraDelay)) * GPMC_FCLK

(7) G = Cycle2CycleDelay * GPMC_FCLK

(8) H = AccessTime * (TimeParaGranularity + 1)

(9) I = ((OEOffTime + (n – 1) * PageBurstAccessTime – CSOnTime) * (TimeParaGranularity + 1) + 0.5 * (OEExtraDelay – CSExtraDelay)) * GPMC_FCLK

(10) J = (CSOnTime * (TimeParaGranularity + 1) + 0.5 * CSExtraDelay) * GPMC_FCLK

(11) K = ((ADVOnTime – CSOnTime) * (TimeParaGranularity + 1) + 0.5 * (ADVExtraDelay – CSExtraDelay)) * GPMC_FCLK

(12) L = ((OEOnTime – CSOnTime) * (TimeParaGranularity + 1) + 0.5 * (OEExtraDelay – CSExtraDelay)) * GPMC_FCLK

(13) For single read: N = RdCycleTime * (TimeParaGranularity + 1) * GPMC_FCLK
For single write: N = WrCycleTime * (TimeParaGranularity + 1) * GPMC_FCLK
For burst read: N = (RdCycleTime + (n – 1) * PageBurstAccessTime) * (TimeParaGranularity + 1) * GPMC_FCLK
For burst write: N = (WrCycleTime + (n – 1) * PageBurstAccessTime) * (TimeParaGranularity + 1) * GPMC_FCLK

(14) In gpmc_ncsx, x is equal to 0, 1, 2, 3, 4, 5, 6, or 7.

(15) P = PageBurstAccessTime * (TimeParaGranularity + 1)

(16) M = ((RdCycleTime – CSOnTime) * (TimeParaGranularity + 1) – 0.5 * CSExtraDelay) * GPMC_FCLK
Above M parameter expression is given as one example of GPMC programming. IO DIR signal will go from IN to OUT after both RdCycleTime and BusTurnAround completion. Behaviour of IO direction signal does depend on kind of successive read/write accesses performed to memory and multiplexed or non/multiplexed memory addressing scheme, bus keeping feature enabled or not. IO DIR behaviour is automactically handled by GPMC controller

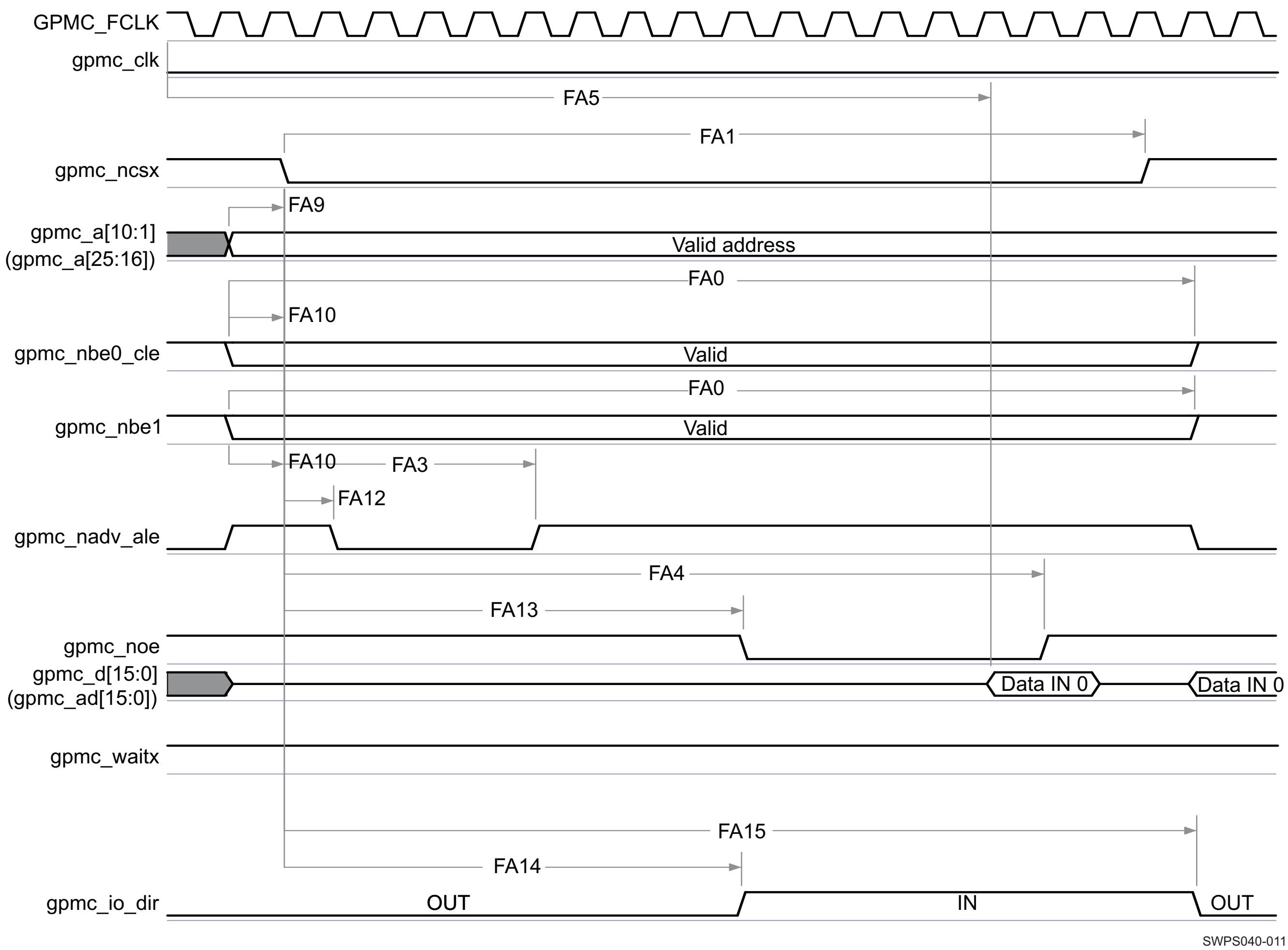

Figure 6-12. GPMC / NOR Flash—Asynchronous Read—Single Word Timing(1)(2)(3)

(1) In gpmc_ncsx, x is equal to 0, 1, 2, 3, 4, 5, 6, or 7. In gpmc_waitx, x is equal to 0, 1, 2, or 3.

(2) FA5 parameter illustrates amount of time required to internally sample input data. It is expressed in number of GPMC functional clock cycles. From start of read cycle and after FA5 functional clock cycles, input data will be internally sampled by active functional clock edge. FA5 value must be stored inside AccessTime register bits field.

(3) GPMC_FCLK is an internal clock (GPMC functional clock) not provided externally.

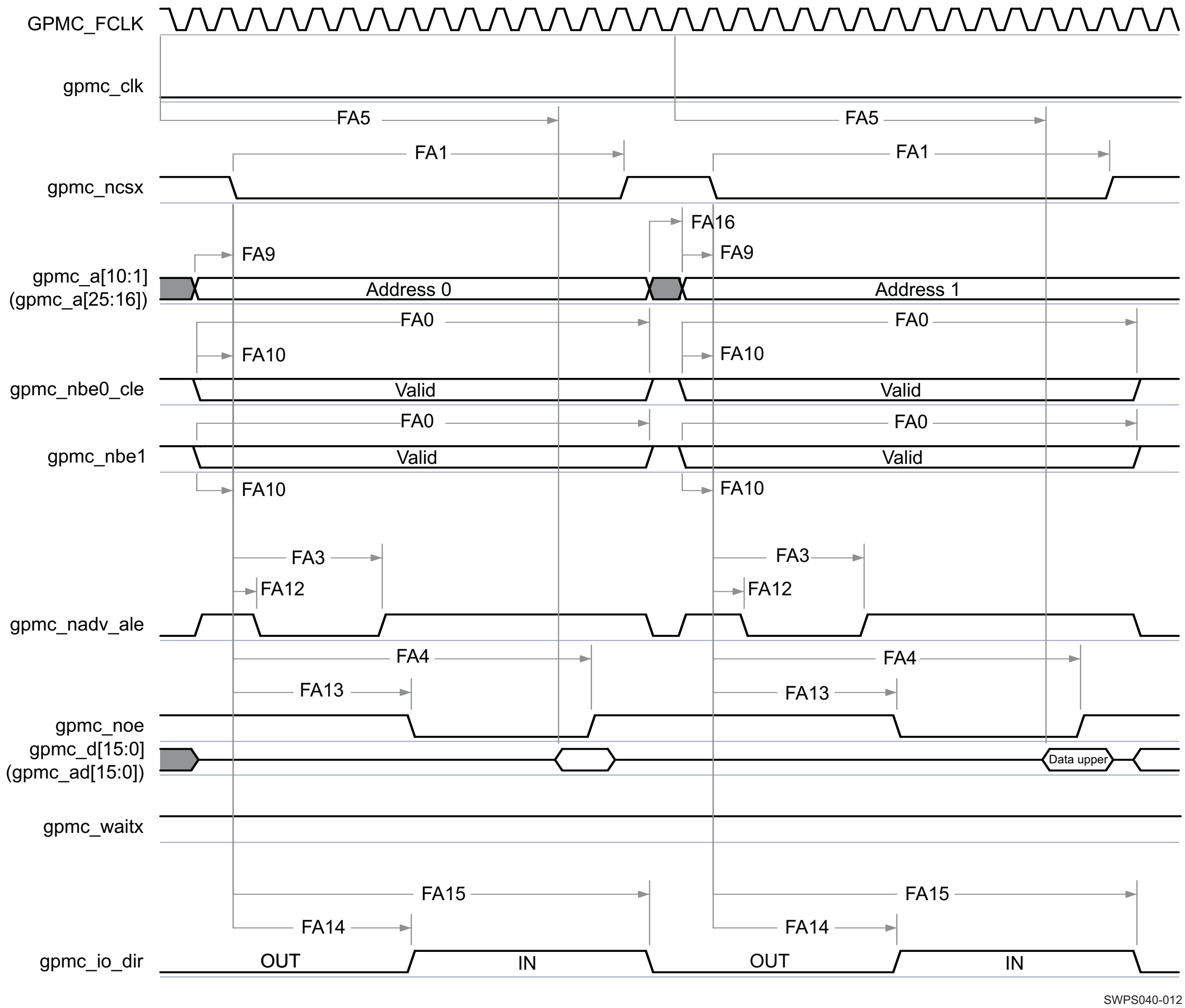

Figure 6-13. GPMC / NOR Flash—Asynchronous Read—32-bit Timing(1)(2)(3)

(1) In gpmc_ncsx, x is equal to 0, 1, 2, 3, 4, 5, 6, or 7. In gpmc_waitx, x is equal to 0, 1, 2, or 3.

(2) FA5 parameter illustrates amount of time required to internally sample input data. It is expressed in number of GPMC functional clock cycles. From start of read cycle and after FA5 functional clock cycles, input Data will be internally sampled by active functional clock edge. FA5 value must be stored inside AccessTime register bits field.

(3) GPMC_FCLK is an internal clock (GPMC functional clock) not provided externally.

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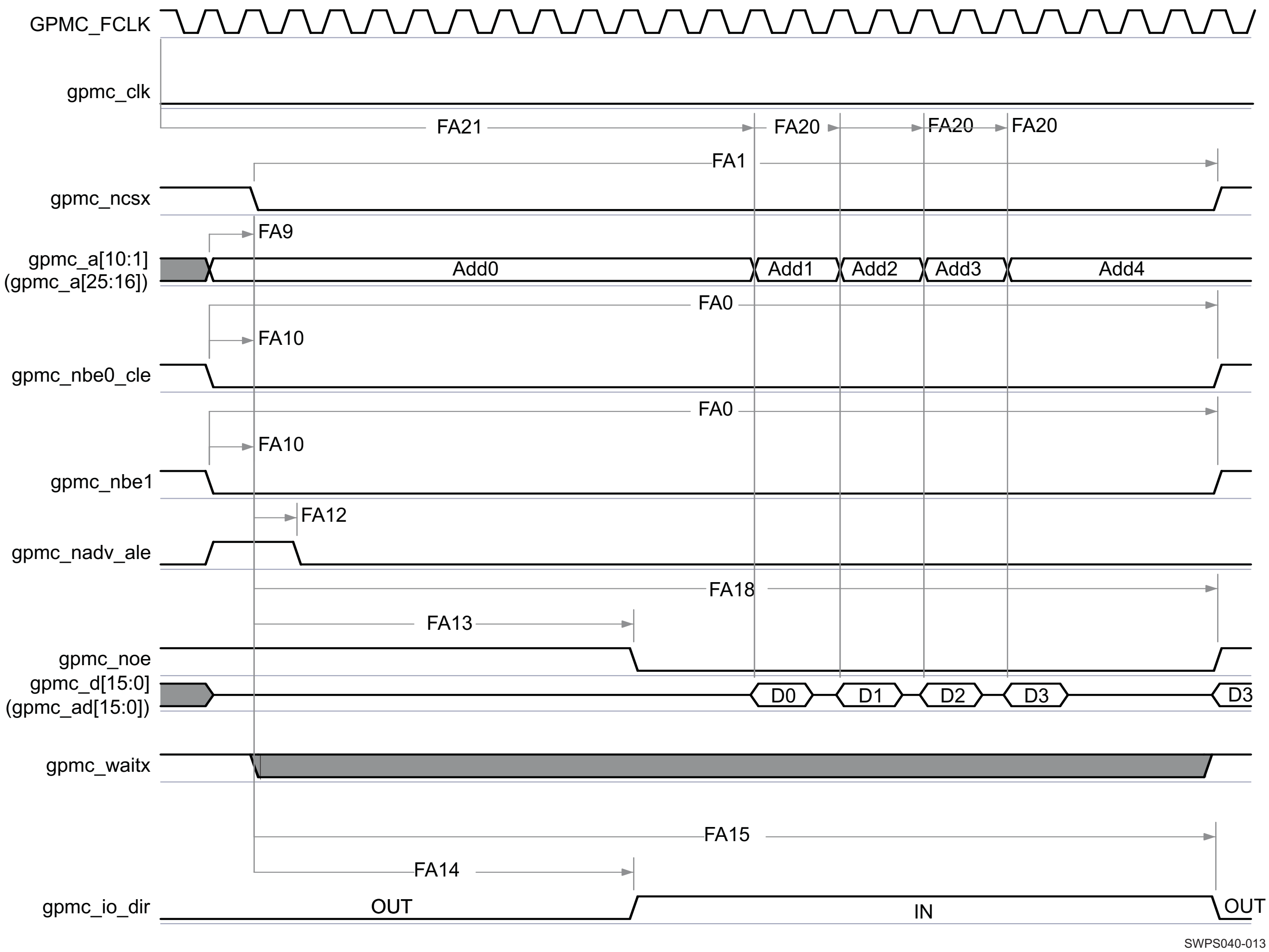

Figure 6-14. GPMC / NOR Flash—Asynchronous Read—Page Mode 4x16-bit Timing(1)(2)(3)(4)

(1) In gpmc_ncsx, x is equal to 0, 1, 2, 3, 4, 5, 6, or 7. In gpmc_waitx, x is equal to 0, 1, or 2.

(2) FA21 parameter illustrates amount of time required to internally sample first input Page Data. It is expressed in number of GPMC functional clock cycles. From start of read cycle and after FA21 functional clock cycles, First input Page Data will be internally sampled by active functional clock edge. FA21 calculation must be stored inside AccessTime register bits field.

(3) FA20 parameter illustrates amount of time required to internally sample successive input Page Data. It is expressed in number of GPMC functional clock cycles. After each access to input Page Data, next input Page Data will be internally sampled by active functional clock edge after FA20 functional clock cycles. FA20 is also the duration of address phases for successive input Page Data (excluding first input Page Data). FA20 value must be stored in PageBurstAccessTime register bits field.

(4) GPMC_FCLK is an internal clock (GPMC functional clock) not provided externally.

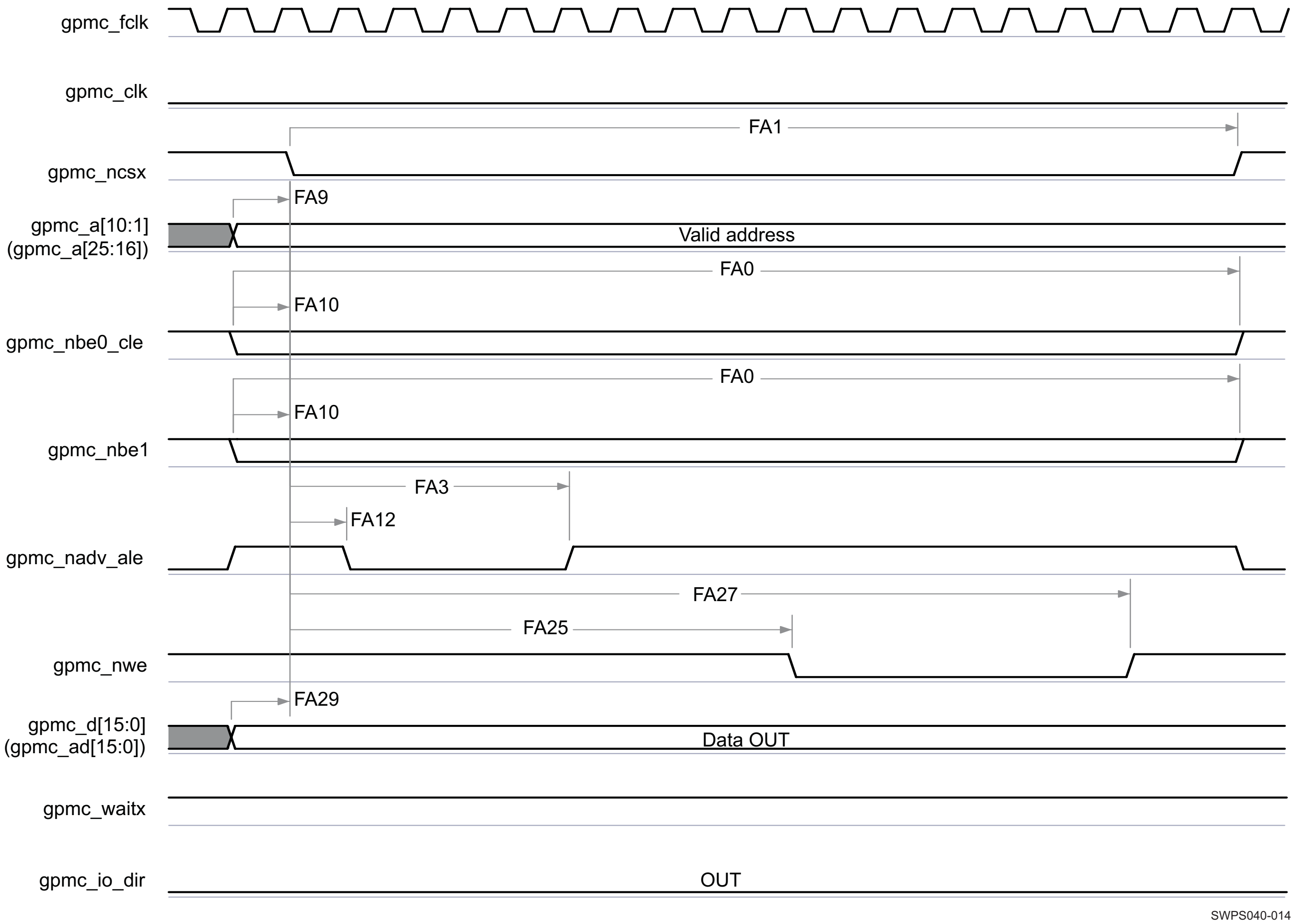

Figure 6-15. GPMC / NOR Flash—Asynchronous Write—Single Word Timing[(1)]

(1) In gpmc_ncsx, x is equal to 0, 1, 2, 3, 4, 5, 6, or 7. In gpmc_waitx, x is equal to 0, 1, or 2.

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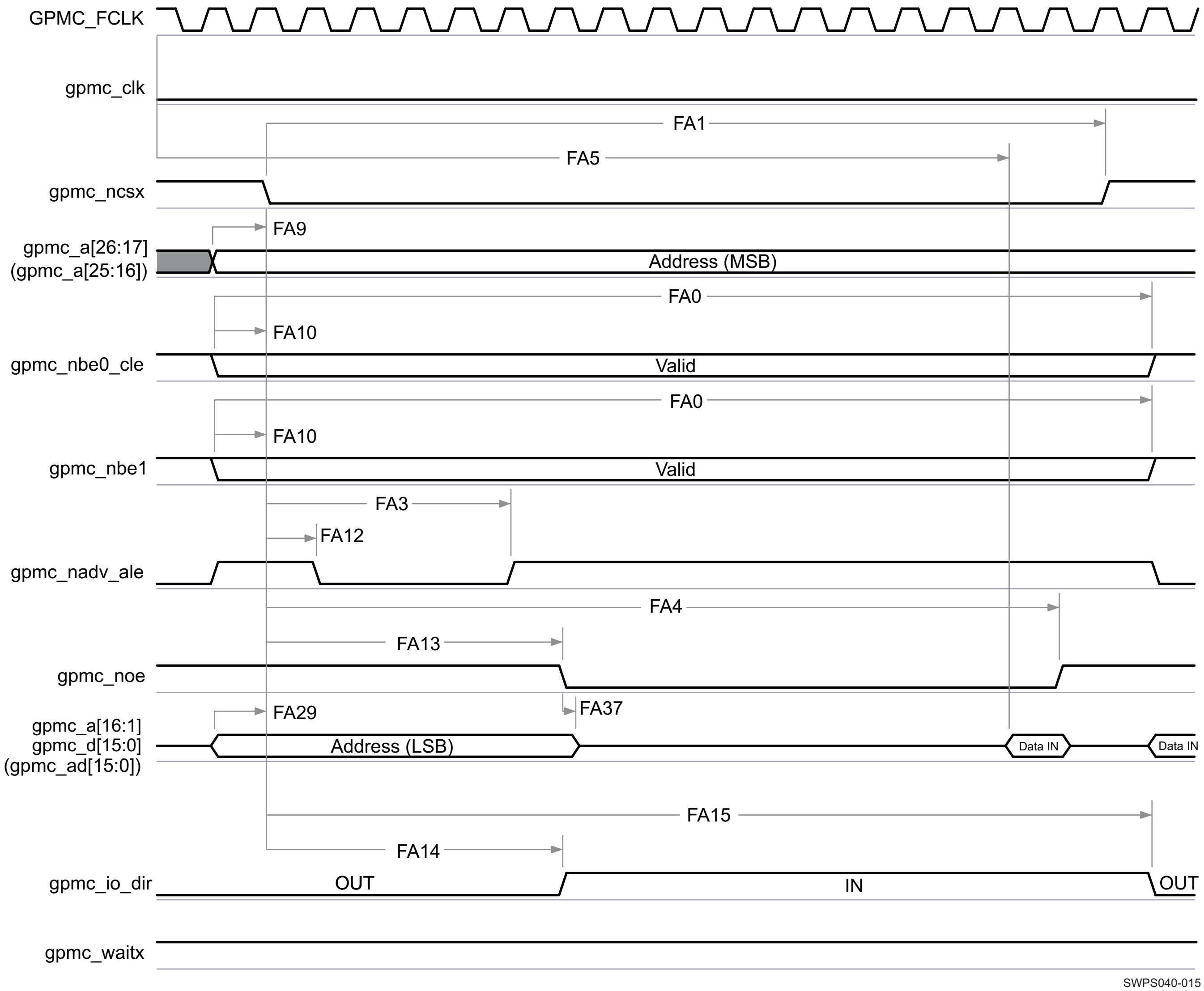

Figure 6-16. GPMC / Multiplexed NOR Flash—Asynchronous Read—Single Word Timing(1)(2)(3)

(1) In gpmc_ncsx, x is equal to 0, 1, 2, 3, 4, 5, 6, or 7. In gpmc_waitx, x is equal to 0, 1, or 2.

(2) FA5 parameter illustrates amount of time required to internally sample input Data. It is expressed in number of GPMC functional clock cycles. From start of read cycle and after FA5 functional clock cycles, input Data will be internally sampled by active functional clock edge. FA5 value must be stored inside AccessTime register bits field.

(3) GPMC_FCLK is an internal clock (GPMC functional clock) not provided externally.

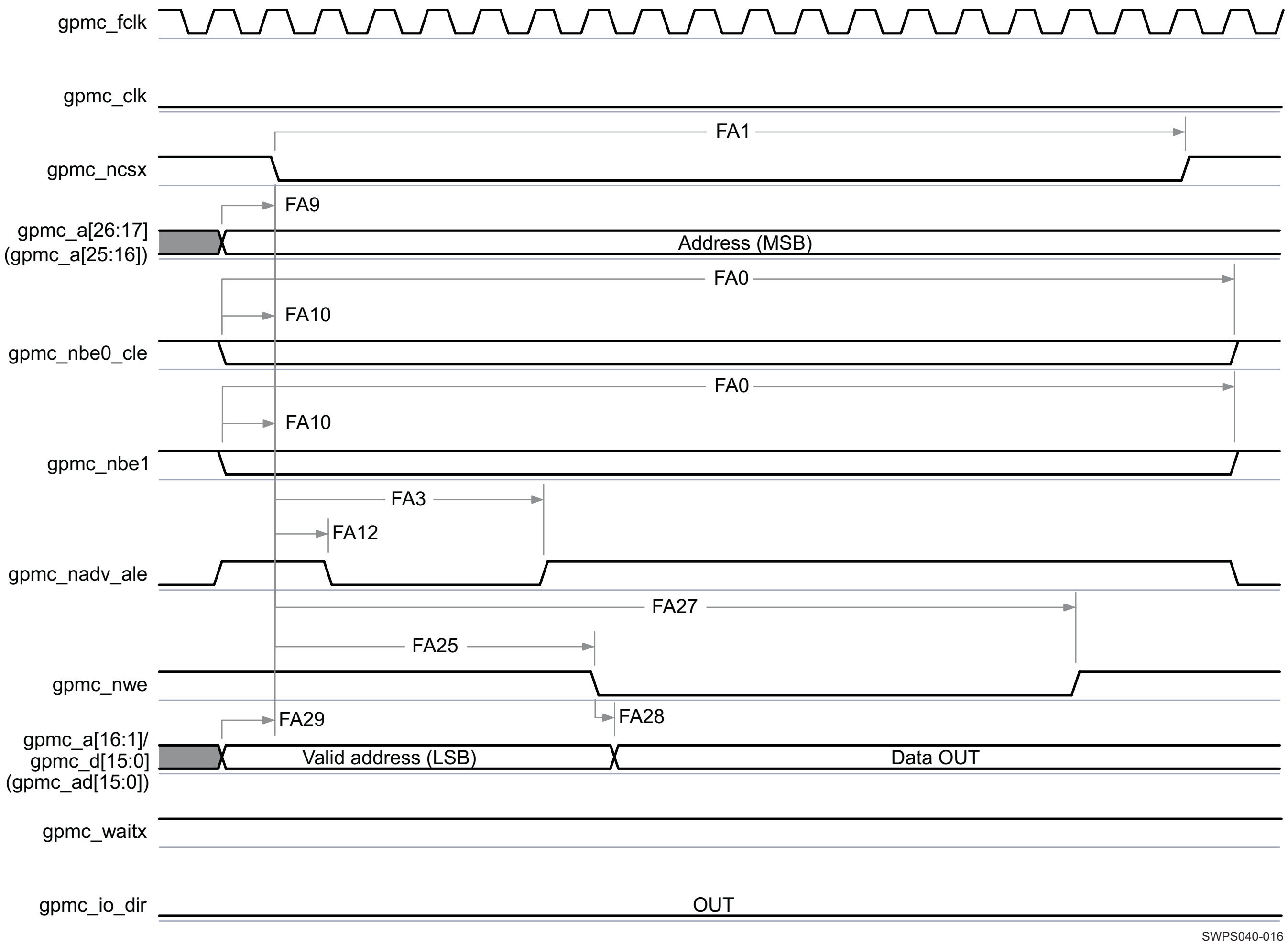

Figure 6-17. GPMC / Multiplexed NOR Flash—Asynchronous Write—Single Word Timing(1)

(1) In gpmc_ncsx, x is equal to 0, 1, 2, 3, 4, 5, 6, or 7. In gpmc_waitx, x is equal to 0, 1, or 2.

6.4.1.4 GPMC/NAND Flash Interface—Asynchronous Mode

Table 6-14 and Table 6-15 assume testing over the recommended operating conditions and electrical characteristic conditions below (see Figure 6-18 through Figure 6-21).

Table 6-12. GPMC/NAND Flash Timing Conditions—Asynchronous Mode(1)(2)(3)

TIMING CONDITION PARAMETER		VALUE		UNIT
		MIN	MAX	
Input Conditions				
t_R	Input signal rise time	1.80		ns
t_F	Input signal fall time	1.80		ns
PCB Conditions				
	Number of external peripherals		1	
	Far end load		10	pF
	Trace length		4	cm
	Characteristics impedance	30	50	Ω

(1) IO settings except gpmc_nwp: LB0 = 1.
For more information, see the Control Module / Control Module Functional Description/ Functional Register Description / Signal Integrity Parameter Control Registers with Pad Group Assignment section of the OMAP4430 TRM.
IO settings for gpmc_nwp: MB[1:0] = 01 and LB0 = 0.
For more information, see the Control Module / Control Module Functional Description/ Functional Register Description / Signal Integrity Parameter Control Registers with Pad Group Assignment / 50-Ω Output Buffer I/Os with Combined Mode and Load Settings section of the OMAP4430 TRM.

(2) In this table the rise and fall times are calculated for 20% to 80% of VDDS. For more information on the corresponding OMAP4 VDDS power supply name, see Table 2-1, POWER [9] column with the ball name.

(3) To have an idea of the output OMAP4 ball load supported for this application, you can consider the following:
Output OMAP4 ball load = Far End load + 1.34 pF/cm typical x trace length (cm).

Table 6-13. GPMC/NAND—Asynchronous Mode—Internal Parameters

NO.	PARAMETER	OPP100		OPP50		UNIT
		MIN	MAX	MIN	MAX	
GNFI1	Maximum output data generation delay from internal functional clock		6.5		13.7	ns
GNFI2	Maximum input data capture delay by internal functional clock		4.0		8.1	ns
GNFI3	Maximum chip select generation delay from internal functional clock		6.5		13.7	ns
GNFI4	Maximum address latch enable generation delay from internal functional clock		6.5		13.7	ns
GNFI5	Maximum command latch enable generation delay from internal functional clock		6.5		13.7	ns
GNFI6	Maximum output enable generation delay from internal functional clock		6.5		13.7	ns
GNFI7	Maximum write enable generation delay from internal functional clock		6.5		13.7	ns
GNFI8	Maximum functional clock skew		100.0		200.0	ps

Table 6-14. GPMC/NAND Flash Timing Requirements—Asynchronous Mode[(1)(2)]

NO.	PARAMETER		OPP100		OPP50		UNIT
			MIN	MAX	MIN	MAX	
GNF12	$t_{ACc(DAT)}$	Data maximum access time		J[(10)]		J[(10)]	GPMC_ FCLK cycles

(1) GNF12 parameter illustrates amount of time required to internally sample input Data. It is expressed in number of GPMC functional clock cycles. From start of read cycle and after GNF12 functional clock cycles, input data will be internally sampled by active functional clock edge. GNF12 value must be stored inside AccessTime register bits field.

(2) See DM Operating Condition Addendum for CORE OPP voltages.

Table 6-15. GPMC/NAND Flash Switching Characteristics—Asynchronous Mode

NO.	PARAMETER		OPP100		OPP50		UNIT
			MIN	MAX	MIN	MAX	
	$t_{R(DO)}$	Rise time, output data		2		2	ns
	$t_{F(DO)}$	Fall time, output data		2		2	ns
GNF0	$t_{w(nWEV)}$	Pulse duration, gpmc_nwe valid time	A[(1)]		A[(1)]		ns
GNF1	$t_{d(nCSV-nWEV)}$	Delay time, gpmc_ncsx valid to gpmc_nwe valid	B[(2)] – 0.2	B[(2)] + 2.0	B[(2)] – 0.2	B[(2)] + 3.7	ns
GNF2	$t_{d(CLEH-nWEV)}$	Delay time, gpmc_nbe0_cle high to gpmc_nwe valid	C[(3)] – 0.2	C[(3)] + 2.0	C[(3)] – 0.2	C[(3)] + 3.7	ns
GNF3	$t_{d(nWEV-DV)}$	Delay time, gpmc_d[15:0] valid to gpmc_nwe valid	D[(4)] – 0.2	D[(4)] + 2.0	D[(4)] – 0.2	D[(4)] + 3.7	ns
GNF4	$t_{d(nWEIV-DIV)}$	Delay time, gpmc_nwe invalid to gpmc_d[15:0] invalid	E[(5)] – 0.2	E[(5)] + 2.0	E[(5)] – 0.2	E[(5)] + 3.7	ns

Table 6-15. GPMC/NAND Flash Switching Characteristics—Asynchronous Mode (continued)

NO.	PARAMETER		OPP100		OPP50		UNIT
			MIN	MAX	MIN	MAX	
GNF5	$t_{d(nWEIV-CLEIV)}$	Delay time, gpmc_nwe invalid to gpmc_nbe0_cle invalid	F(6) – 0.2	F(6) + 2.0	F(6) – 0.2	F(6) + 3.7	ns
GNF6	$t_{d(nWEIV-nCSIV)}$	Delay time, gpmc_nwe invalid to gpmc_ncsx invalid	G(7) – 0.2	G(7) + 2.0	G(7) – 0.2	G(7) + 3.7	ns
GNF7	$t_{d(ALEH-nWEV)}$	Delay time, gpmc_nadv_ale high to gpmc_nwe valid	C(3) – 0.2	C(3) + 2.0	C(3) – 0.2	C(3) + 3.7	ns
GNF8	$t_{d(nWEIV-ALEIV)}$	Delay time, gpmc_nwe invalid to gpmc_nadv_ale invalid	F(6) – 0.2	F(6) + 2.0	F(6) – 0.2	F(6) + 3.7	ns
GNF9	$t_{c(nWE)}$	Cycle time, Write cycle time	H(8)		H(8)		ns
GNF10	$t_{d(nCSV-nOEV)}$	Delay time, gpmc_ncsx valid to gpmc_noe valid	I(9) – 0.2	I(9) + 2.0	I(9) – 0.2	I(9) + 3.7	ns
GNF13	$t_{w(nOEV)}$	Pulse duration, gpmc_noe valid time	K(11)		K(11)		ns
GNF14	$t_{c(nOE)}$	Cycle time, read cycle time	L(12)		L(12)		ns
GNF15	$t_{d(nOEIV-nCSIV)}$	Delay time, gpmc_noe invalid to gpmc_ncsx invalid	M(13) – 0.2	M(13) + 2.0	M(13) – 0.2	M(13) + 3.7	ns

(1) A = (WEOffTime – WEOnTime) * (TimeParaGranularity + 1) * GPMC_FCLK
(2) B = ((WEOnTime – CSOnTime) * (TimeParaGranularity + 1) + 0.5 * (WEExtraDelay – CSExtraDelay)) * GPMC_FCLK
(3) C = ((WEOnTime – ADVOnTime) * (TimeParaGranularity + 1) + 0.5 * (WEExtraDelay – ADVExtraDelay)) * GPMC_FCLK
(4) D = (WEOnTime * (TimeParaGranularity + 1) + 0.5 * WEExtraDelay) * GPMC_FCLK
(5) E = ((WrCycleTime – WEOffTime) * (TimeParaGranularity + 1) – 0.5 * WEExtraDelay) * GPMC_FCLK
(6) F = ((ADVWrOffTime – WEOffTime) * (TimeParaGranularity + 1) + 0.5 * (ADVExtraDelay – WEExtraDelay)) * GPMC_FCLK
(7) G = ((CSWrOffTime – WEOffTime) * (TimeParaGranularity + 1) + 0.5 * (CSExtraDelay – WEExtraDelay)) * GPMC_FCLK
(8) H = WrCycleTime * (1 + TimeParaGranularity) * GPMC_FCLK
(9) I = ((OEOnTime – CSOnTime) * (TimeParaGranularity + 1) + 0.5 * (OEExtraDelay – CSExtraDelay)) * GPMC_FCLK
(10) J = AccessTime * (TimeParaGranularity + 1)
(11) K = (OEOffTime – OEOnTime) * (1 + TimeParaGranularity) * GPMC_FCLK
(12) L = RdCycleTime * (1 + TimeParaGranularity) * GPMC_FCLK
(13) M = ((CSRdOffTime – OEOffTime) * (TimeParaGranularity + 1) + 0.5 * (CSExtraDelay – OEExtraDelay))* GPMC_FCLK
(14) In gpmc_ncsx, x is equal to 0, 1, 2, 3, 4, 5, 6, or 7.

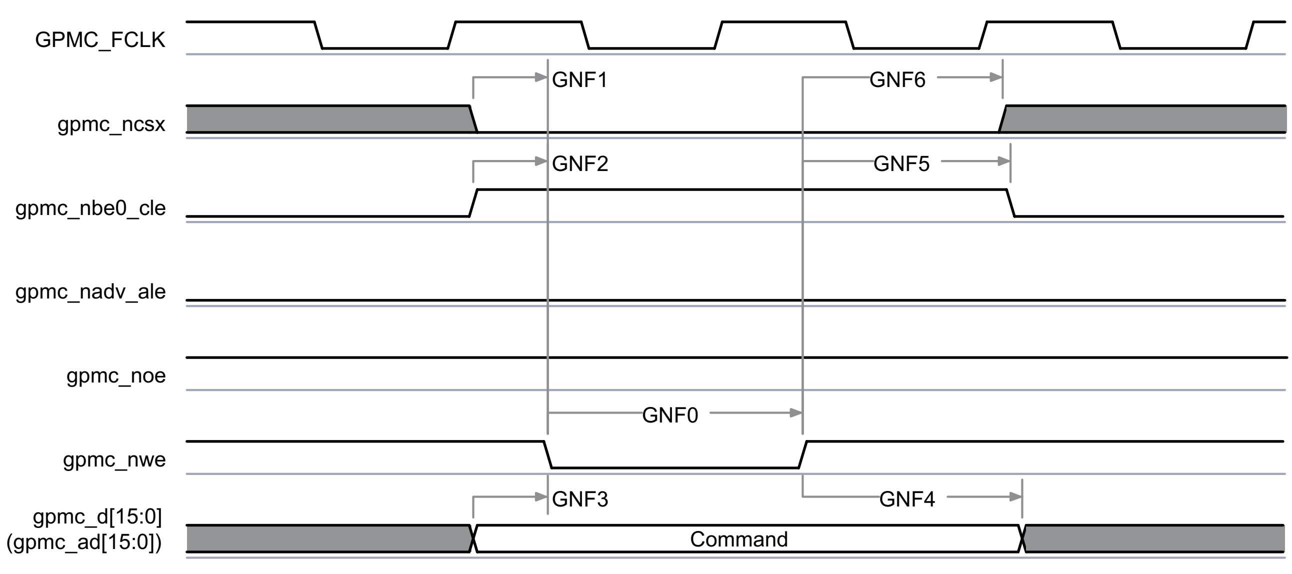

Figure 6-18. GPMC / NAND Flash—Asynchronous Mode—Command Latch Cycle Timing(1)

(1) In gpmc_ncsx, x is equal to 0, 1, 2, 3, 4, 5, 6, or 7.

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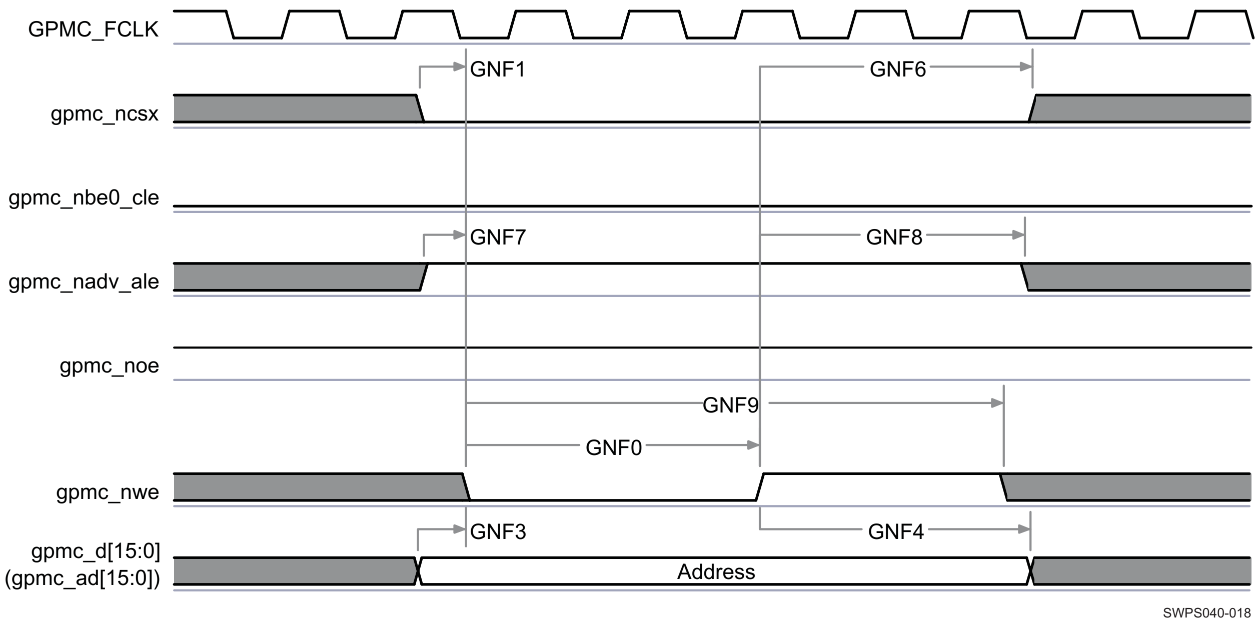

Figure 6-19. GPMC / NAND Flash—Asynchronous Mode—Address Latch Cycle Timing[(1)]

(1) In gpmc_ncsx, x is equal to 0, 1, 2, 3, 4, 5, 6, or 7.

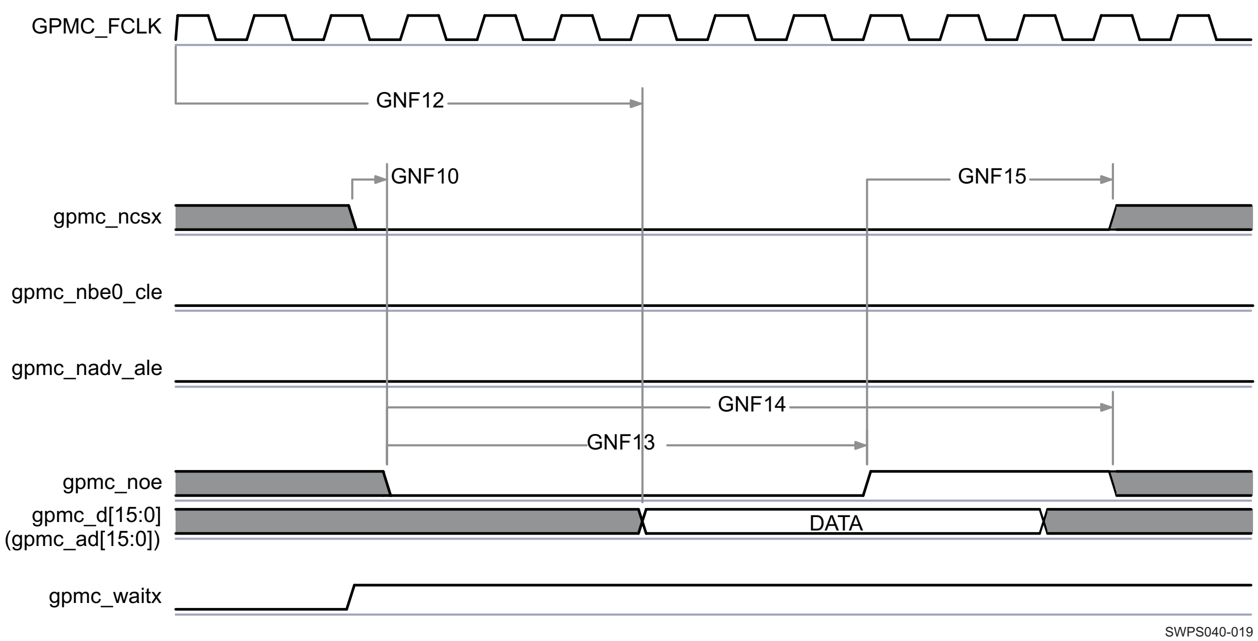

Figure 6-20. GPMC / NAND Flash—Asynchronous Mode—Data Read Cycle Timing[(1)(2)(3)]

(1) GNF12 parameter illustrates amount of time required to internally sample input Data. It is expressed in number of GPMC functional clock cycles. From start of read cycle and after GNF12 functional clock cycles, input data will be internally sampled by active functional clock edge. GNF12 value must be stored inside AccessTime register bits field.

(2) GPMC_FCLK is an internal clock (GPMC functional clock) not provided externally.

(3) In gpmc_ncsx, x is equal to 0, 1, 2, 3, 4, 5, 6, or 7. In gpmc_waitx, x is equal to 0, 1, or 2.

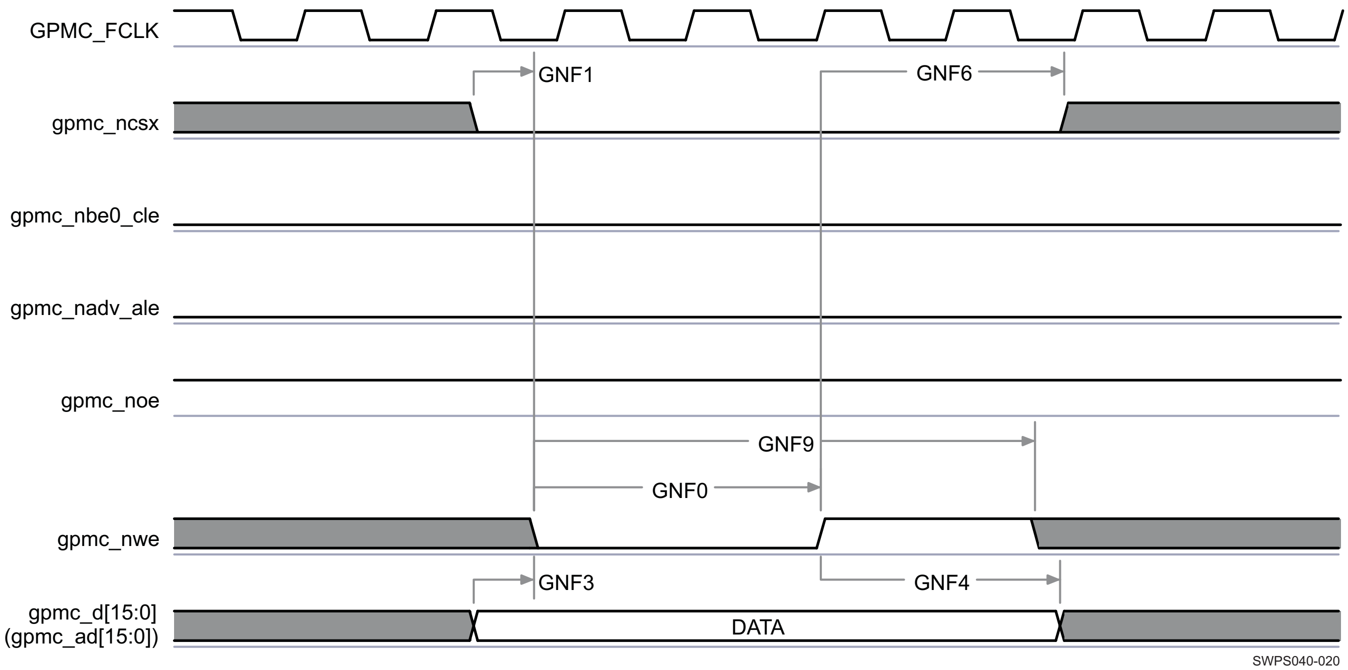

Figure 6-21. GPMC / NAND Flash—Asynchronous Mode—Data Write Cycle Timing[(1)]

(1) In gpmc_ncsx, x is equal to 0, 1, 2, 3, 4, 5, 6, or 7.

6.4.2 External Memory Interface (EMIF)

NOTE

For more information, see the EMIF Controller section of the OMAP4430 TRM.

The SDRAM controller subsystem module provides connectivity between the processor and external DRAM memory components. The module includes support for double-data-rate SDRAM (mobile DDR).

6.4.2.1 EMIF—DDR Mode

Table 6-17 and Table 6-18 assume testing over the recommended operating conditions and electrical characteristic conditions below (see Figure 6-22 through Figure 6-43). For timing parameters correspondence with JEDEC standard, see Table 6-19 and Table 6-20.

Table 6-16. EMIF Timing Conditions—DDR Mode

TIMING CONDITION PARAMETER		VALUE		UNIT
		MIN	MAX	
Input Conditions				
t_R	Input rise time		0.4	ns
t_F	Input fall time		0.4	ns
Output Condition				
C_{LOAD}	Output load capacitance[(1)]	2	5	pF

(1) IO settings: sr[1:0] = 11.
For more information, see the Control Module / Control Module Functional Description/ Functional Register Description / Signal Integrity Parameter Control Registers with Pad Group Assignment / High-speed I/O Buffers with Impedance, Slew Rate and Weak Driver Settings section of the OMAP4430 TRM.

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Table 6-17. EMIF Timing Requirements—DDR Mode[(3)(4)]

NO.	PARAMETER		OPP100		OPP50		UNIT
			MIN	MAX	MIN	MAX	
DQ/DM/DQS Read Parameters							
	$t_{dc(DQSI)}$	Duty cycle error, input clock lpddr2_ndqsX[(1)]	–125	125	–125	125	ps
	$t_{j(DQSI)}$	Jitter standard deviation, input clock lpddr2_ndqsX[(1)]	0	0	0	0	ps
DD300	$t_{c(DQSI)}$	Cycle time, lpddr2_dqsX[(1)] and lpddr2_ndqsX[(1)]	2.5		5		ns
DD301	$t_{w(DQSIH)}$	Pulse duration, lpddr2_dqsX[(1)] and lpddr2_ndqsX[(1)] high duration	0.5	0.5	0.5	0.5	DD100
DD301	$t_{w(DQSIL)}$	Pulse duration, lpddr2_dqsX[(1)] and lpddr2_ndqsX[(1)] low duration	0.5	0.5	0.5	0.5	DD100
DD302	$t_{sk(DQSI-NDQSI)}$	Skew , lpddr2_dqsX[(1)] edge to opposite lpddr2_ndqsX[(1)] edge	–67	67	–67	67	ps
DD303	$t_{d(DV-DQSI)}$	Delay time, lpddr2_dqsX[(1)] input transition after lpddr2_ck output transition	2.2	6.0	2.1	6.1	ns
DD304	$t_{su(DV-DQSI)}$	Setup time, lpddr2_dqY data valid before lpddr2_dqsX[(1)] reading transition	–0.28		–0.28		ns
DD305	$t_{h(DQSI-DIV)}$	Hold time, lpddr2_dqY data valid after lpddr2_dqsX[(1)] reading transition	0.42 * DD100 – 0.32		0.42 * DD100 – 0.32		ns
DD306	$t_{d(DQSIHZ-DQSILZ)}$	Delay time, lpddr2_dqsX[(1)] low impedance before lpddr2_dqsX[(1)] first transition	0.9		0.9		DD100
DD307	$t_{d(DQSILZ-DQSIHZ)}$	Delay time, lpddr2_dqsX[(1)] high impedance after lpddr2_dqsX[(1)] last transition		0.45		0.45	DD100
DD308	$t_{d(DQSILZ-CLKH)}$	Delay time, lpddr2_dqsX[(1)] driven after lpddr2_ck transition	2.20		2.20		ns
DD309	$t_{d(DQILZ-CLKH)}$	Delay time, lpddr2_dqY driven after lpddr2_ck transition	2.11		1.87		ns
DD310	$t_{d(clkH-DQSIHZ)}$	Delay time, lpddr2_dqsX[(1)] high impedance after lpddr2_ck transition		5.25		5.25	ns
DD311	$t_{d(clkH-DQIHZ)}$	Delay time, lpddr2_dqY high impedance after lpddr2_ck transition		5.68		5.91	ns
DQ/DM/DQS Boot Read Parameters							
DD303b	$t_{db(DV-DQSI)}$	Delay time, lpddr2_dqsX[(1)] input transition after lpddr2_ck output transition	2.2	6.0	2.1	6.1	ns
DD304b	$t_{sub(DV-DQSI)}$	Setup time, lpddr2_dqY data valid before lpddr2_dqsX[(1)] reading transition	–0.28		–0.28		ns
DD305b	$t_{hb(DQSI-DIV)}$	Hold time, lpddr2_dqY data valid after lpddr2_dqsX[(1)] reading transition	0.42 * DD100 – 0.32		0.42 * DD100 – 0.32		ns

(1) X = [3:0]

(2) Y = [31:0]

(3) In this table, LPDDR2 means LPDDR21 and LPDDR22. For more information, see Table 2-4.

(4) See DM Operating Condition Addendum for CORE OPP voltages.

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Table 6-18. EMIF Switching Characteristics—DDR Mode[(5)(6)]

NO.	PARAMETER		OPP100 MIN	OPP100 MAX	OPP50 MIN	OPP50 MAX	UNIT
Output Clocks Parameters							
	$t_{dc(clk)}$	Duty cycle error, output clock lpddr2_ck and lpddr2_nck	–31	31	–63	63	ps
	$t_{j(clk)}$	Jitter standard deviation, output clock lpddr2_ck and lpddr2_nck	–63	63	–125	125	ps
	$t_{dc(DQS)}$	Duty cycle error, output clock lpddr2_dqsX[(1)] and lpddr2_ndqsX[(1)]	–31	31	–63	63	ps
	$t_{j(DQS)}$	Jitter standard deviation, output clock lpddr2_dqsX[(1)] and lpddr2_ndqsX[(1)]	–63	63	–125	125	ps
	$t_{R(O)}$	Output signal rise time		400		400	ps
	$t_{F(O)}$	Output signal fall time		400		400	ps
DD100	$t_{c(clk)}$	Cycle time, lpddr2_ck and lpddr2_nck	2.5		5		ns
DD101	$t_{w(clkH)}$	Typical pulse duration, lpddr2_ck and lpddr2_nck high duration	0.5	0.5	0.5	0.5	DD100
DD101	$t_{w(clkL)}$	Typical pulse duration, lpddr2_ck and lpddr2_nck low duration	0.5	0.5	0.5	0.5	DD100
DD102	$t_{sk(clk-Nclk)}$	Skew, lpddr2_ck edge to opposite lpddr2_nck edge	–67	67	–67	67	ps
CKE and Command Address Write Parameters							
DD200	$t_{w(CKE)}$	Pulse duration, lpddr2_cke high and low duration	3 * DD100		3 * DD100		ns
DD201	$t_{d(clkL-CKE)}$	Delay time, lpddr2_ck low to lpddr2_cke	0.05	0.16 * DD100 – 0.05	0.05	0.16 * DD100 – 0.05	ns
DD202	$t_{d(clkL-NCS)}$	Delay time, lpddr2_ck low to lpddr2_ncs	0.34	0.41 * DD100 – 0.34	0.34	0.41 * DD100 – 0.34	ns
DD203	$t_{d(clk-CA)}$	Delay time, lpddr2_ck low to lpddr2_caZ[(3)]	0.05 * DD100 + 0.34	0.45 * DD100 – 0.34	0.05 * DD100 + 0.34	0.45 * DD100 – 0.34	ns
DD204	$t_{w(CA)}$	Pulse duration, lpddr2_caZ[(3)] high and low duration	0.50		0.50		DD100
CKE and Command Boot Write Parameters							
DD200b	$t_{cb(clk)}$	Cycle time, lpddr2_ck and lpddr2_nck	2.5		5		ns
DD201b	$t_{db(clkL-CKE)}$	Delay time, lpddr2_ck low to lpddr2_cke	0.05	0.16 * DD100 – 0.05	0.05	0.16 * DD100 – 0.05	ns
DD202b	$t_{db(clkL-NCS)}$	Delay time, lpddr2_ck low to lpddr2_ncs	0.34	0.41 * DD100 – 0.34	0.34	0.41 * DD100 – 0.34	ns
DD203b	$t_{db(clk-CA)}$	Delay time, lpddr2_ck low to lpddr2_caZ[(3)]	0.05 * DD100 + 0.34	0.45 * DD100 – 0.34	0.05 * DD100 + 0.34	0.45 * DD100 – 0.34	ns
DQ/DM/DQS Write Parameters							
DD400	$t_{c(DQSO)}$	Cycle time, lpddr2_dqsX[(1)] and lpddr2_ndqsX[(1)]	2.5		5		ns
DD401	$t_{w(DQSOH)}$	Pulse duration, lpddr2_dqsX[(1)] and lpddr2_ndqsX[(1)] high duration	0.5	0.5	0.5	0.5	DD400
DD401	$t_{w(DQSOL)}$	Pulse duration, lpddr2_dqsX[(1)] and lpddr2_ndqsX[(1)] low duration	0.5	0.5	0.5	0.5	DD400
DD402	$t_{sk(DQSO-NDQSO)}$	Skew , lpddr2_dqsX[(1)] edge to opposite lpddr2_ndqsX[(1)] edge	–67	67	–67	67	ps

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Table 6-18. EMIF Switching Characteristics—DDR Mode[(5)(6)] (continued)

NO.	PARAMETER		OPP100		OPP50		UNIT
			MIN	MAX	MIN	MAX	
DD403	$t_{d(DQSO-DQO/DM)}$	Delay time, lpddr2_dqsX[(1)] to lpddr2_dqY[(2)] and lpddr2_dmX[(1)]	0.05 * DD100 + 0.32	0.45 * DD100 – 0.32	0.05 * DD100 + 0.32	0.45 * DD100 – 0.32	ns
DD404	$t_{d(DV-DQSO)}$	Delay time, lpddr2_dqsX[(1)] valid after lpddr2_ck transition	0.09	0.19 * DD100 – 0.09	0.09	0.19 * DD100 – 0.09	ns
DD405	$t_{d(clkV-DQSO)}$	Delay time, lpddr2_ck valid to first lpddr2_dqsX[(1)] edge	0.75	1.25	0.75	1.25	ns
DD406	$t_{d(DQSOHZ-DQSOV)}$	Delay time, lpddr2_dqsX[(1)] high impedance to lpddr2_dqsX[(1)] valid	0.35		0.35		DD100
DD407	$t_{d(DQSOV-DQSOHZ)}$	Delay time, lpddr2_dqsX[(1)] last edge to lpddr2_dqsX[(1)] high impedance state	0.4		0.4		DD100
DD408	$t_{w(DQO/DM)}$	Pulse duration, lpddr2_dqY[(2)] and lpddr2_dmX[(1)] high/low duration	0.5		0.5		DD100
SDRAM Core Parameters							
DD500	$t_{c(ACT-ACT)s}$	Cycle time, ACTIVE to ACTIVE command	DD508 + DD509		DD508 + DD509		ns
DD501	$t_{w(SRL)s}$	Pulse duration, lpddr2_cke during SELF REFRESH low duration	15		15		ns
DD502	$t_{c(SR-VAL)s}$	Cycle time, SELF REFRESH to VALID command	DD514 + 10		DD514 + 10		ns
DD503	$t_{d(DPWDN)s}$	Delay time, POWER DOWN exit time	7.5		10		ns
DD504	$t_{d(PWDN)s}$	Delay time, DEEP POWER DOWN command	500		500		µs
DD505	$t_{c(RD-RD)s}$	Cycle time, READ to READ command	2		2		DD100
DD506	$t_{c(RD-PRE)s}$	Cycle time, READ to PRECHARGE command	7.5		10		ns
DD507	$t_{c(ACT-RD)s}$	Cycle time, ACTIVE to READ command	18		18		ns
DD508	$t_{d(PRE)s}$	Delay time, PRECHARGE command (8-bank)	18		18		ns
DD509	$t_{c(ACT-PRE)s}$	Cycle time, ACTIVE to PRECHARGE command	42	70000	42	70000	ns
DD510	$t_{d(WRREC)s}$	Delay time, WRITE recovery time	15		15		ns
DD511	$t_{c(WR-RD)s}$	Cycle time, WRITE to READ command	7.5		10		ns
DD512	$t_{c(ACTBA-ACTBB)s}$	Cycle time, ACTIVE bank A to ACTIVE bank B command	10		10		ns
DD513	$t_{c(ACT-4B-ACT)s}$	Cycle time, Four banks ACTIVE to ACTIVE command	50		50		ns
DD514	$t_{c(REF)s}$	Cycle time, Four banks REFRESH Command	A[(4)]		A[(4)]		ns
NVM Core Parameters							
DD601	$t_{c(ACT-RD/WR)n}$	Cycle time, ACTIVE to READ or WRITE command	15	255	25	255	ns
DD602	$t_{c(ACTBA-ACTBB)n}$	Cycle time, ACTIVE bank A to ACTIVE bank B command	DD601		DD601		ns
DD603	$t_{c(ACT-ACT)n}$	Cycle time, ACTIVE to ACTIVE command	DD601		DD601		ns
DD604	$t_{c(CAS-CAS)n}$	Cycle time, CAS to CAS command	2		2		DD100
DD605	$t_{c(WRREC-ACT)n}$	Cycle time, WRITE recovery Time before ACTIVE	15		15		ns
DD606	$t_{c(WR-RD)n}$	Cycle time, WRITE to READ command	7.5		10		ns
DD607	$t_{c(PRE-ACT)n}$	Cycle time, PRECHARGE to ACTIVE command	3		3		DD100

Table 6-18. EMIF Switching Characteristics—DDR Mode(5)(6) (continued)

NO.	PARAMETER		OPP100		OPP50		UNIT
			MIN	MAX	MIN	MAX	
DD608	$t_{c(ACT-PRE)n}$	Cycle time, ACTIVE to PREACTIVE command	DD601		DD601		ns
DD609	$t_{c(EXPWDN-VAL)n}$	Cycle time, EXIT POWER DOWN to next Valid command	10		20		ns
Mode Register Parameters							
DD700	$t_{d(MRW)}$	Delay time, MODE REGISTER WRITE command	5		5		DD100
DD701	$t_{d(MRR)}$	Delay time, MODE REGISTER READ command	2		2		DD100
ZQ Calibration Parameters							
DD800	$t_{d(QINIT)}$	Delay time, Initialization Calibration command		1		1	µs
DD801	$t_{d(QCL)}$	Delay time, Long Calibration command		360		360	ns
DD802	$t_{d(QCS)}$	Delay time, Short Calibration command		90		90	ns
DD803	$t_{d(QRESET)}$	Delay time, Calibration Reset command		50		50	ns

(1) X = [3:0]

(2) Y = [31:0]

(3) Z = [9:0]

(4) Per device density:

- In the range [64 Mbits to 512 Mbits], density = 90 ns
- In the range [1 Gbit to 4 Gbits], density = 130 ns
- For 8 Gbits, density = 210 ns

(5) In this table, LPDDR2 means LPDDR21 and LPDDR22. For more information, see Table 2-4.

(6) See DM Operating Condition Addendum for CORE OPP voltages.

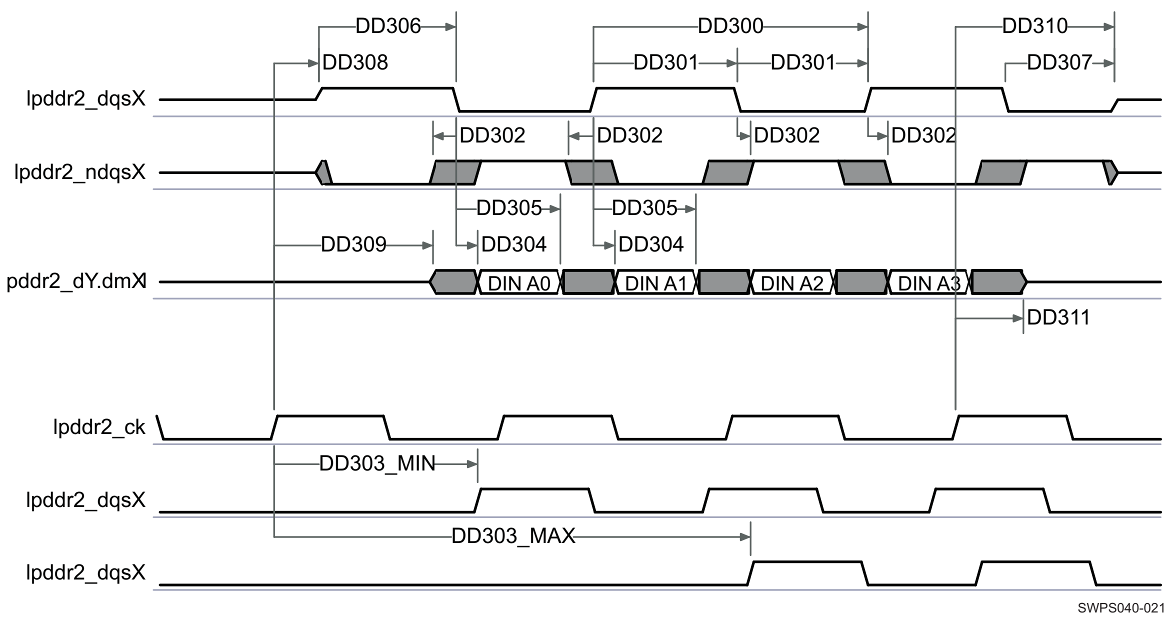

Figure 6-22. EMIF—DDR Mode—DQ / DM / DQS Read Parameters(1)(2)

(1) X = [3:0]

(2) Y = [31:0]

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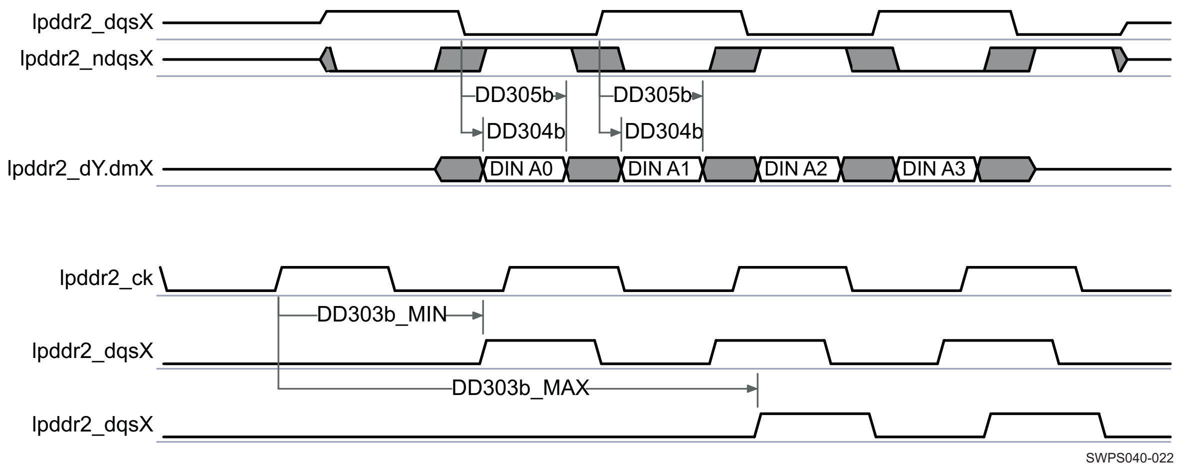

Figure 6-23. EMIF—DDR Mode—DQ / DM / DQS Boot Read Parameters(1)(2)

(1) X = [3:0]

(2) Y = [31:0]

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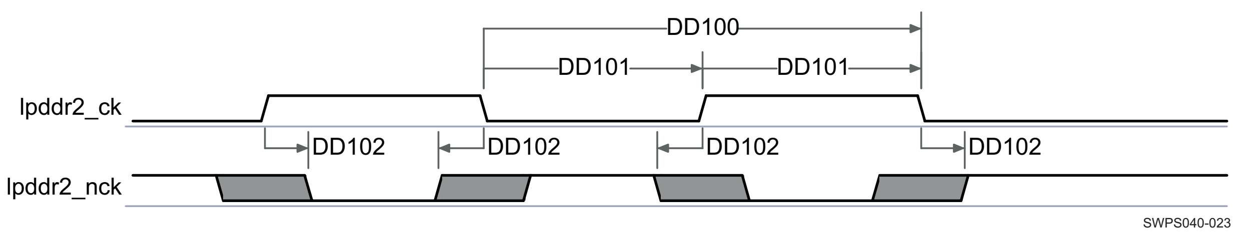

Figure 6-24. EMIF—DDR Mode—Output Clock Parameters

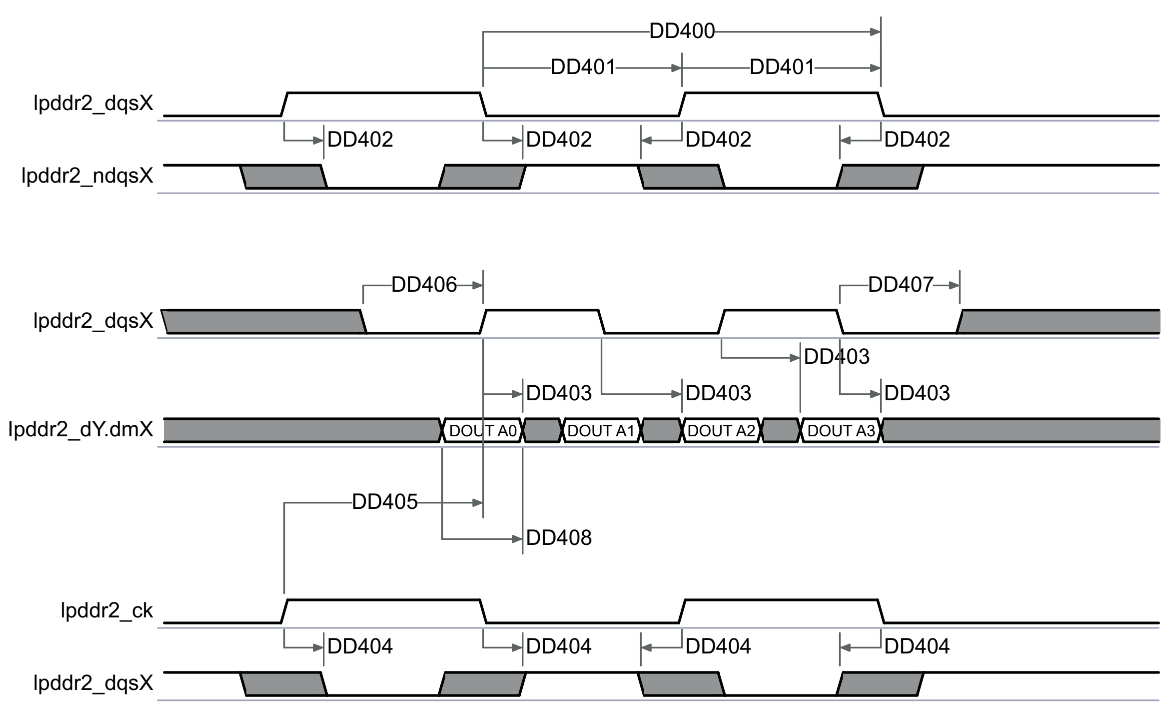

Figure 6-25. EMIF—DDR Mode—DQ / DM / DQS Write Parameters(1)(2)

(1) X = [3:0]

(2) Y = [31:0]

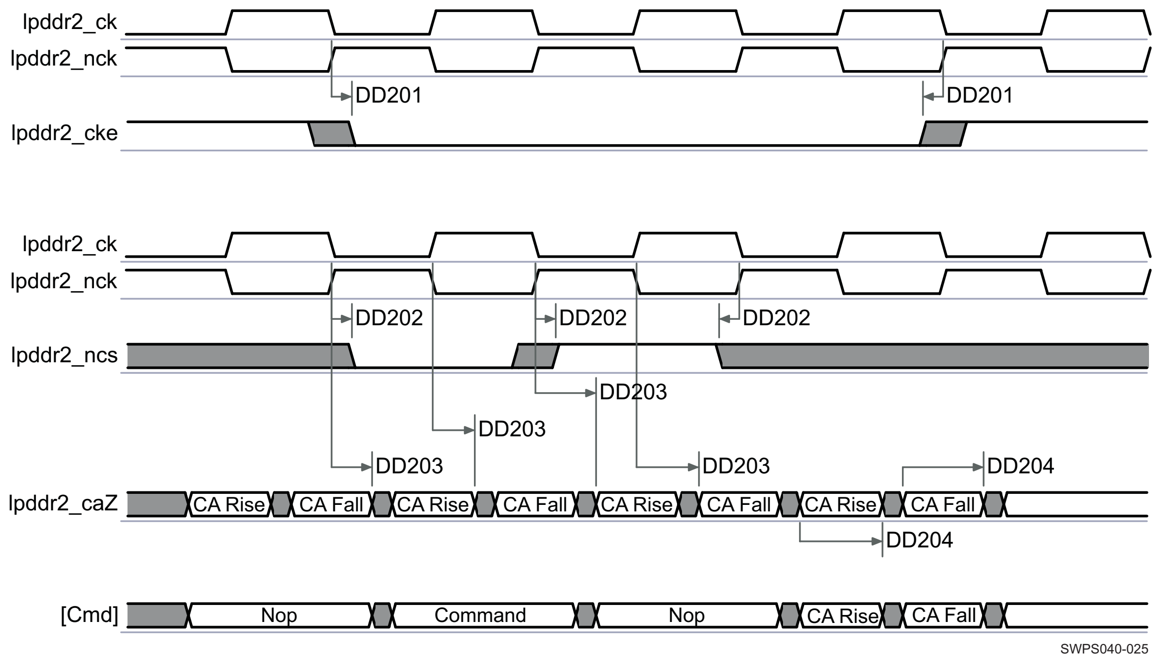

Figure 6-26. EMIF—DDR Mode—CKE and Command Address Write Parameters[(1)]

(1) Z = [9:0]

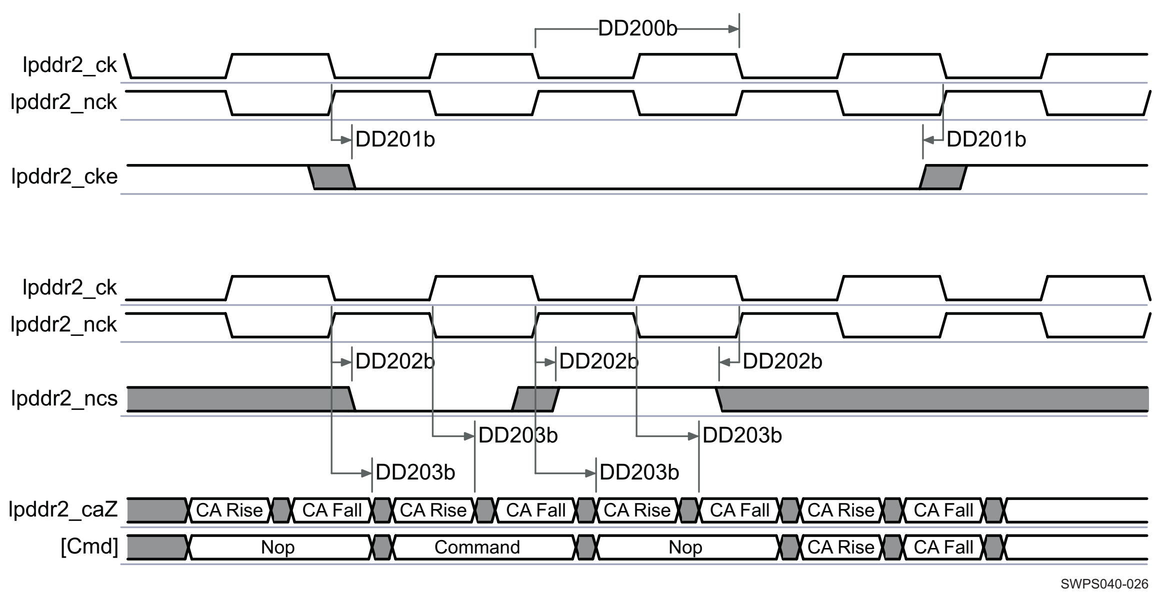

Figure 6-27. EMIF—DDR Mode—CKE and Command Boot Write Parameters[(1)]

(1) Z = [9:0]

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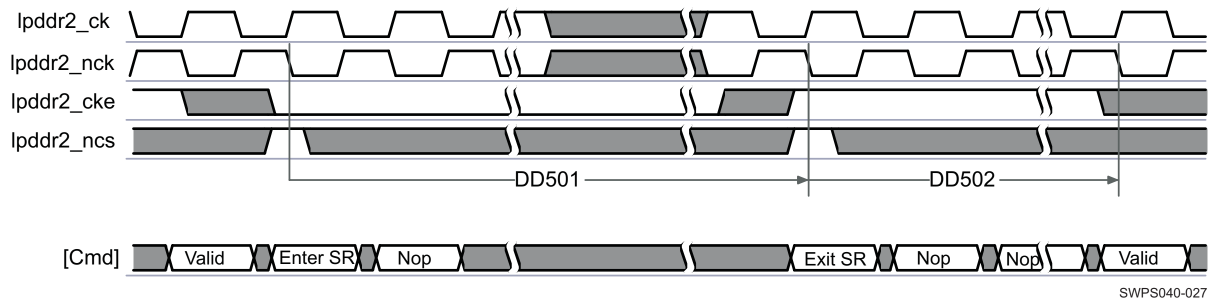

Figure 6-28. EMIF—DDR Mode—SDRAM Core Parameters—Self-Refresh Command(1)(2)(3)

(1) X = [3:0]

(2) Y = [31:0]

(3) Z = [9:0]

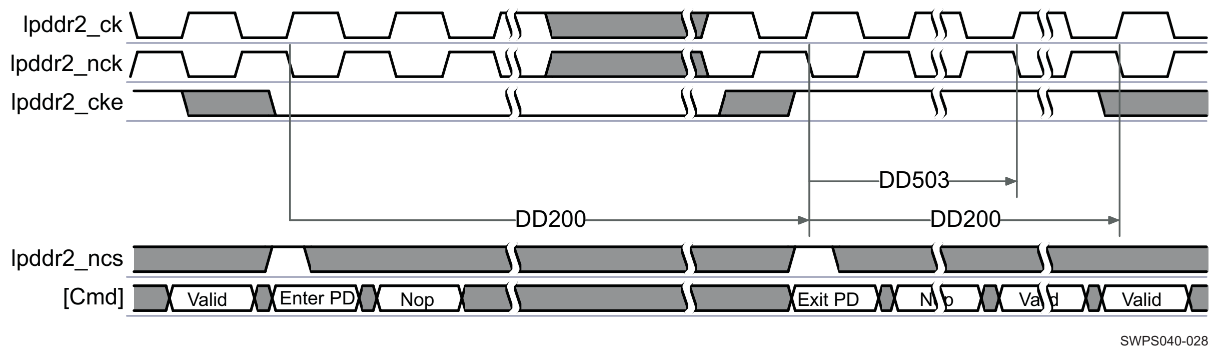

Figure 6-29. EMIF—DDR Mode—SDRAM Core Parameters—Power-Down Exit Time Command(1)(2)

(1) X = [3:0]

(2) Y = [31:0]

(3) Z = [9:0]

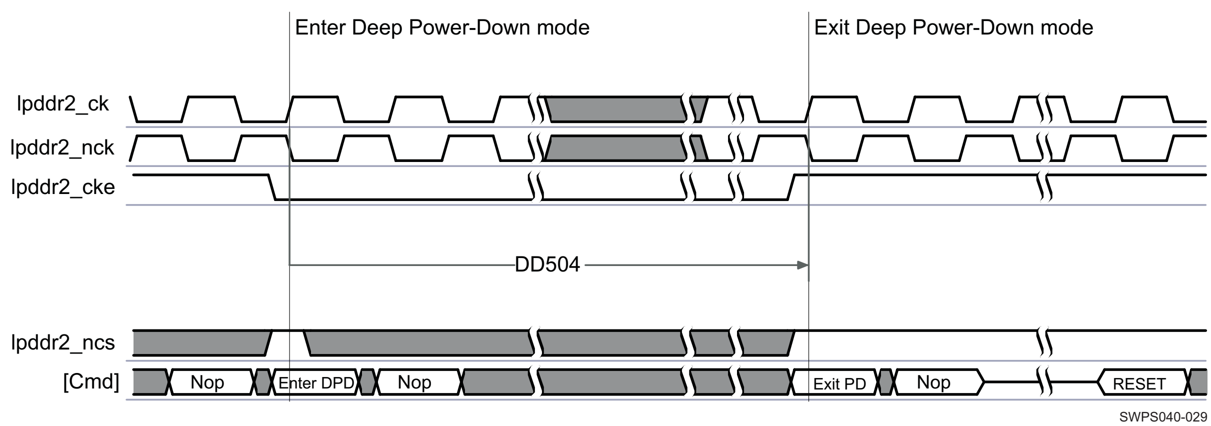

Figure 6-30. EMIF—DDR Mode—SDRAM Core Parameters—Deep Power-Down Command(1)(2)(3)

(1) X = [3:0]

(2) Y = [31:0]

(3) Z = [9:0]

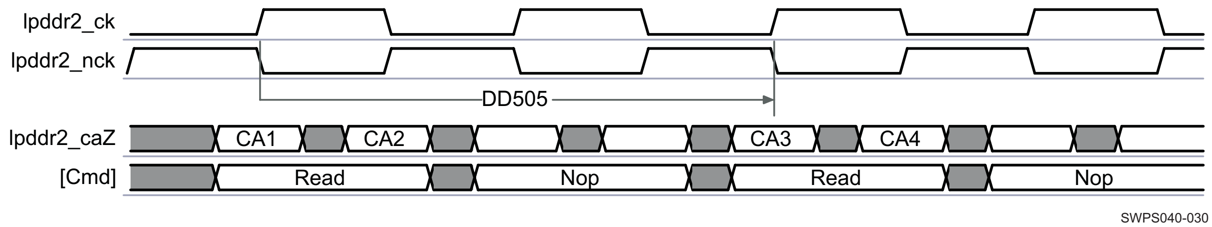

Figure 6-31. EMIF—DDR Mode—SDRAM Core Parameters—Read to Read Command(1)(2)(3)(4)(5)(6)(7)

(1) X = [3:0]
(2) Y = [31:0]
(3) Z = [9:0]
(4) CA1 = Bank N Column Address A
(5) CA2 = Column Address A
(6) CA3 = Bank N Column Address B
(7) CA4 = Column Address B

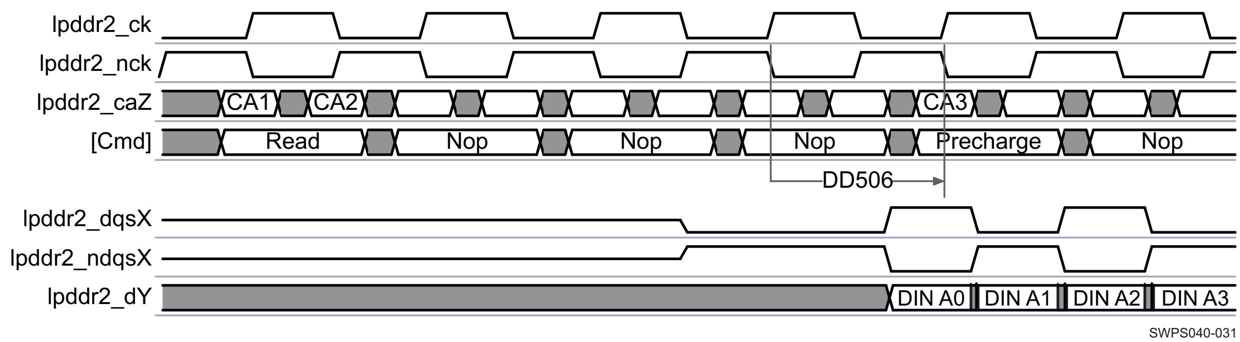

Figure 6-32. EMIF—DDR Mode—SDRAM Core Parameters—Read to Precharge(1)(2)(3)(4)(5)(6)

(1) X = [3:0]
(2) Y = [31:0]
(3) Z = [9:0]
(4) CA1 = Bank M Column Address A
(5) CA2 = Column Address A
(6) CA3 = Bank M

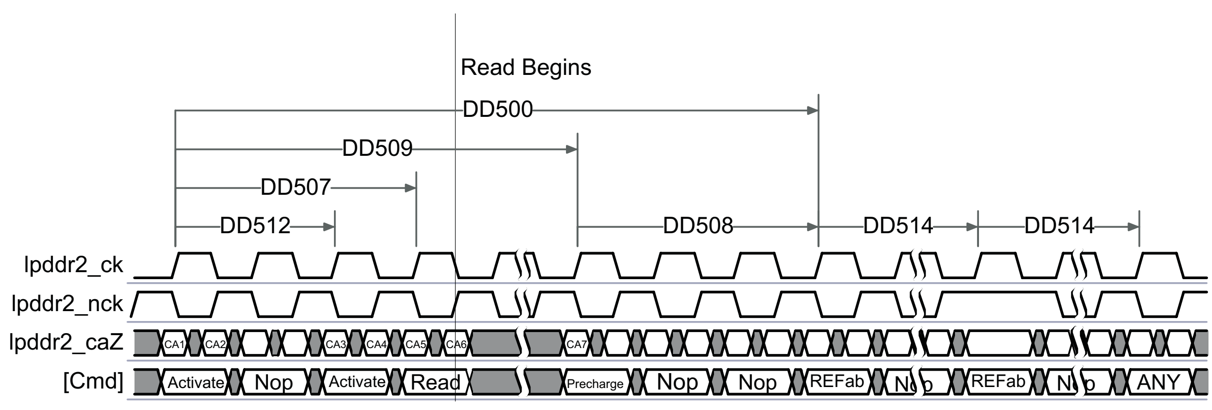

Figure 6-33. EMIF—DDR Mode—SDRAM Core Parameters—Active to Read, Precharge, Active to Precharge, Write, Write to Read, Active Bank A to Active Bank B Commands(1)(2)(3)(4)(5)(6)(7)(8)(9)(10)

(1) X = [3:0]

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(2) Y = [31:0]
(3) Z = [9:0]
(4) CA1 = Bank A Row Address
(5) CA2 = Row Address
(6) CA3 = Bank B Row Address
(7) CA4 = Row Address
(8) CA5 = Bank A Column Address
(9) CA6 = Column Address
(10) CA7 = Bank A

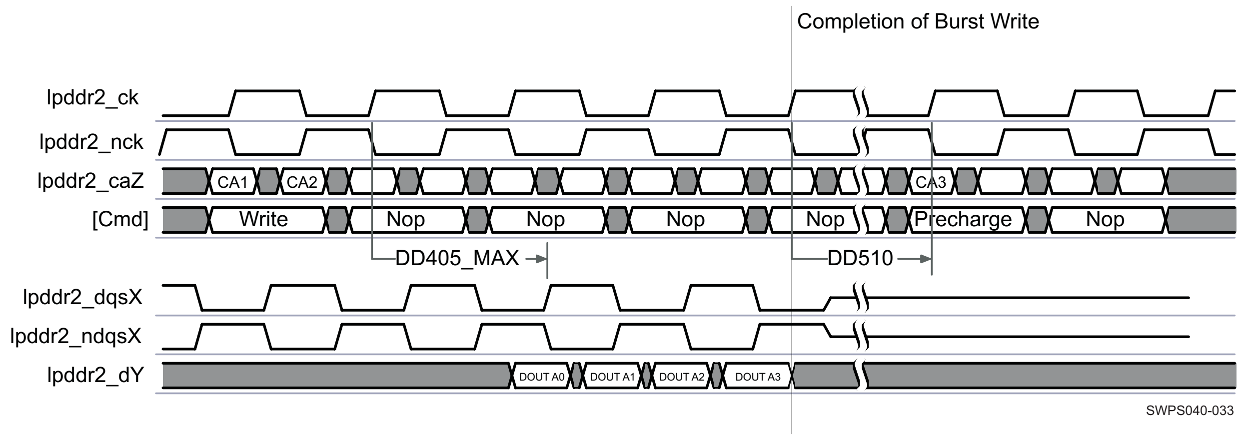

Figure 6-34. EMIF—DDR Mode—SDRAM Core Parameters—Write Recovery Time(1)(2)(3)(4)(5)(6)

(1) X = [3:0]
(2) Y = [31:0]
(3) Z = [9:0]
(4) CA1 = Bank A Column Address A
(5) CA2 = Column Address
(6) CA3 = Bank A

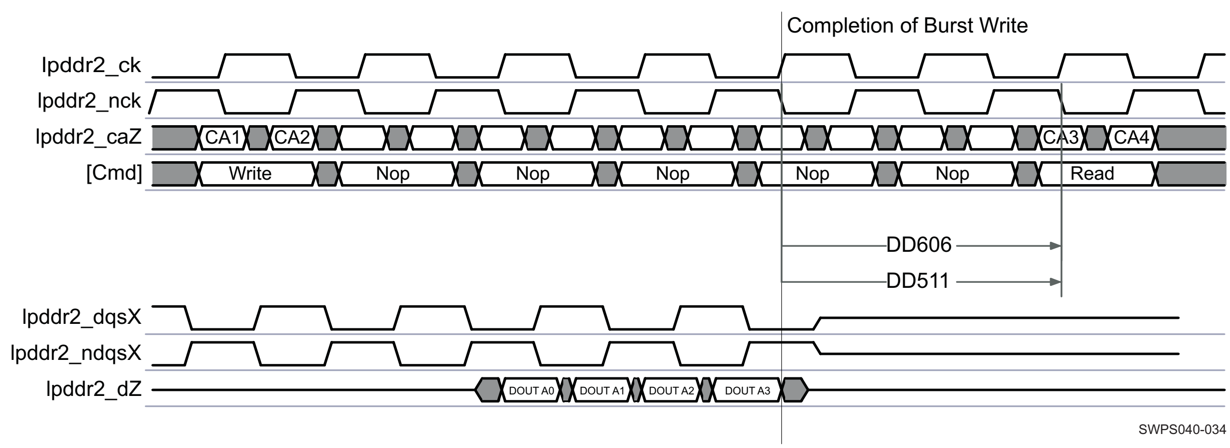

Figure 6-35. EMIF—DDR Mode—SDRAM Core Parameters—Write to Read Command(1)(2)(3)(4)(5)(6)(7)(8)(9)(10)(11)

(1) X = [3:0]
(2) Y = [31:0]
(3) Z = [9:0]
(4) CA1[SDRAM DD511] = Bank M Column Address A
(5) CA2[SDRAM DD511] = Column Address A

(6) CA3[SDRAM DD511] = Bank N Column Address B
(7) CA4[SDRAM DD511] = Column Address B
(8) CA1[NVM DD606] = RDB M Column Address A
(9) CA2[NVM DD606] = Column Address A
(10) CA3[NVM DD606] = RDB N Column Address B
(11) CA4[NVM DD606] = Column Address B

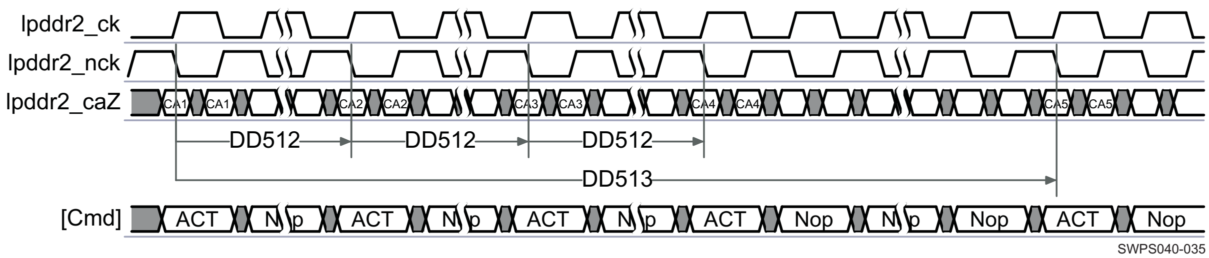

Figure 6-36. EMIF—DDR Mode—SDRAM Core Parameters—Active to Active Command(1)(2)(3)(4)(5)(6)(7)(8)

(1) X = [3:0]
(2) Y = [31:0]
(3) Z = [9:0]
(4) CA1 = Bank A
(5) CA2 = Bank B
(6) CA3 = Bank C
(7) CA4 = Bank D
(8) CA5 = Bank E

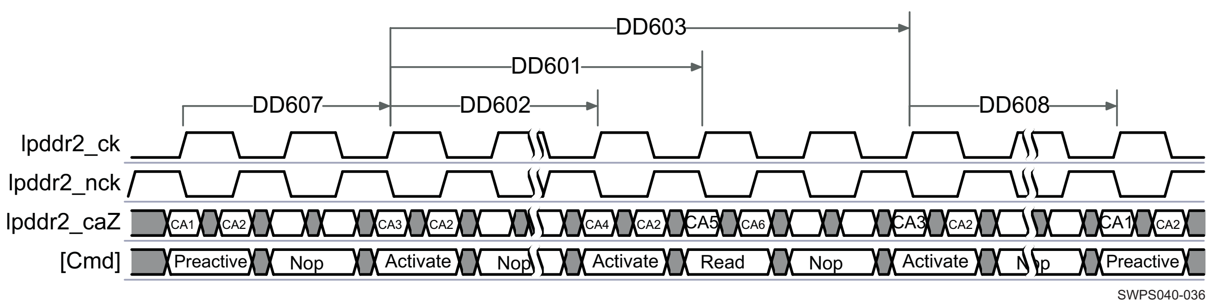

Figure 6-37. EMIF—DDR Mode—NVM Core Parameters—Active to Read or Write, Active Bank A to Active Bank B, Active to Active, Precharge to Active, Active to Preactive Commands(1)(2)(3)(4)(5)(6)(7)(8)(9)

(1) X = [3:0]
(2) Y = [31:0]
(3) Z = [9:0]
(4) CA1 = RAB A Row Address
(5) CA2 = Row Address
(6) CA3 = RB A Row Address
(7) CA4 = RB B Row Address
(8) CA5 = RDB A Column Address
(9) CA6 = Column Address

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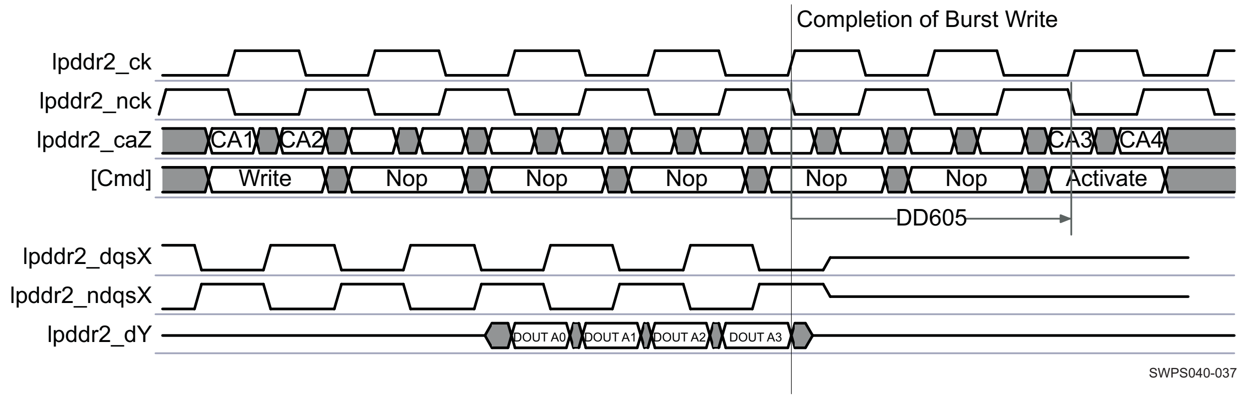

Figure 6-38. EMIF—DDR Mode—NVM Core Parameters—Write Recovery Time Before Active(1)(2)(3)(4)(5)(6)(7)

(1) X = [3:0]
(2) Y = [31:0]
(3) Z = [9:0]
(4) CA1 = RDB A Column Address
(5) CA2 = Column Address
(6) CA3 = RB A Row Address
(7) CA4 = Row Address

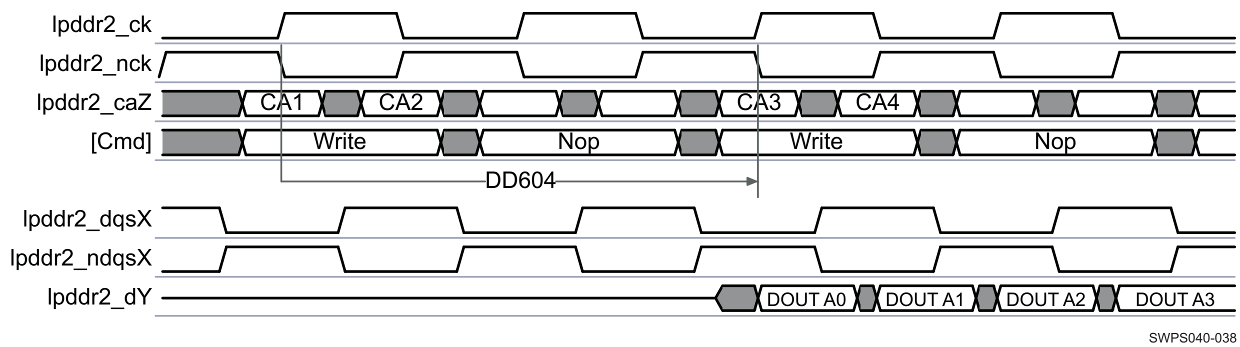

Figure 6-39. EMIF—DDR Mode—NVM Core Parameters—CAS to CAS(1)(2)(3)(4)(5)(6)(7)

(1) X = [3:0]
(2) Y = [31:0]
(3) Z = [9:0]
(4) CA1 = RDB M Column Address A
(5) CA2 = Column Address A
(6) CA3 = RDB N Column Address B
(7) CA4 = Column Address B

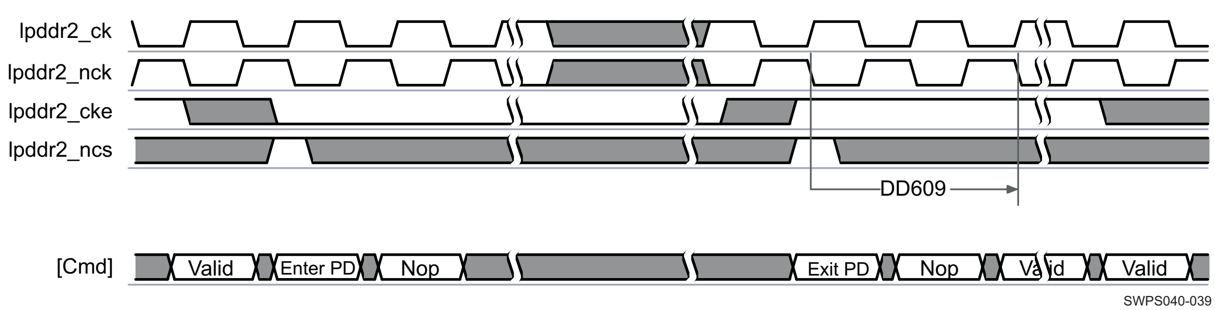

Figure 6-40. EMIF—DDR Mode—NVM Core Parameters—Exit Power-Down to Next Valid Command(1)(2)(3)

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(1) X = [3:0]

(2) Y = [31:0]

(3) Z = [9:0]

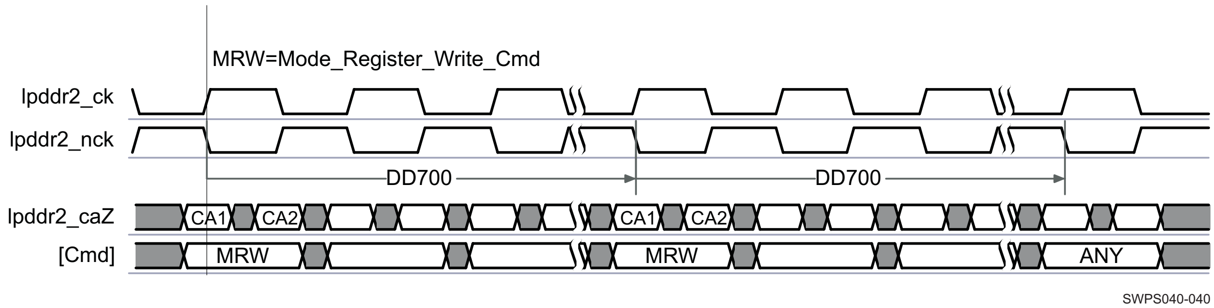

Figure 6-41. EMIF—DDR Mode—Mode Register Parameters—Write Command(1)(2)(3)

(1) Z = [9:0]

(2) CA1 = MR Address

(3) CA2 = MR Data

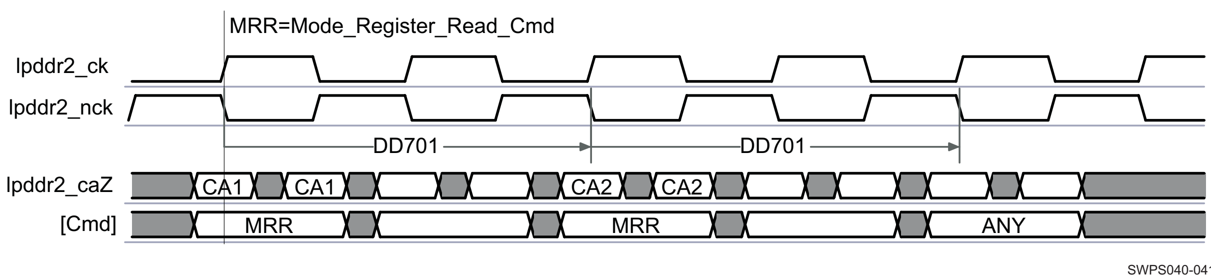

Figure 6-42. EMIF—DDR Mode—Mode Register Parameters—Read Command(1)(2)(3)

(1) Z = [9:0]

(2) CA1 = Register A

(3) CA2 = Register B

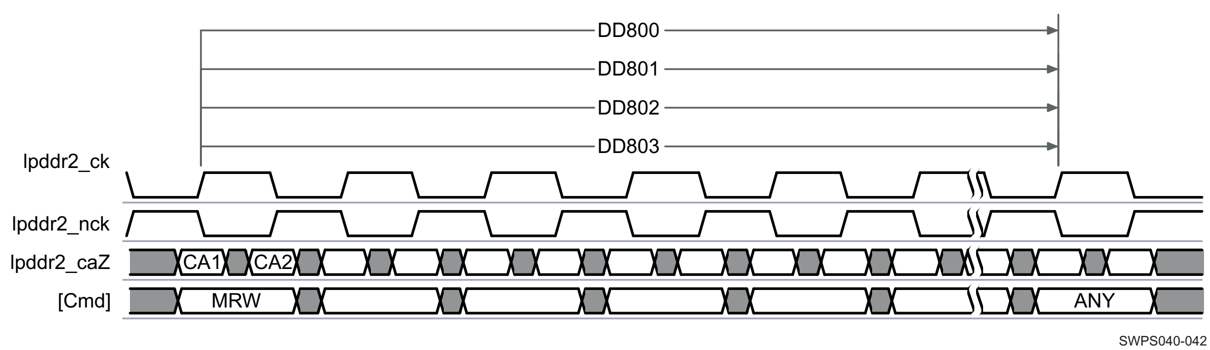

Figure 6-43. EMIF—DDR Mode—ZQ Calibration Parameters(1)(2)(3)

(1) Z = [9:0]

(2) CA1 = MR Address

(3) CA2 = MR Data

Table 6-19. LPDDR2 Timing Requirements Correspondence Between Data Manual and LPDDR2 JEDEC Standard—(JESD209-2A)[3]

TIMINGS PARAMETERS			JEDEC STANDARD PARAMETERS	
REF.	DESCRIPTION		REF.	DESCRIPTION
DD300	$t_{c(DQSI)}$	Cycle time, lpddr2_dqsx[1] and lpddr2_ndqsx[1]	$t_{CK(avg)}$	Average clock period
DD301	$t_{w(DQSIH)}$	Pulse duration, lpddr2_dqsx[1] and lpddr2_ndqsx[1] high duration	t_{QSH}	DQS output high pulse width
DD301	$t_{w(DQSIL)}$	Pulse duration, lpddr2_dqsx[1] and lpddr2_ndqsx[1] low duration	t_{QSL}	DQS output low pulse width
DD302	$t_{sk(DQSI-NDQSI)}$	Skew , lpddr2_dqsx[1] edge to opposite lpddr2_ndqsx[1] edge	V_{IX}	Crossing point differential skew
DD303	$t_{d(DV-DQSI)}$	Delay time, lpddr2_dqsx[1] input transition after lpddr2_ck output transition	t_{DQSCK}	DQS output access time from CK / nCK
DD304	$t_{su(DV-DQSI)}$	Setup time, lpddr2_dqy[2] data valid before lpddr2_dqsx[1] reading transition	t_{DQSQ}	DQS - DQ skew
DD305	$t_{h(DQSI-DIV)}$	Hold time, lpddr2_dqy[2] data valid after lpddr2_dqsx[1] reading transition	t_{QH} / t_{QHS}	DQ output hold time from DQS / Data hold skew factor
DD306	$t_{d(DQSIHZ-DQSILZ)}$	Delay time, lpddr2_dqsx[1] low impedance before lpddr2_dqsx[1] first transition	t_{RPRE}	Read preamble
DD307	$t_{d(DQSILZ-DQSIHZ)}$	Delay time, lpddr2_dqsx[1] high impedance after lpddr2_dqsx[1] last transition	t_{RPST}	Read postamble
DD308	$t_{d(DQSILZ-CLKH)}$	Delay time, lpddr2_dqsx[1] driven after lpddr2_ck transition	$t_{LZ(DQS)}$	DQS low-Z from clock
DD309	$t_{d(DQILZ-CLKH)}$	Delay time, lpddr2_dqy[2] driven after lpddr2_ck transition	$t_{LZ(DQ)}$	DQ low-Z from clock
DD310	$t_{d(clkH-DQSIHZ)}$	Delay time, lpddr2_dqsx[1] high impedance after lpddr2_ck transition	$t_{HZ(DQS)}$	DQS high-Z from clock
DD311	$t_{d(clkH-DQIHZ)}$	Delay time, lpddr2_dqy[2] high impedance after lpddr2_ck transition	$t_{HZ(DQ)}$	DQ high-Z from clock
DD303b	$t_{db(DV-DQSI)}$	Delay time, lpddr2_dqsx[1] input transition after lpddr2_ck output transition	t_{DQSCKb}	DQS output access time from CK / nCK
DD304b	$t_{sub(DV-DQSI)}$	Setup time, lpddr2_dqy[2] data valid before lpddr2_dqsx[1] reading transition	t_{DQSQb}	DQS - DQ skew
DD305b	$t_{hb(DQSI-DIV)}$	Hold time, lpddr2_dqy[2] data valid after lpddr2_dqsx[1] reading transition	t_{QHSb}	DQ output hold time from DQS / Data hold skew factor

(1) x = [3:0]

(2) y = [31:0]

(3) The timing correspondence in this table means that a system equation exists between the Data Manual parameters and the JEDEC ones.

Table 6-20. LPDDR2 Switching Characteristics Correspondence Between Data Manual and LPDDR2 JEDEC Standard—(JESD209-2A)[4]

TIMING PARAMETERS			JEDEC STANDARD PARAMETERS	
REF.	DESCRIPTION		REF.	DESCRIPTION
	$t_{dc(clk)}$	Duty cycle error, output clock lpddr2_ck and lpddr2_nck	$t_{JIT(duty)}$	Duty cycle jitter
	$t_{j(clk)}$	Jitter standard deviation, output clock lpddr2_ck and lpddr2_nck	$t_{JIT(per)}$	Clock period jitter
	$t_{dc(DQS)}$	Duty cycle error, output clock lpddr2_dqsx[1] and lpddr2_ndqsx[1]	$t_{JIT(duty)}$	Duty cycle jitter
	$t_{j(DQS)}$	Jitter standard deviation, output clock lpddr2_dqsx[1] and lpddr2_ndqsx[1]	$t_{JIT(per)}$	Clock period jitter
DD100	$t_{c(clk)}$	Cycle time, lpddr2_ck and lpddr2_nck	t_{CK}	Average clock period
DD101	$t_{w(clkH)}$	Typical pulse duration, lpddr2_ck and lpddr2_nck high duration	t_{CH}	Average high pulse width

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Table 6-20. LPDDR2 Switching Characteristics Correspondence Between Data Manual and LPDDR2 JEDEC Standard—(JESD209-2A)[(4)] (continued)

TIMING PARAMETERS			JEDEC STANDARD PARAMETERS	
REF.	DESCRIPTION		REF.	DESCRIPTION
DD101	$t_{w(clkL)}$	Typical pulse duration, lpddr2_ck and lpddr2_nck low duration	t_{CL}	Average low pulse width
DD102	$t_{sk(clk-Nclk)}$	Skew , lpddr2_ck edge to opposite lpddr2_nck edge	V_{IX}	Crossing point differential skew
DD200	$t_{w(CKE)}$	Pulse duration, lpddr2_cke high and low duration	t_{CKE}	CKE minimum pulse width (high and low pulse width)
DD201	$t_{d(clkL-CKE)}$	Delay time, lpddr2_ck low to lpddr2_cke	t_{IHCKE} / t_{ISCKE}	CKE input setup / hold time
DD202	$t_{d(clkL-NCS)}$	Delay time, lpddr2_ck low to lpddr2_ncs	t_{IH} / t_{IS}	Address and control input setup/hold time
DD203	$t_{d(clk-CA)}$	Delay time, lpddr2_ck low to lpddr2_caz[(3)]	t_{IH} / t_{IS}	Address and control input setup/hold time
DD204	$t_{w(CA)}$	Pulse duration, lpddr2_caz[(3)] high and low duration	t_{IPW}	Adress and control input pulse width
DD200b	$t_{cb(clk)}$	Cycle time, lpddr2_ck and lpddr2_nck	t_{CKb}	Clock cycle time
DD201b	$t_{db(clkL-CKE)}$	Delay time, lpddr2_ck low to lpddr2_cke	t_{ISCKEb} / t_{IHCKEb}	CKE input setup/hold time
DD202b	$t_{db(clkL-NCS)}$	Delay time, lpddr2_ck low to lpddr2_ncs	t_{ISb} / t_{IHb}	Address and control input setup / hold time
DD203b	$t_{db(clk-CA)}$	Delay time, lpddr2_ck low to lpddr2_caz[(3)]	t_{ISb} / t_{IHb}	Address and control input setup / hold time
DD400	$t_{c(DQSO)}$	Cycle time, lpddr2_dqsx[(1)] and lpddr2_ndqsx[(1)]	t_{CK}	Clock period jitter
DD401	$t_{w(DQSOH)}$	Pulse duration, lpddr2_dqsx[(1)] and lpddr2_ndqsx[(1)] high duration	t_{DQSH}	DQS input high-level width
DD401	$t_{w(DQSOL)}$	Pulse duration, lpddr2_dqsx[(1)] and lpddr2_ndqsx[(1)] low duration	t_{DQSL}	DQS input low-level width
DD402	$t_{sk(DQSO-NDQSO)}$	Skew , lpddr2_dqsx[(1)] edge to opposite lpddr2_ndqsx[(1)] edge	V_{IX}	Crossing point differential skew
DD403	$t_{d(DQSO-DQO/DM)}$	Delay time, lpddr2_dqsx[(1)] to lpddr2_dqy[(2)] and lpddr2_dmx[(1)]	t_{DS} / t_{DH}	DQ and DM input setup/hold time
DD404	$t_{d(DV-DQSO)}$	Delay time, lpddr2_dqsx[(1)] valid after lpddr2_ck transition	t_{DSS} / t_{DSH}	DQS falling edge to CK setup / hold time
DD405	$t_{d(clkV-DQSO)}$	Delay time, lpddr2_ck valid to first lpddr2_dqsx[(1)] edge	t_{DQSS}	Write command to first DQS latching transition
DD406	$t_{d(DQSOHZ-DQSOV)}$	Delay time, lpddr2_dqsx[(1)] high impedance to lpddr2_dqsx[(1)] valid	t_{WPRE}	Write preamble
DD407	$t_{d(DQSOV-DQSOHZ)}$	Delay time, lpddr2_dqsx[(1)] last edge to lpddr2_dqsx[(1)] high impedance state	t_{WPST}	Write postamble
DD408	$t_{w(DQO/DM)}$	Pulse duration, lpddr2_dqy[(2)] and lpddr2_dmx[(1)] high / low duration	t_{DIPW}	DQ qnd DM output pulse width
DD500	$t_{c(ACT-ACT)s}$	Cycle time, ACTIVE to ACTIVE command	t_{RC}	ACTIVE to ACTIVE command period
DD501	$t_{w(SRL)s}$	Pulse duration, lpddr2_cke during SELF REFRESH low duration	t_{CKESR}	CKE MIN. pulse width during self-refresh (low pulse width during self-refresh)
DD502	$t_{c(SR-VAL)s}$	Cycle time, SELF REFRESH to VALID command	t_{XSR}	Self refresh exit to next valid command delay
DD503	$t_{d(DPWDN)s}$	Delay time, POWER DOWN exit time	t_{XP}	Exit power down to next valid command delay
DD504	$t_{d(PWDN)s}$	Delay time, DEEP POWER DOWN command	t_{DPD}	MINimun deep power down time
DD505	$t_{c(RD-RD)s}$	Cycle time, READ to READ command	t_{CCD}	LPDDR2-S4 CAS to CAS delay
DD506	$t_{c(RD-PRE)s}$	Cycle time, READ to PRECHARGE command	t_{RTP}	Internal read to precharge command delay
DD507	$t_{c(ACT-RD)s}$	Cycle time, ACTIVE to READ command	t_{RCD}	RAS to CAS delay

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Table 6-20. LPDDR2 Switching Characteristics Correspondence Between Data Manual and LPDDR2 JEDEC Standard—(JESD209-2A)(4) (continued)

TIMING PARAMETERS			JEDEC STANDARD PARAMETERS	
REF.	DESCRIPTION		REF.	DESCRIPTION
DD508	$t_{d(PRE)s}$	Delay time, PRECHARGE command (8-bank)	$t_{RPab\ (8\text{-}bank)}$	Row precharge time (all banks)
DD509	$t_{c(ACT-PRE)s}$	Cycle time, ACTIVE to PRECHARGE command	t_{RAS}	Row active time
DD510	$t_{d(WRREC)s}$	Delay time, WRITE recovery time	t_{WR}	Write recovery time
DD511	$t_{c(WR-RD)s}$	Cycle time, WRITE to READ command	t_{WTR}	Internal write to read command delay
DD512	$t_{c(ACTBA-ACTBB)s}$	Cycle time, ACTIVE bank A to ACTIVE bank B command	t_{RRD}	Active bank A to active bank B
DD513	$t_{c(ACT-4B-ACT)s}$	Cycle time, four banks ACTIVE to ACTIVE command	t_{FAW}	Four bank activate window
DD514	$t_{c(REF)s}$	Cycle time, four banks REFRESH Command	t_{RFCab}	Refresh cycle time
DD601	$t_{c(ACT-RD/WR)n}$	Cycle time, ACTIVE to READ or WRITE command	t_{RCD} / t_{RCDMIN}	Activate to read / write command period
DD602	$t_{c(ACTBA-ACTBB)n}$	Cycle time, ACTIVE bank A to ACTIVE bank B command	t_{RRD}	Activate to activate command period (different row buffer)
DD603	$t_{c(ACT-ACT)n}$	Cycle time, ACTIVE to ACTIVE command	t_{RC}	Activate to activate command period (same row buffer)
DD604	$t_{c(CAS-CAS)n}$	Cycle time, CAS to CAS command	t_{CCD}	CAS to CAS delay
DD605	$t_{c(WRREC-ACT)n}$	Cycle time, WRITE recovery Time before ACTIVE	t_{WRA}	Write recovery time before activate
DD606	$t_{c(WR-RD)n}$	Cycle time, WRITE to READ command	t_{WTR}	Internal write to read command delay
DD607	$t_{c(PRE-ACT)n}$	Cycle time, PRECHARGE to ACTIVE command	t_{RP}	Preactive to activate command period
DD608	$t_{c(ACT-PRE)n}$	Cycle time, ACTIVE to PREACTIVE command	t_{RAS}	Activate to preactive command period
DD609	$t_{c(EXPWDN-VAL)n}$	Cycle time, EXIT POWER DOWN to next valid command	t_{XP}	Exit power down to next valid command delay
DD700	$t_{d(MRW)}$	Delay time, MODE REGISTER WRITE command	t_{MRW}	MODE REGISTER write command period
DD701	$t_{d(MRR)}$	Delay time, MODE REGISTER READ command	t_{MRR}	MODE REGISTER read command period
DD800	$t_{d(QINIT)}$	Delay time, initialization calibration command	t_{ZQINIT}	Initialization calibration time
DD801	$t_{d(QCL)}$	Delay time, long calibration command	t_{ZQCL}	Long calibration time
DD802	$t_{d(QCS)}$	Delay time, short calibration command	t_{ZQCS}	Short calibration time
DD803	$t_{d(QRESET)}$	Delay time, calibration reset command	$t_{ZQRESET}$	Calibration reset time

(1) x = [3:0]

(2) y = [31:0]

(3) z = [9:0]

(4) The timing correspondence in this table means that a system equation exists between the Data Manual parameters and the JEDEC ones.

6.5 Multimedia Interfaces

6.5.1 Camera Interface

The camera subsystem supports most of the raw image sensors available in the market. It contains two serial interfaces compatible with the CCP, MIPI® CSI1, and CSI2 protocols.

The main serial interface, CSI21, supports up to 4 data lanes (824 Mb/s maximum with 4 data lanes (412 MHz), 1Gb/s maximum with 3, 2, or 1 data lane(s) (500 MHz)) using CSI2 MIPI® standard.

The secondary CSI22 interface provides both CSI2 and CCP2 / CSI1 modes:

- CSI2 at 500 MHz (1 Gbps) in double data rate (DDR) mode

- CCP2 at 325 MHz (650 Mbps) in double data rate (DDR) mode
- CSI1 at 208 MHz (208 Mbps) in single data rate (SDR) mode

6.5.1.1 Camera Serial Interface (CSI2)

CSI2 camera serial interface is a MIPI® (MIPI® CSI2) D-PHY compliant interface connecting a digital camera module and a mobile phone application. This interface is made of three differential lanes, each of them being configurable for carrying data or clock. The polarity of each wire of a lane is also configurable.

6.5.1.1.1 CSI21 and CSI22—High-Speed Mode

Table 6-22 assumes testing over the recommended operating conditions and electrical characteristic conditions below (see Figure 6-44).

NOTE

If the skew degradation due to the interconnect (from the output transmitter ball to the input receiver ball) between the clock and the data lanes is less than ±170 ps (instead of ±200 ps in the MIPI D-PHY specification) then 1Gbps per data lane is achievable with 4 data lanes at OPP100 operating point. This must be met for an interconnect length less than 10 cm.

Table 6-21. CSI21 and CSI22 Timing Conditions—High-Speed Mode(1)(3)

TIMING CONDITION PARAMETER		VALUE		UNIT
		MIN	MAX	
Input Conditions: Up to 3 data lanes				
t_R	Input signal rise time(2)	0.135	0.4 * $t_{UI(INST,MIN)}$	ns
t_F	Input signal fall time(2)	0.135	0.4 * $t_{UI(INST,MIN)}$	ns
Input Conditions: 4 data lanes				
t_R	Input signal rise time(2)	0.166	0.4 * $t_{UI(INST,MIN)}$	ns
t_F	Input signal fall time(2)	0.166	0.4 * $t_{UI(INST,MIN)}$	ns

(1) For more information about $t_{UI(INST,MIN)}$ timing, see the CS2, CS3, and CS6 parameters defined in Table 6-22.
(2) Rise time or fall time are evaluated between differential input high threshold V_{IDTH} and differential input low threshold V_{IDTL}. For more information about V_{IDTH} and V_{IDTL} values, please see the MIPI D-PHY standard v1.0, High-Speed Receiver section.
(3) For more information on the PCB requirements, see Section A.4.3, *MIPI D-PHY PCB Guidelines in OMAP4*.

Table 6-22. CSI21 and CSI22 Timing Requirements—High-Speed Mode(2)(5)

NO.	PARAMETER		OPP100		OPP50		UNIT
			MIN	MAX	MIN	MAX	
Up to 3 Data Lanes							
CS1	1 / $t_{c(clk)}$	Frequency, input clock period		500		400	MHz
CS2, CS3	$t_{UI(INST,MIN)}$	Minimum instantaneous unit interval	0.9(4)		1.15(4)		ns
CS4	$t_{su(dV-clkH)}$	Setup time, data valid before clock rising edge	0.135(3)		0.173(3)		ns
CS5	$t_{h(clkH-dV)}$	Hold time, data valid after clock rising edge	0.135(3)		0.173(3)		ns
CS6	$t_{UI(INST,MIN)}$	Minimum instantaneous bit duration	0.9		1.15		ns
4 Data Lanes							
CS1	1 / $t_{c(clk)}$	Frequency, input clock period		412(6)		400	MHz
CS2, CS3	$t_{UI(INST,MIN)}$	Minimum instantaneous unit interval	1.11		1.15		ns
CS4	$t_{su(dV-clkH)}$	Setup time, input data valid before input clock rising edge	0.166(3)		0.173(3)		ns
CS5	$t_{h(clkH-dV)}$	Hold time, input data valid after input clock rising edge	0.166(3)		0.173(3)		ns

Table 6-22. CSI21 and CSI22 Timing Requirements—High-Speed Mode(2)(5) (continued)

NO.	PARAMETER		OPP100		OPP50		UNIT
			MIN	MAX	MIN	MAX	
CS6	$t_{UI(INST,MIN)}$	Minimum instantaneous bit duration	1.11		1.15		ns

(1) Related to the input maximum frequency supported by the CSI21 and CSI22 modules.

(2) The timing requirements are assured up to the minimum instantaneous bit duration.

(3) Setup/hold time = 0.15 x $t_{UI(INST,MIN)}$

(4) $t_{UI(INST,MIN)} = t_{UI(NOM)} - 100$ ps
Where: $t_{UI(NOM)}$ is the minimum unit interval. $t_{UI(NOM)} = 0.5 * t_{c(clk)}$.

(5) See DM Operating Condition Addendum for CORE OPP voltages.

(6) If the skew degradation due to the interconnect (from the output transmitter ball to the input receiver ball) between the clock and the data lanes is less than ±170 ps (instead of ±200 ps in the MIPI D-PHY specification) then 1Gbps per data lane is achievable with 4 data lanes at OPP100 operating point. This must be met for an interconnect length less than 10 cm.

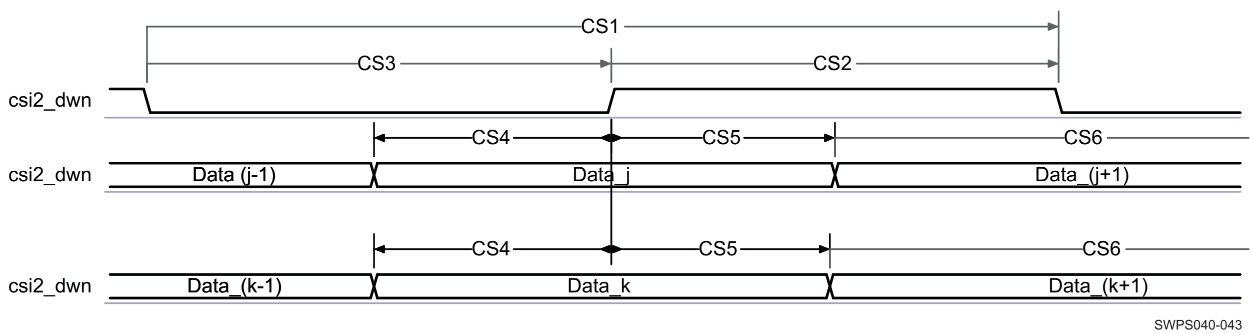

Figure 6-44. CSI21 and CSI22—High-Speed Mode(1)(2)(3)

(1) In csi2z_dwn, w is equal to x or y, n is equal to 0, 1, 2, 3, or 4 and z is equal to 1 or 2.

(2) The use of each csi2z_dwn lane (clock or data) is software programmable with the CSI2[1 or 2]_COMPLEXIO_CFG1 register, by setting bits field CLOCK_POSITION to 0x1, 0x2, 0x3, 0x4, 0x5.

(3) The polarity of each csi2z_dwn lane is software programmable with the CSI2[1 or 2]_COMPLEXIO_CFG1 register, DATAi_POL bit field.

6.5.1.1.2 CSI21 and CSI22—Low-Power and Ultralow-Power Modes

Table 6-24 assumes testing over the recommended operating conditions and electrical characteristic conditions below (see Figure 6-45).

Table 6-23. CSI21 and CSI22 Timing Conditions—Low-Power and Ultralow-Power Modes(2)

TIMING CONDITION PARAMETER		VALUE		UNIT
		MIN	MAX	
Input Conditions				
t_R	Input signal rise time(1)	2.6	25	ns
t_F	Input signal fall time(1)	2.6	25	ns

(1) Rise or fall time between 15% and 85% of the full signal swing. Input rise and fall times (t_R and t_F) are not applicable for clock lane.

(2) For more information on the PCB requirements, see Section A.4.3, *MIPI D-PHY PCB Guidelines in OMAP4*.

Table 6-24. CSI21 and CSI22 Timing Requirements—Low-Power and Ultralow-Power Modes(2)

NO.	PARAMETER		OPP100		OPP50		UNIT
			MIN	MAX	MIN	MAX	
CS7	$t_{V(LPstate)}$	Duration of a low-power state(1)	20		20		ns
	$t_{c(xorclk)}$	Period of the LP exclusive-OR clock	90		90		ns

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(1) Low-power and ultralow-power communication modes are asynchronous, data is Spaced-One-Hot bit encoded, data transfer clock is recovered by means of an XOR between csi2z_dxn and csi2z_dyn with n = 0, 1, 2, 3, or 4 and z is equal to 1 or 2. For more information about the LP exclusive-OR clock, see Table 19 of MIPI D-PHY standard v1.0.

(2) See DM Operating Condition Addendum for CORE OPP voltages.

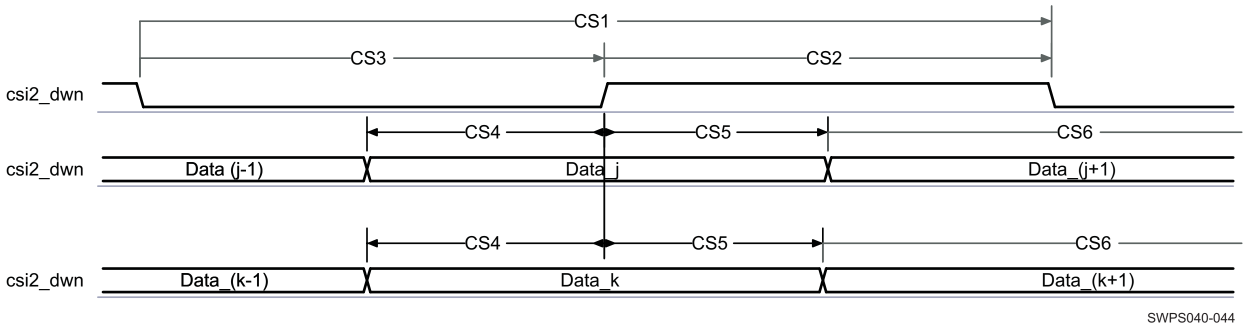

Figure 6-45. CSI21 and CSI22—Low-Power and Ultralow-Power Modes(1)(2)

(1) In csi2z_dxn and csi2z_dyn, n is equal to 0, 1, 2, 3, or 4 and z is equal to 1 or 2.

(2) Low-power and ultralow-power communication modes are asynchronous, data is Spaced-One-Hot bit encoded, data transfer clock is recovered by means of an XOR between csi2[1 or 2]_dxn and csi2[1 or 2]_dyn.

6.5.1.2 Camera Serial Interface (CCP2—CSI22)

Camera serial interface CCP2 is a MIPI serial interface supporting the following input data formats: YUV420, YUV422, RGB444, RGB565, RGB888, RAW6, RAW7, RAW8, RAW10, RAW12, or JPEG8. Clock and data are transferred on a differential SubLVDS link.

Table 6-26 assumes testing over the recommended operating conditions and electrical characteristic conditions below (see Figure 6-46 and Figure 6-47).

Table 6-25. CCP2—CSI22—Timing Conditions(2)

TIMING CONDITION PARAMETER		VALUE MIN	VALUE MAX	UNIT
CCP2 – Class 0 and Class 1/2 Input Conditions				
t_R	Input signal rise time(1)	0.3	0.6	ns
t_F	Input signal fall time(1)	0.3	0.6	ns
Δt_{RF}	Difference between rise / fall time of input data and input clock	–0.1	0.1	ns

(1) Rise or fall time between 20% and 80% of the full signal swing.

(2) For more information on the PCB requirements, see Section A.4.3, *MIPI D-PHY PCB Guidelines in OMAP4*.

Table 6-26. CCP2—CSI22—Timing Requirements(3)

NO.	PARAMETER		OPP100 MIN	OPP100 MAX	OPP50 MIN	OPP50 MAX	UNIT
CCP2 – Class 0							
CS0	$1 / t_{c(strb)}$	Frequency(2), input clock		208		208	MHz
CS1, CS2	$t_{w(strb)}$	Pulse duration, input clock high or low	0.45*P(1)	0.55*P(1)	0.45*P(1)	0.55*P(1)	ns
CS3	$t_{su(datV-strbH)}$	Setup time, input data valid before input clock rising edge	0.8		0.8		ns
CS4	$t_{h(strbH-datV)}$	Hold time, input data valid after input clock rising edge	0.8		0.8		ns
CCP2 – Class 1							
CS10	$1 / t_{c(strb)}$	Frequency(2), input strobe		208		208	MHz
CS11, CS17	$t_{w(strb)}$	Pulse width, input strobe and input data	1.1		1.1		ns

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Table 6-26. CCP2—CSI22—Timing Requirements[3] (continued)

NO.	PARAMETER		OPP100 MIN	OPP100 MAX	OPP50 MIN	OPP50 MAX	UNIT
CS12	$t_{sk(datV-strbH)}$	Skew time, input data valid before input strobe rising edge	0.78		0.78		ns
CS13	$t_{sk(strbH-datV)}$	Skew time, input data valid after input strobe falling edge	0.78		0.78		ns
CCP2 – Class 2							
CS10	$1 / t_{c(strb)}$	Frequency[2], input strobe		325		325	MHz
CS11, CS17	$t_{w(strb)}$	Pulse width, input strobe and input data	1.1		1.1		ns
CS12	$t_{sk(datV-strbH)}$	Skew time, input data valid before input strobe rising edge	0.78		0.78		ns
CS13	$t_{sk(strbH-datV)}$	Skew time, input data valid after input strobe falling edge	0.78		0.78		ns

(1) P = clock period in ns

(2) The maximum clock frequency of the CCP2 must be chosen to be the lowest possible for the application / transmitting device to reduce the power consumption of the sensor, the IO pad of the device and the camera core module itself.

(3) See DM Operating Condition Addendum for CORE OPP voltages.

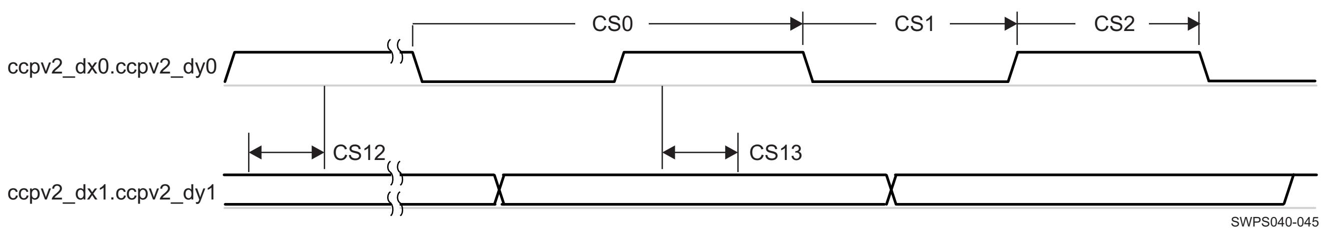

Figure 6-46. CCP2—CSI22—Class 0[(1)(2)(3)]

(1) ccpv2_dx0/ccpv2_dy0 and ccpv2_dx1/ccpv2_dy1 are the result of low-voltage differential data signal converters (see the Camera Subsystem in OMAP4430 TRM).

(2) The CCP2 receives up to 208 Mbps data rate or data/clock transmission.

(3) The CCP2 supports YUV422, YUV420, Bayer RGB444, RGB565, RGB888, RAW Bayer 6-, 7-, 8-, 10-, and 12-bit, and JPEG8 input data formats.

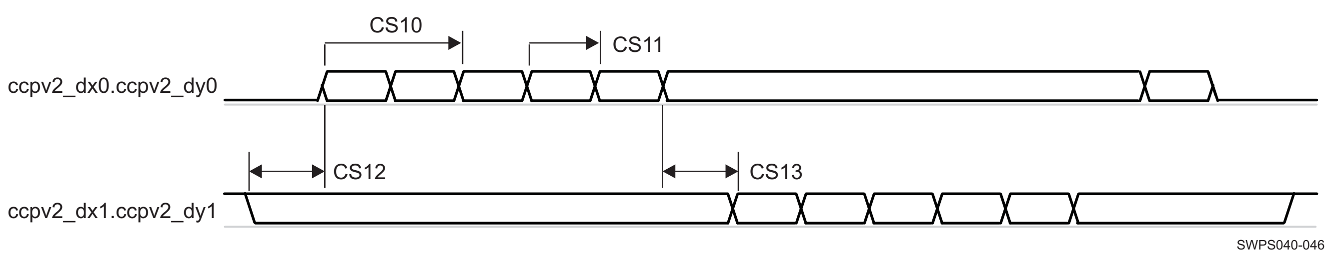

Figure 6-47. CCP2—CSI22—Class 1, Class 2[(1)(2)(3)]

(1) ccpv2_dx0/ccpv2_dy0 and ccpv2_dx1/ccpv2_dy1 are the result of low-voltage differential data signal converters (see the Camera Subsystem in OMAP4430 TRM).

(2) The CCP2 receives up to 208 Mbps data rate or data/clock transmission and up to 416 or 650 Mbps data rate for data/strobe transmission.

(3) The CCP2 supports YUV422, YUV420, Bayer RGB444, RGB565, RGB888, RAW Bayer 6-, 7-, 8-, 10-, and 12-bit, and JPEG8 input data formats.

6.5.2 Display Subsystem Interface

NOTE

For more information, see the Display Subsystem chapter in the OMAP4430 TRM.

The display subsystem (DSS) provides the logic to display a video frame from the memory frame buffer on a liquid-crystal display (LCD) panel or a TV set. The modules integrated in the display subsystem are:

- Display controller (DISPC)
- Remote Frame Buffer Interface (RFBI)
- Display Serial Interface (DSI)
- NTSC/PAL video encoder (VENC)

NOTE

The NTSC/PAL video encoder (VENC) is not described in the OMAP4430 Data Manual.

- High Definition Multimedia Interface (HDMI)

6.5.2.1 DSS—Display Controller (DISPC)

The DISPC interface consists of:

- 24-bit data bus
- Horizontal synchronization signal (HSYNC)
- Vertical synchronization signal (VSYNC)
- Data enable (DE)
- Pixel clock (PCLK)

This interface is functionally compliant to MIPI DPI standard revision 1.0 and delivers the parallel pixel / synchronization signals of the secondary LCD pipeline. DSI1 output must be deactivating when DISPC2 port is used.

6.5.2.1.1 DSS—DISPC—Quad eXtended Graphics Array (QXGA) Application—SDR Mode

Table 6-28 assumes testing over the recommended operating conditions and electrical characteristic conditions below (see Figure 6-48).

Table 6-27. DISPC Timing Conditions—QXGA SDR Mode(1)(2)(4)

TIMING CONDITION PARAMETER		VALUE		UNIT
		MIN	MAX	
PCB Conditions(3)				
	Number of external peripherals		1	
	Far end load		5	pF
	Trace length		2	cm
	Characteristics impedance	30	50	Ω

(1) IO settings: DS0 = 1.
For more information, see Control Module / Control Module Functional Description/ Functional Register Description / Signal Integrity Parameter Control Registers with Pad Group Assignment / I/O cells with Configurable Output Driver Impedance section of the OMAP4430 TRM.

(2) In this table the rise and fall times are calculated for 10% to 90% of VDDS. For more information on the corresponding OMAP4 VDDS power supply name, see Table 2-1, POWER [9] column with the ball name.

(3) Minimize the number of vias by layer transitions.

(4) To have an idea of the output OMAP4 ball load supported for this application, you can consider the following:
Output OMAP4 ball load = Far End load + 1.34 pF/cm typical x trace length (cm).

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Table 6-28. DISPC Switching Characteristics—QXGA SDR Mode[4]

NO.	PARAMETER		OPP100		UNIT
			MIN	MAX	
D1	1 / $t_{c(pclk)}$	Frequency[1], output pixel clock dispc2_pclk		170	MHz
D2	$t_{w(pclkL)}$	Pulse duration, output pixel clock dispc2_pclk low	0.5*P[2]		ns
D3	$t_{w(pclkH)}$	Pulse duration, output pixel clock dispc2_pclk high	0.5*P[2]		ns
	$t_{dc(pclk)}$	Duty cycle error, output pixel clock dispc2_pclk	–118	118	ps
	$t_{j(pclk)}$	Jitter standard deviation[3], output pixel clock dispc2_pclk		39	ps
	$t_{R(pclk)}$	Rise time, output pixel clock dispc2_pclk		1066	ps
	$t_{F(pclk)}$	Fall time, output pixel clock dispc2_pclk		959	ps
D4	$t_{d(pclkA-vsyncV)}$	Delay time, output pixel clock dispc2_pclk transition to output vertical synchronization dispc2_vsync valid	–1832	332	ps
	$t_{R(vsync)}$	Rise time, output vertical synchronization dispc2_vsync		1066	ps
	$t_{F(vsync)}$	Fall time, output vertical synchronization dispc2_vsync		959	ps
D5	$t_{d(pclkA-hsyncV)}$	Delay time, output pixel clock dispc2_pclk transition to output horizontal synchronization dispc2_hsync valid	–1832	332	ps
	$t_{R(hsync)}$	Rise time, output horizontal synchronization dispc2_hsync		1066	ps
	$t_{F(hsync)}$	Fall time, output horizontal synchronization dispc2_hsync		959	ps
D6	$t_{d(pclkA-dV)}$	Delay time, output pixel clock dispc2_pclk transition to output data dispc2_data[23:0] valid	–1832	332	ps
	$t_{R(d)}$	Rise time, output data dispc2_data[23:0]		1066	ps
	$t_{F(d)}$	Fall time, output data dispc2_data[23:0]		959	ps
D7	$t_{d(pclkA-deV)}$	Delay time, output pixel clock dispc2_pclk transition to output data enable dispc2_de valid	–1832	332	ps
	$t_{R(de)}$	Rise time, output data enable dispc2_de		1066	ps
	$t_{F(de)}$	Fall time, output data enable dispc2_de		959	ps
D8	$t_{d(pclkA-fidV)}$	Delay time, output pixel clock dispc2_pclk transition to output field ID dispc2_fid valid	–1832	332	ps
	$t_{R(fid)}$	Rise time, output field ID dispc2_fid		1066	ps
	$t_{F(fid)}$	Fall time, output field ID dispc2_fid		959	ps

(1) Related to the output dispc2_clk[4] maximum frequency programmable.
(2) P = output dispc2_pclk period in ns
(3) The jitter probability density can be approximated by a Gaussian function.
(4) See DM Operating Condition Addendum for CORE OPP voltages.

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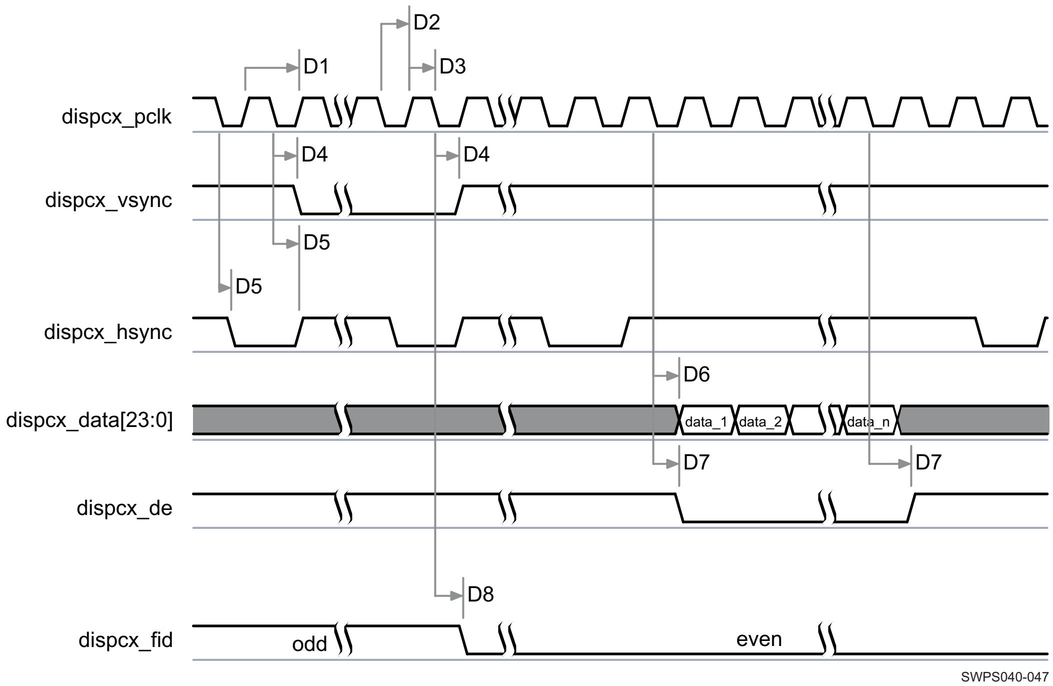

Figure 6-48. DSS—DISPC—QXGA SDR Application(1)(2)(3)(4)(5)(6)

(1) The configuration of assertion of the data can be programmed on the falling edge or rising edge of the pixel clock.

(2) In progressive mode, dispcx_fid signal is set to 0. In interlaced mode, the dispcx_fid signal toggles on the back edge of the vertical pulse.

(3) The polarity and the pulse width of dispcx_hsync and dispcx_vsync are programmable; see the DSS chapter in the OMAP4430 TRM.

(4) The dispcx_pclk(5) frequency can be configured, see DSS chapter in the OMAP4430 TRM.

(5) In dispcx_clk, x = 2

(6) For more information, see the DISPC chapter in the OMAP4430 TRM.

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6.5.2.2 DSS—Remote Frame Buffer Interface (RFBI) Applications

6.5.2.2.1 DSS—Remote Frame Buffer Interface (RFBI)—MIPI DBI2.0—LCD Panel

NOTE

For more information, see the Remote Frame Buffer Interface chapter in the OMAP4430 TRM.

The remote frame buffer interface (RFBI) module is part of the display subsystem that provides the logic to display a picture from the memory frame buffer (SDRAM or SRAM) on a liquid-crystal display (LCD) panel.

Table 6-30 and Table 6-31 assume testing over the recommended operating conditions and electrical characteristic conditions below (see Figure 6-49 through Figure 6-51).

Table 6-29. DSS—RFBI Timing Conditions—LCD Panel(1)(2)(3)

TIMING CONDITION PARAMETER		VALUE		UNIT
		MIN	MAX	
Input Conditions				
t_R	Input signal rise time		15	ns
t_F	Input signal fall time		15	ns
PCB Conditions				
	Number of external peripherals		1	
	Far end load		30	pF
	Trace length		20	cm
	Characteristics impedance	20	50	Ω

(1) IO settings: DS0 = 0.
For more information, see Control Module / Control Module Functional Description / Functional Register Description / Signal Integrity Parameter Control Registers with Pad Group Assignment / I/O cells with Configurable Output Driver Impedance section of the OMAP4430 TRM.

(2) In this table the rise and fall times are calculated for 30% to 70% of VDDS. For more information on the corresponding OMAP4 VDDS power supply name, see Table 2-1, POWER [9] column with the ball name.

(3) To have an idea of the output OMAP4 ball load supported for this application, you can consider the following:
Output OMAP4 ball load = Far End load + 1.34 pF/cm typical x trace length (cm).

Table 6-30. DSS—RFBI Timing Requirements—LCD Panel

NO.	PARAMETER		OPP100		OPP50		UNIT
			MIN	MAX	MIN	MAX	
DR0	$t_{su(dataV-rfbi\_rdH)}$	Setup time, rfbi_data[n:0](2) valid to rfbi_rd high	20		20		ns
DR1	$t_{h(rfbi\_rdH-dataIV)}$	Hold time, rfbi_rd high to rfbi_data[n:0](2) invalid	5.6		5.6		ns
	$t_{d(Data\ sampled)}$	rfbi_data are sampled at the end of the access time	N(1)		N(1)		ns

(1) N = (AccessTime) * (TimeParaGranularity + 1) * L3CLK

(2) rfbi_data[n:0], n up to 8

Table 6-31. DSS—RFBI Switching Characteristics—LCD Panel

NO.	PARAMETER		OPP100		OPP50		UNIT
			MIN	MAX	MIN	MAX	
	$t_{w(rfbi\_wrH)}$	Pulse duration, rfbi_we high	A(1)		A(1)		ns
	$t_{w(rfbi\_wrL)}$	Pulse duration, rfbi_we low	B(2)		B(2)		ns
	$t_{d(rfbi\_a0-rfbi\_wrL)}$	Delay time, rfbi_a0 transition to rfbi_we low	C(3)		C(3)		ns

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Table 6-31. DSS—RFBI Switching Characteristics—LCD Panel (continued)

NO.	PARAMETER		OPP100		OPP50		UNIT
			MIN	MAX	MIN	MAX	
	$t_{d(rfbi\_wrH-rfbi\_a0)}$	Delay time, rfbi_we high to rfbi_a0 transition	D(4)		D(4)		ns
	$t_{d(rfbi\_csx-rfbi\_wrL)}$	Delay time, rfbi_csx(14) low to rfbi_we low	E(5)		E(5)		ns
	$t_{d(rfbi\_wrH-rfbi\_csxH)}$	Delay time, rfbi_we high to rfbi_csx(14) high	F(6)		F(6)		ns
	$t_{d(dataV)}$	Output rfbi_data[n:0](15) valid	G(7)		G(7)		ns
	$t_{sk(Skew)}$	Skew between output write enable falling rfbi_we and output rfbi_data[n:0](15) high or low	1.81		1.81		ns
	$t_{d(rfbi\_a0H-rfbi\_rdL)}$	Delay time, rfbi_a0 high to rfbi_re low	H(8)		H(8)		ns
	$t_{d(rfbi\_rdlH-rfbi\_a0)}$	Delay time, rfbi_re high to rfbi_a0 transition	I(9)		I(9)		ns
	$t_{w(rfbi\_rdH)}$	Pulse duration, rfbi_re high	J(10)		J(10)		ns
	$t_{w(rfbi\_rdL)}$	Pulse duration, rfbi_re low	K(11)		K(11)		ns
	$t_{d(rfbi\_rdL-rfbi\_csxL)}$	Delay time, rfbi_re low to rfbi_csx(14) low	L(12)		L(12)		ns
	$t_{d(rfbi\_rdH-rfbi\_csxH)}$	Delay time, rfbi_re high to rfbi_csx(14) high	M(13)		M(13)		ns
	$t_{R(rfbi\_wr)}$	Rise time, rfbi_we		8		8	ns
	$t_{F(rfbi\_wr)}$	Fall time, rfbi_we		8		8	ns
	$t_{R(rfbi\_a0)}$	Rise time, rfbi_a0		8		8	ns
	$t_{F(rfbi\_a0)}$	Fall time, rfbi_a0		8		8	ns
	$t_{R(rfbi\_csx)}$	Rise time, rfbi_csx(14)		8		8	ns
	$t_{F(rfbi\_csx)}$	Fall time, rfbi_csx(14)		8		8	ns
	$t_{R(rfbi\_da)}$	Rise time, rfbi_data[n:0](15)		8		8	ns
	$t_{F(rfbi\_da)}$	Fall time, rfbi_data[n:0](15)		8		8	ns
	$t_{R(rfbi\_rd)}$	Rise time, rfbi_re		8		8	ns
	$t_{F(rfbi\_rd)}$	Fall time, rfbi_re		8		8	ns
	CsOnTime	CS signal assertion time from Start Access Time – RFBI_ONOFF_TIME Register	0(16)				ns
	CsOffTime	CS signal de-assertion time from Start Access Time – RFBI_ONOFF_TIME Register	65(16)				ns
	WeOnTime	WE signal assertion time from Start Access Time – RFBI_ONOFF_TIME Register	10(16)				ns
	WeOffTime	WE signal de-assertion time from Start Access Time – RFBI_ONOFF_TIME Register	30(16)				ns
	ReOnTime	RE signal assertion time from Start Access Time – RFBI_ONOFF_TIME Register	30(16)				ns
	ReOffTime	RE signal de-assertion time from Start Access Time – RFBI_ONOFF_TIME Register	65(16)				ns
	WeCycleTime	Write cycle time – RFBI_CYCLE_TIME_Register	50(16)				ns
	RdCycleTime	Read cycle time – RFBI_CYCLE_TIME_Register	65(16)				ns
	CsPulseWidth	CS pulse width – RFBI_CYCLE_TIME_Register	0(16)				ns

(1) A = (WeCycleTime – WeOffTime) * (TimeParaGranularity + 1) * L3CLK

(2) B = (WeOffTime – WeOntime) * (TimeParaGranularity + 1) * L3CLK

(3) C = (WEOnTime) * (TimeParaGranularity + 1) * L3CLK

(4) D = (WeCycleTime + CsPulseWidth – WeOffTime) * (TimeParaGranularity + 1) * L3CLK. * if mode Write to Read or Read to Write is enabled

(5) E = (WeOnTime – CsOnTime) * (TimeParaGranularity + 1) * L3CLK

(6) F = (CsOffTime – WeOffTime) * (TimeParaGranularity + 1) * L3CLK

(7) G = (WeCycleTime) * (TimeParaGranularity + 1) * L3CLK

(8) H = (ReOnTime) * (TimeParaGranularity + 1) * L3CLK

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(9) I = (ReCycleTime + CsPulseWidth – ReOffTime) * (TimeParaGranularity + 1) * L3CLK. * if mode Write to Read or Read to Write is enabled
(10) J = (ReCycleTime – ReOffTime) * (TimeParaGranularity + 1) * L3CLK
(11) K = (ReOffTime – ReOntime) * (TimeParaGranularity + 1) * L3CLK
(12) L = (ReOnTime – CsOnTime) * (TimeParaGranularity + 1) * L3CLK
(13) M = (CsOffTime – ReOffTime) * (TimeParaGranularity + 1) * L3CLK
(14) In RFBI_nCSx, x is equal to 0.
(15) rfbi_data[n:0], n up to 8
(16) These values are calculated by the following formula: RFBI registers values * L3 Clock (ns), with L3 clock = 200 MHz. See Table 6-32 for the RFBI registers values.

Table 6-32. DSS—RFBI Registers Configuration—LCD Panel(1)

DESCRIPTION	REGISTER AND BIT FIELD	BIT	VALUES
CS signal assertion time from Start Access Time	RFBI_ONOFF_TIME & CSONTIME	[3:0]	0b0000
CS signal de-assertion time from Start Access Time	RFBI_ONOFF_TIME & CSOFFTIME	[9:4]	0b001101: 13 cycles
WE signal assertion time from Start Access Time	RFBI_ONOFF_TIME & WEONTIME	[13:10]	0b0010: 2 cycles
WE signal de-assertion time from Start Access Time	RFBI_ONOFF_TIME & WEOFFTIME	[19:14]	0b000110: 6 cycles
RE signal assertion time from Start Access Time	RFBI_ONOFF_TIME & RDONTIME	[23:20]	0b000110: 6 cycles
RE signal de-assertion time from Start Access Time	RFBI_ONOFF_TIME & REOFFTIME	[29:24]	0b001101: 13 cycles
Write cycle time	RFBI_CYCLE_TIME & WECYCLETIME	[5:0]	0b001010: 10 cycles
Read cycle time	RFBI_CYCLE_TIME & RECYCLETIME	[11:6]	0b001101: 13 cycles
CS pulse width	RFBI_CYCLE_TIME & CSPULSEWIDTH	[17:12]	0b000000

(1) For more information on the RFBI registers, see the Display Subsystem / Remote Frame Buffer Interface section of the OMAP4430 TRM.

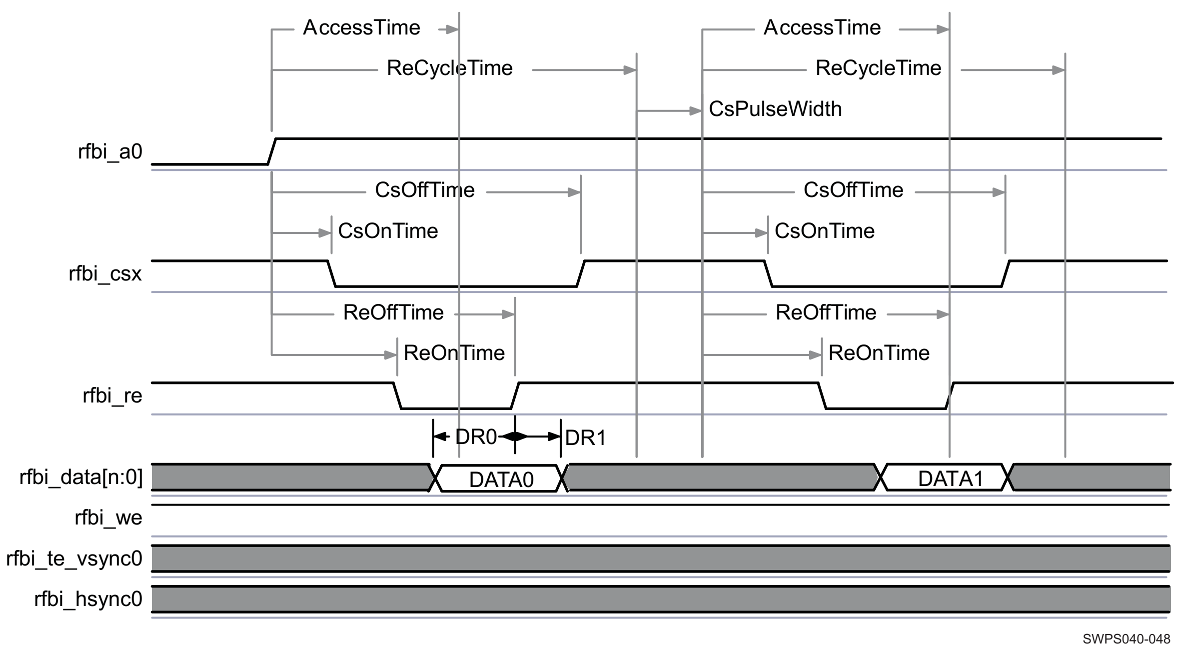

Figure 6-49. DSS—RFBI—Command / Data Write—LCD Panel(1)(2)(3)

(1) In rfbi_csx, x is equal to 0.
(2) In rfbi_data[n:0], n up to 8
(3) For more information, see the Display Subsystem chapter in the OMAP4430 TRM.

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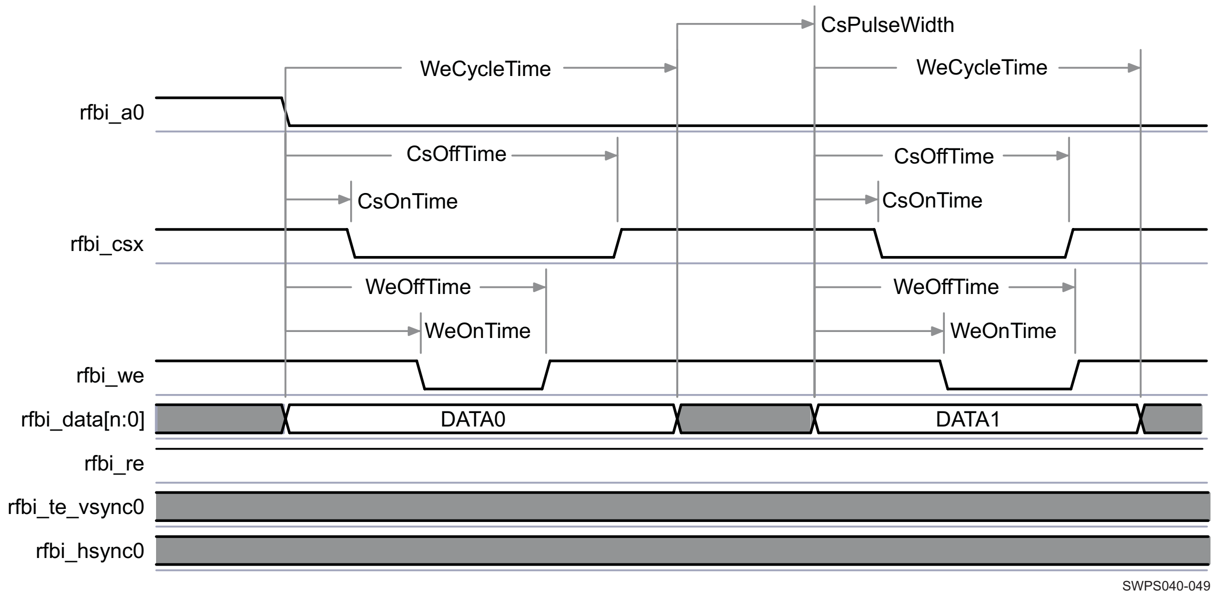

Figure 6-50. DSS—RFBI—Command / Data Read—LCD Panel(1)(2)(3)

(1) In rfbi_csx, x is equal to 0.
(2) In rfbi_data[n:0], n up to 8
(3) For more information, see the Display Subsystem chapter in the OMAP4430 TRM.

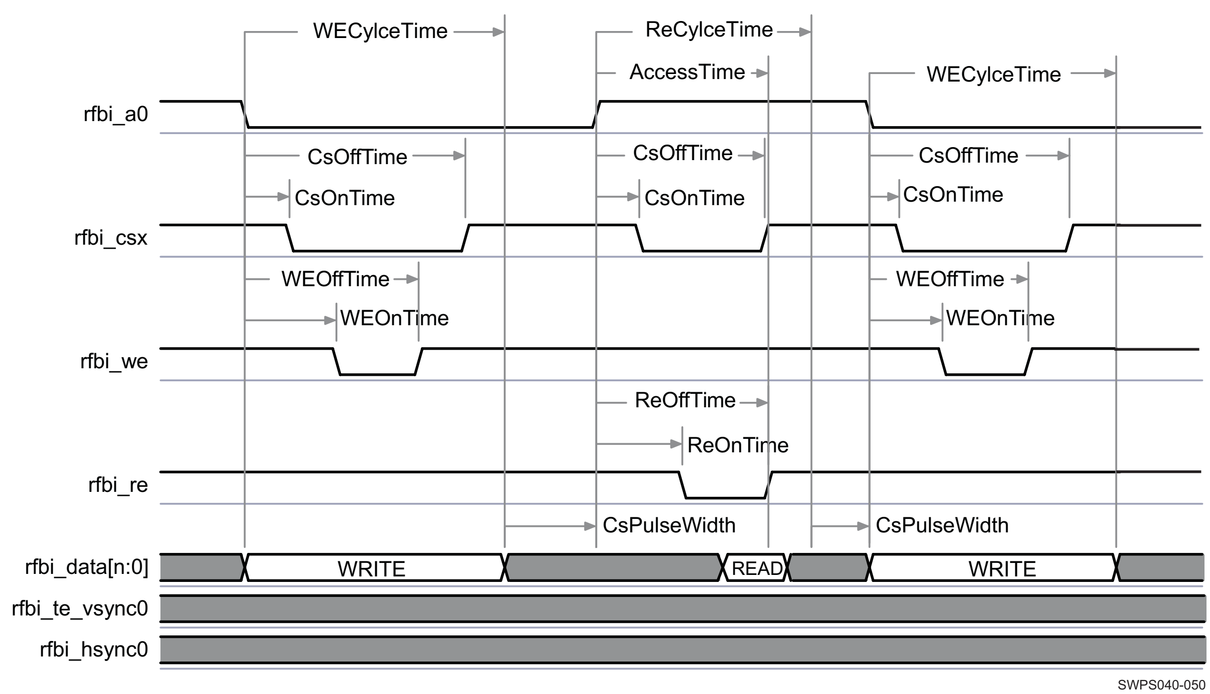

Figure 6-51. DSS—RFBI—Command / DataWrite to Read and Read to Write—LCD Panel(1)(2)(3)

(1) In rfbi_csx, x is equal to 0.
(2) In rfbi_data[n:0], n up to 8
(3) For more information, see the Display Subsystem chapter in the OMAP4430 TRM.

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6.5.2.2.2 DSS—Remote Frame Buffer Interface (RFBI)—Pico DLP

The Remote Frame Buffer Interface (RFBI) module can provide also the necessary control signals and data to interface to the Pico DLP driver of the Pico DLP panel.

Table 6-34 assume testing over the recommended operating conditions and electrical characteristic conditions below (see Figure 6-52).

Table 6-33. DSS—RFBI Timing Conditions—Pico DLP(1)(2)(3)

TIMING CONDITION PARAMETER		VALUE MIN	VALUE MAX	UNIT
PCB Conditions				
	Number of external peripherals		1	
	Far end load		5	pF
	Trace length		10	cm
	Characteristics impedance	30	50	Ω

(1) IO settings: DS0 = 0.
For more information, see Control Module / Control Module Functional Description/ Functional Register Description / Signal Integrity Parameter Control Registers with Pad Group Assignment / I/O cells with Configurable Output Driver Impedance section of the OMAP4430 TRM.

(2) In this table the rise and fall times are calculated for 20% to 80% of VDDS. For more information on the corresponding OMAP4 VDDS power supply name, see Table 2-1, POWER [9] column with the ball name.

(3) To have an idea of the output OMAP4 ball load supported for this application, you can consider the following:
Output OMAP4 ball load = Far End load + 1.34 pF/cm typical x trace length (cm).

Table 6-34. DSS—RFBI Switching Characteristics—Pico DLP(16)(17)(18)

NO.	PARAMETER		OPP100 MIN	OPP100 MAX	OPP50 MIN	OPP50 MAX	UNIT
	$t_{w(rfbi\_wrH)}$	Pulse duration, rfbi_we high	A(1)		A(1)		ns
	$t_{w(rfbi\_wrL)}$	Pulse duration, rfbi_we low	B(2)		B(2)		ns
	$t_{d(rfbi\_a0-rfbi\_wrL)}$	Delay time, rfbi_a0 transition to rfbi_we low	C(3)		C(3)		ns
	$t_{d(rfbi\_wrH-rfbi\_a0)}$	Delay time, rfbi_we high to rfbi_a0 transition	D(4)		D(4)		ns
	$t_{d(rfbi\_csx-rfbi\_wrL)}$	Delay time, rfbi_csx(14) low to rfbi_we low	E(5)		E(5)		ns
	$t_{d(rfbi\_wrH-rfbi\_csxH)}$	Delay time, rfbi_we high to rfbi_csx(14) high	F(6)		F(6)		ns
	$t_{d(dataV)}$	Output rfbi_data[n:0](15) valid	G(7)		G(7)		ns
	$t_{sk(Skew)}$	Skew between output write enable falling rfbi_we and output rfbi_data[n:0](15) high or low	15.6		15.6		ns
	$t_{d(rfbi\_a0H-rfbi\_rdL)}$	Delay time, rfbi_a0 high to rfbi_re low	H(8)		H(8)		ns
	$t_{d(rfbi\_rdlH-rfbi\_a0)}$	Delay time, rfbi_re high to rfbi_a0 transition	I(9)		I(9)		ns
	$t_{w(rfbi\_rdH)}$	Pulse duration, rfbi_re high	J(10)		J(10)		ns
	$t_{w(rfbi\_rdL)}$	Pulse duration, rfbi_re low	K(11)		K(11)		ns
	$t_{d(rfbi\_rdL-rfbi\_csxL)}$	Delay time, rfbi_re low to rfbi_csx(14) low	L(12)		L(12)		ns
	$t_{d(rfbi\_rdH-rfbi\_csxH)}$	Delay time, rfbi_re high to rfbi_csx(14) high	M(13)		M(13)		ns
	$t_{R(rfbi\_wr)}$	Rise time, rfbi_we		7		7	ns
	$t_{F(rfbi\_wr)}$	Fall time, rfbi_we		7		7	ns
	$t_{R(rfbi\_a0)}$	Rise time, rfbi_a0		7		7	ns
	$t_{F(rfbi\_a0)}$	Fall time, rfbi_a0		7		7	ns
	$t_{R(rfbi\_csx)}$	Rise time, rfbi_csx(14)		7		7	ns
	$t_{F(rfbi\_csx)}$	Fall time, rfbi_csx(14)		7		7	ns
	$t_{R(rfbi\_da)}$	Rise time, rfbi_data[n:0](15)		7		7	ns
	$t_{F(rfbi\_da)}$	Fall time, rfbi_data[n:0](15)		7		7	ns
	$t_{R(rfbi\_rd)}$	Rise time, rfbi_re		7		7	ns

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Table 6-34. DSS—RFBI Switching Characteristics—Pico DLP(16)(17)(18) (continued)

NO.	PARAMETER		OPP100		OPP50		UNIT
			MIN	MAX	MIN	MAX	
	$t_{F(rfbi\_rd)}$	Fall time, rfbi_re		7		7	ns
	CsOnTime	CS signal assertion time from Start Access Time – RFBI_ONOFF_TIME1 Register	0(19)				ns
	CsOffTime	CS signal de-assertion time from Start Access Time – RFBI_ONOFF_TIME1 Register	40(19)				ns
	WeOnTime	WE signal assertion time from Start Access Time – RFBI_ONOFF_TIME1 Register	0(19)				ns
	WeOffTime	WE signal de-assertion time from Start Access Time – RFBI_ONOFF_TIME1 Register	20(19)				ns
	ReOnTime	RE signal assertion time from Start Access Time – RFBI_ONOFF_TIME1 Register	-				ns
	ReOffTime	RE signal de-assertion time from Start Access Time – RFBI_ONOFF_TIME1 Register	-				ns
	WeCycleTime	Write cycle time – RFBI_CYCLE_TIME1_Register	40(19)				ns
	ReCycleTime	Read cycle time – RFBI_CYCLE_TIME1_Register	-				ns
	CsPulseWidth	CS pulse width – RFBI_CYCLE_TIME1_Register	0(19)				ns

(1) A = (WeCycleTime – WeOffTime) * (TimeParaGranularity + 1) * L3CLK

(2) B = (WeOffTime – WeOntime) * (TimeParaGranularity + 1) * L3CLK

(3) C = (WEOnTime) * (TimeParaGranularity + 1) * L3CLK

(4) D = (WeCycleTime + CsPulseWidth – WeOffTime) * (TimeParaGranularity + 1) * L3CLK
* if mode Write to Read or Read to Write is enabled.

(5) E = (WeOnTime – CsOnTime) * (TimeParaGranularity + 1) * L3CLK

(6) F = (CsOffTime – WeOffTime) * (TimeParaGranularity + 1) * L3CLK

(7) G = (WeCycleTime) * (TimeParaGranularity + 1) * L3CLK

(8) H = (ReOnTime) * (TimeParaGranularity + 1) * L3CLK

(9) I = (ReCycleTime + CsPulseWidth – ReOffTime) * (TimeParaGranularity + 1) * L3CLK
* if mode Write to Read or Read to Write is enabled.

(10) J = (ReCycleTime – ReOffTime) * (TimeParaGranularity + 1) * L3CLK

(11) K = (ReOffTime – ReOntime) * (TimeParaGranularity + 1) * L3CLK

(12) L = (ReOnTime – CsOnTime) * (TimeParaGranularity + 1) * L3CLK

(13) M = (CsOffTime – ReOffTime) * (TimeParaGranularity + 1) * L3CLK

(14) In RFBI_nCSx, x is equal to 0.

(15) rfbi_data[n:0], n up to 15.

(16) See DM Operating Condition Addendum for CORE OPP voltages.

(17) At OPP100, L3 clock is 200 MHz and at OPP50, L3 clock is 100 MHz.

(18) rfbi_wr must be at 25 MHz.

(19) These values are calculated by the following formula: RFBI Register (Values) * L3 Clock (ns), with L3 clock = 200 MHz. See Table 6-35 for the RFBI registers values.

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Table 6-35. DSS—RFBI Register Configuration—Pico DLP(1)

DESCRIPTION	REGISTER AND BIT FIELD	BIT	VALUES
CS signal assertion time from Start Access Time	RFBI_ONOFF_TIME1 & CSOnTime	[3:0]	0b0000
CS signal de-assertion time from Start Access Time	RFBI_ONOFF_TIME1 & CSOffTime	[9:4]	0b001000: 8 cycles
WE signal assertion time from Start Access Time	RFBI_ONOFF_TIME1 & WEOnTime	[13:10]	0b0000
WE signal de-assertion time from Start Access Time	RFBI_ONOFF_TIME1 & WEOffTime	[19:14]	0b000100: 4 cycles
RE signal assertion time from Start Access Time	RFBI_ONOFF_TIME1 & REOnTime	[23:20]	0b0000
RE signal de-assertion time from Start Access Time	RFBI_ONOFF_TIME1 & REOffTime	[29:24]	0b0000
Write cycle time	RFBI_CYCLE_TIME1 & WECycleTime	[5:0]	0b001000: 8 cycles
Read cycle time	RFBI_CYCLE_TIME1 & RdCycleTime	[11:6]	0b0000
CS pulse width	RFBI_CYCLE_TIME1 & CSPulseWidth	[17:12]	0b0000
Read to Write CS pulse width enable	RFBI_CYCLE_TIME1 & RWEnable	[18]	0b0
Read to Read CS pulse width enable	RFBI_CYCLE_TIME1 & RREnable	[19]	0b0
Write to Write CS pulse width enable	RFBI_CYCLE_TIME1 & WWEnable	[20]	0b0
Write to Read CS pulse width enable	RFBI_CYCLE_TIME1 & WREnable	[21]	0b0
From Start Access Time to CLK rising edge used for the first data capture	RFBI_CYCLE_TIME1 & AccessTime	[27:22]	0b0000
Latencies multiplied by 2.	RFBI_CONFIG1 & TimeParaGranularity	[4]	0b0: x2 latency disable

(1) For more information on the RFBI registers, see the Display Subsystem / Remote Frame Buffer Interface section of the OMAP4430 TRM.

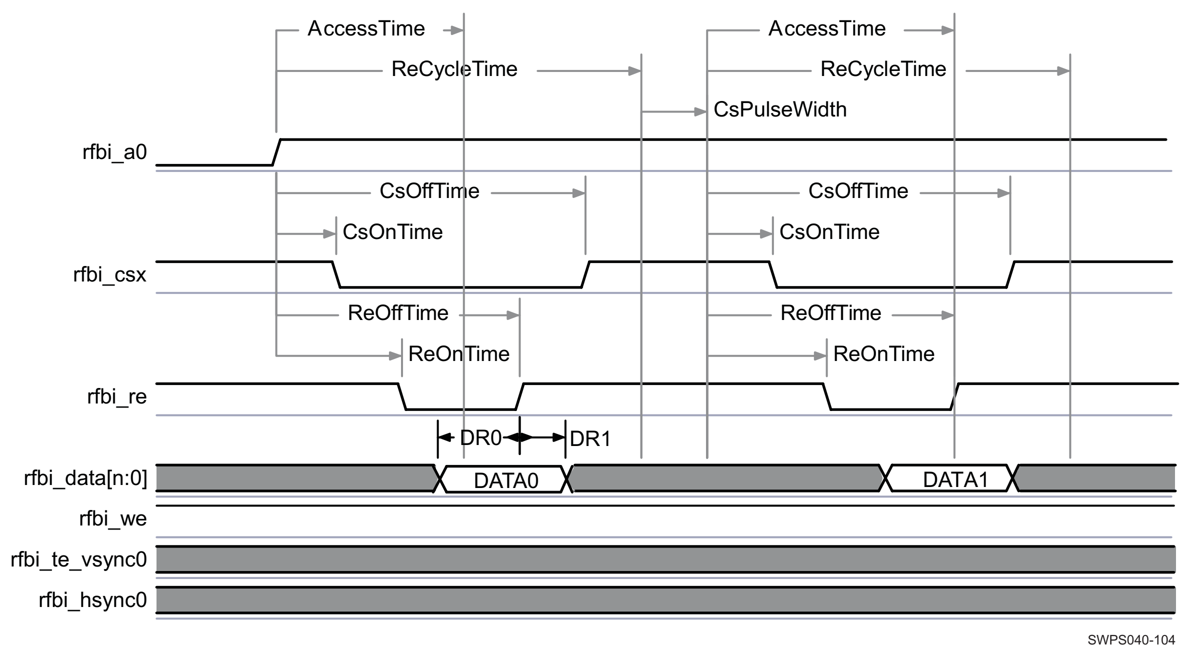

Figure 6-52. DSS—RFBI—Command / Data Write—Pico DLP(1)(2)(3)

(1) In rfbi_csx, x is equal to 0.
(2) In rfbi_data[n:0], n up to 15
(3) For more information, see the Display Subsystem chapter in the OMAP4430 TRM.

6.5.2.3 Display Serial Interface (DSI1)

NOTE

For more information, see the MIPI Display Serial chapter in the OMAP4430 TRM.

Display Serial Interface is a MIPI D-PHY compliant interface connecting a display module and a mobile phone application. This interface is made of three differential lanes, each of them being configurable for carrying data or clock. The polarity of each wire of a lane is also configurable.

6.5.2.3.1 DSS—DSI—High-Speed Mode

Table 6-36 assumes testing over the recommended operating conditions and electrical characteristic conditions below (see Figure 6-53).

Table 6-36. DSS—DSI Switching Characteristics—High-Speed Mode[(2)(4)(5)(6)]

NO.	PARAMETER		OPP100		OPP50		UNIT
			MIN	MAX	MIN	MAX	
DSI1 and DSI2 – Up To 3 Data Lanes							
DSI1	$1 / t_{c(clk)}$	Frequency[(1)], output clock	40	450	40	450	MHz
DSI1 – 4 Data Lanes							
DSI1	$1 / t_{c(clk)}$	Frequency[(1)], output clock	40	412	40	412	MHz
DSI1 and DSI2 – Up To 3 Data Lanes Or 4 Data Lanes							
DSI2, DSI3	$t_{UI[NOM]}$	Instantaneous unit interval	$t_{c(clk)}$ / 2		$t_{c(clk)}$ / 2		ns
DSI4	$t_{UI(INST,MIN)}$	Instantaneous bit duration	$t_{UI[NOM]} - t_{j(UI(INST,MIN))}$		$t_{UI[NOM]} - t_{j(UI(INST,MIN))}$		ns
	$t_{j(UI(INST,MIN))}$	Total jitter / uncertainty on instantaneous unit interval including clock jitter, DSI PHY transmitter jitter and duty cycle degradation		2.5% * $t_{UI[NOM]}$ + 0.05		2.5% * $t_{UI[NOM]}$ + 0.05	ns
DSI5	$t_{d(clkAE-dV)}$	Delay time, clock active edge to next data valid or delay time, previous data valid to clock active edge	50% * $t_{UI(INST,MIN)} - t_{SKEW}$	50% * $t_{UI(INST,MIN)} + t_{SKEW}$	50% * $t_{UI(INST,MIN)} - t_{SKEW}$	50% * $t_{UI(INST,MIN)} + t_{SKEW}$	ns
	t_{SKEW}	Lane to lane skew introduced by DSI PHY transmitter		15% * $t_{UI(INST,MIN)}$		15% * $t_{UI(INST,MIN)}$	ns
	$t_{R(DXi-DYi)}$	Rise time, dsim_dxn, dsim_dyn[(3)], (20% to 80%)	0.150	0.3 * $t_{UI(INST,MIN)}$	0.150	0.3 * $t_{UI(INST,MIN)}$	ns
	$t_{F(DXi-DYi)}$	Fall time, dsim_dxn, dsim_dyn[(3)], (20% to 80%)	0.150	0.3 * $t_{UI(INST,MIN)}$	0.150	0.3 * $t_{UI(INST,MIN)}$	ns

(1) Related to the maximum frequency supported by the DSI module.

(2) The timing requirements are assured up to the minimum instantaneous bit duration.

(3) In dsim_dxn and dsim_dyn, m is equal to 1 or 2, and n is equal to 0, 1, 2, 3, or 4 for DSI1 and n is equal to 0, 1, or 2 for DSI2.

(4) No specific capacitive load is needed in DSI high-speed mode. The PCB interconnect must be 50-Ω transmission line on DSI dsim_dx[2;0] and DSI dsim_dy[2;0]. DSI dsim_dx[2;0] and DSI dsi_dy[2;0] lines must be well matched. See Chapter 7 of the MIPI D-PHY standard v1.0 for completes specification of the Interconnect.

(5) See DM Operating Condition Addendum for CORE OPP voltages.

(6) For more information on the PCB requirements, see Section A.4.3, *MIPI D-PHY PCB Guidelines in OMAP4*.

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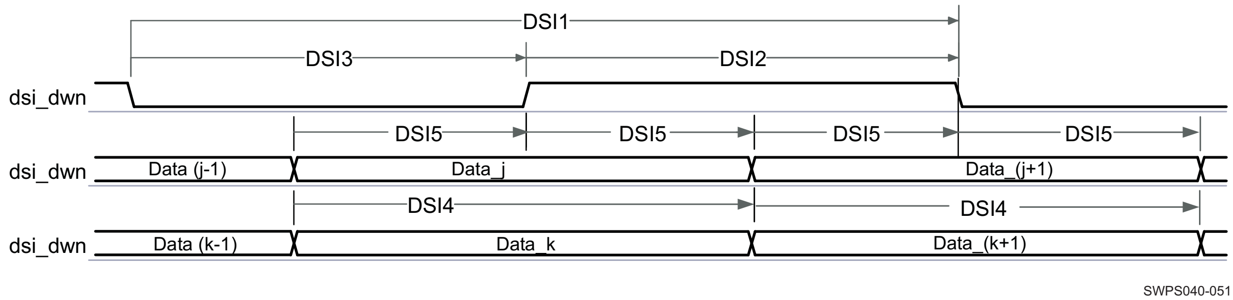

Figure 6-53. DSS—DSI—High-Speed Mode(1)(2)(3)

(1) In dsim_dwn, w is equal to x or y, m is equal to 1 or 2, and n is equal to 0, 1, 2, 3, or 4 for DSI1 and n is equal to 0, 1, or 2 for DSI2.

(2) The use of each dsim_dwn(1) lane (clock or data) is software programmable with the DSI_COMPLEXIO_CFG1 register. For more information, see the Display Subsystem chapter in the OMAP4430 TRM.

(3) The polarity of each dsim_dwn(1) lane is software programmable with the DSI_COMPLEXIO_CFG1 register. For more information, see the Display Subsystem chapter in the OMAP4430 TRM.

6.5.2.3.2 DSS—DSI—Low-Power and Ultralow-Power Modes

Table 6-38 assumes testing over the recommended operating conditions and electrical characteristic conditions below (see Figure 6-54).

Table 6-37. DSS—DSI Timing Conditions—Low-Power and Ultralow-Power Modes(3)

TIMING CONDITION PARAMETER		VALUE		UNIT
		MIN	MAX	
Output Condition				
C_{LOAD}	Output load capacitance	0	60(1)	pF

(1) The maximum capacitive load for the DSI low-power mode is equal to 60 pF. See Chapter 8 of the MIPI D-PHY standard v1.0 for complete specification on the electrical characteristics. The PCB interconnect must be 50-Ω transmission line on DSI dsim_dx[n;0](2) and DSI dsim_dy[n;0](2). DSI dsim_dx[n;0](2) and DSI dsim_dy[n;0](2) lines must be well matched. See Chapter 7 of the MIPI D-PHY standard v1.0 for complete specification of the interconnect.

(2) In dsim_dxn and dsim_dyn, m is equal to 1 or 2, and n is equal to 0, 1, 2, 3, or 4 for DSI1 and n is equal to 0, 1, or 2 for DSI2.

(3) For more information on the PCB requirements, see Section A.4.3, *MIPI D-PHY PCB Guidelines in OMAP4*

Table 6-38. DSI Switching Characteristics—Low-Power and Ultralow-Power Modes(5)

NO.	PARAMETER			OPP100		OPP50		UNIT
				MIN	MAX	MIN	MAX	
DSI6	$t_{w(XORclk)}$	Pulse width of the LP exclusive-OR clock(1)	First LP exclusive-OR clock(1) pulse after Stop state or last pulse before Stop state	40		40		ns
			All other pulses	20		20		ns
	$t_{c(XORclk)}$	Period of the LP exclusive-OR clock(1)		90		90		ns
	$t_{REOT(LP)}$	Rise time, dsim_dxn, dsim_dyn(4)			35		35	ns
	$t_{R(LP)}$	Rise time, dsim_dxn, dsim_dyn(2)(3) for a 5-pF C_L load		2.6	25	2.6	25	ns
		Rise time, dsim_dxn, dsim_dyn(2)(3) for a 20-pF C_L load		3.1	25	3.1	25	
		Rise time, dsim_dxn, dsim_dyn(2)(3) for a 70-pF C_L load		5.1	25	5.1	25	

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Table 6-38. DSI Switching Characteristics—Low-Power and Ultralow-Power Modes[5] (continued)

NO.	PARAMETER		OPP100		OPP50		UNIT
			MIN	MAX	MIN	MAX	
	$t_{F(LP)}$	Fall time, dsim_dxn, dsim_dyn[2][3] or a 5-pF C_L load	2.6	25	2.6	25	ns
		Fall time, dsim_dxn, dsim_dyn[2][3] or a 20-pF C_L load	3.1	25	3.1	25	
		Fall time, dsim_dxn, dsim_dyn[2][3] or a 70-pF C_L load	5.1	25	5.1	25	

(1) Low-power and ultralow-power communication modes are asynchronous, data is Spaced-One-Hot bit encoded, data transfer clock is recovered by means of an XOR between dsim_dxn[2] and dsim_dyn[2]. For more information about the LP exclusive-OR clock, see Table 19 of MIPI D-PHY standard v1.0.

(2) In dsim_dxn and dsim_dyn, m is equal to 1 or 2, and n is equal to 0, 1, 2, 3, or 4 for DSI1 and n is equal to 0, 1, or 2 for DSI2.

(3) The output rise and fall times are measured between 15% and 85% of vdds_dsi.

(4) Rise or fall time between 30% and 85% of the low-power (LP) levels. This is applicable only when high-speed (HS) burst is ending, that is, the lines go from a high-speed state 0 or a high-speed state 1 to a low-power stop state (the differential drive is stopped). Since there is extra load on the lines (the receiver in low-power mode has a common mode capacitor of up to 60 pF), this is slower. See the Low-Power Receiver Mode (LPRX) section of Table 3-9 for the Low-Power V_{IL}/V_{OL} input threshold values.

(5) See DM Operating Condition Addendum for CORE OPP voltages.

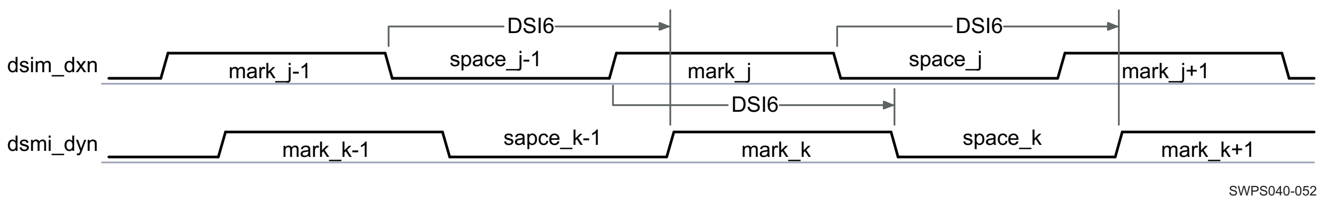

Figure 6-54. DSS—DSI—Low-Power and Ultralow-Power Modes[1][2]

(1) In dsim_dwn, w is equal to x or y, m is equal to 1 or 2, and n is equal to 0, 1, 2, 3, or 4 for DSI1 and n is equal to 0, 1, or 2 for DSI2.

(2) Low-Power and Ultralow-Power communication modes are asynchronous, data is Spaced-One-Hot bit encoded, data transfer clock is recovered by means of an XOR between dsim_dxn[1] and dsim_dyn[1].

6.5.2.4 High Definition Multimedia Interface (HDMI)

NOTE

For more information on HDMI, please contact your TI representative.

6.6 Serial Communications Interfaces

6.6.1 Multichannel Buffered Serial Port (McBSP)

NOTE

For more information, see the Serial Communication Interface / Multichannel Buffered Serial Port (McBSP) / McBSP Functional Description section of the OMAP4430 TRM.

The multichannel buffered serial port (McBSP) provides a full-duplex direct serial interface between the OMAP chip and other devices in a system, such as other application chips, codecs. It can accommodate a wide range of peripherals and clocked frame oriented protocols (I2S™, PCM, TDM) due to its high level of versatility.

McBSP supports two types of data transfer at the system level:

- The full-cycle mode, for which one clock period is used to transfer the data, generated on one edge and captured on the same edge (one clock period later).

- The half-cycle mode, for which one-half clock period is used to transfer the data, generated on one edge and captured on the opposite edge (one-half clock period later). Note that a new data is generated only every clock period, which secures the required hold time.

The interface clock (clkX/CLKR) activation edge (data/frame sync capture and generation) has to be configured accordingly with the external peripheral (activation edge capability) and the type of data transfer required at the system level.

Depending on the number of pins, McBSP supports either:

- 6-pin mode: dx and dr as data pins; clkx, clkr, fsx, and fsr as control pins.
- 4-pin mode: dx and dr as data pins; clkx and fsx pins as control pins. The clkx and fsx pins are internally looped back, via software configuration, respectively to the clkr and fsr internal signals for data receive.

6.6.1.1 McBSP1, McBSP2, and McBSP3 Set#1

6.6.1.1.1 McBSP1, McBSP2, and McBSP3 Set#1—I2S/PCM

Table 6-40 through Table 6-43 assume testing over the recommended operating conditions and electrical characteristic conditions below (see Figure 6-55 and Figure 6-56).

Table 6-39. McBSP1, 2 Timing Conditions—I2S/PCM(1)(2)(3)

SYSTEM CONDITION PARAMETER		VALUE		UNIT
		MIN	MAX	
Input Conditions				
t_R	Input signal rise time	400	6500	ps
t_F	Input signal fall time	400	6500	ps
PCB Conditions				
	Number of external peripherals		1	
	Far end load		5	pF
	Trace length		9	cm
	Characteristics impedance	30	55	Ω

(1) IO settings: MB[1:0] = 10 and LB0 = 0.
For more information, see Control Module / Control Module Functional Description/ Functional Register Description / Signal Integrity Parameter Control Registers with Pad Group Assignment / 50-Ω Output Buffer I/Os with Combined Mode and Load Settings section of the OMAP4430 TRM.

(2) In this table the rise and fall times are calculated for 10% to 90% of VDDS. For more information on the corresponding OMAP4 VDDS power supply name, see Table 2-1, POWER [9] column with the ball name.

(3) To have an idea of the output OMAP4 ball load supported for this application, you can consider the following:
Output OMAP4 ball load = Far End load + 1.34 pF/cm typical x trace length (cm).

6.6.1.1.1.1 McBSP1 and McBSP2—I2S/PCM Full and Half Cycle—Master Mode—24 MHz

Table 6-40. McBSP1, 2 Timing Requirements—I2S/PCM—Master Mode(1)(3)(4)

NO.	PARAMETER		OPP100		OPP50		UNIT
			MIN	MAX	MIN	MAX	
BM5	$t_{su(drV-clkAE)}$	Setup time, abe_mcbspx_dr valid before abe_mcbspx_clk(2) active edge	4.6		10.5		ns
BM6	$t_{h(clkAE-drV)}$	Hold time, abe_mcbspx_dr valid after abe_mcbspx_clk(2) active edge	0.7		0.6		ns

(1) The timings apply to all configurations regardless of abe_mcbspx_clk polarity and which clock edges are used to drive output data and capture input data.

(2) abe_mcbspx_clk corresponds to either abe_mcbspx_clkx or abe_mcbspx_clkr; abe_mcbspx_clkr is available in 6-pin mode only.

(3) In abe_mcbspx, x is equal to 1 or 2.

(4) See DM Operating Condition Addendum for CORE OPP voltages.

Table 6-41. McBSP1, 2 Switching Characteristics—I2S/PCM—Master Mode(4)(7)(9)

NO.	PARAMETER		OPP100		OPP50		UNIT
			MIN	MAX	MIN	MAX	
BM0	$1 / t_{c(clk)}$	Frequency(1), output abe_mcbspx_clk(5) clock		24.576(8)		12.288(8)	MHz
BM1	$t_{w(clkL)}$	Typical pulse duration, output abe_mcbspx_clk(5) low	0.5*P(2)		0.5*P(2)		ns
BM2	$t_{w(clkH)}$	Typical pulse duration, output abe_mcbspx_clk(5) high	0.5*P(2)		0.5*P(2)		ns
	$t_{dc(clk)}$	Duty cycle error, output abe_mcbspx_clk(5)	–2035	2035	–4069	4069	ps
	$t_{j(clk)}$	Jitter standard deviation(3), output abe_mcbspx_clk(5)		65		65	ps
	$t_{R(clk)}$	Rise time, output abe_mcbspx_clk(5)	400	6500	400	6500	ps
	$t_{F(clk)}$	Fall time, output abe_mcbspx_clk(5)	400	6500	400	6500	ps
BM3	$t_{d(clkAE-fsV)}$	Delay time, output abe_mcbspx_clk(5) active edge to output abe_mcbspx_fs(6) valid	0.9	11.0	1.0	22.6	ns
BM4	$t_{d(clkxAE-dxV)}$	Delay time, output abe_mcbspx_clkx active edge to output abe_mcbspx_dx valid	0.9	11.0	1.0	22.6	ns
	$t_{R(fs)}$	Rise time, output abe_mcbspx_fs(6)	400	6500	400	6500	ps
	$t_{F(fs)}$	Fall time, output abe_mcbspx_fs(6)	400	6500	400	6500	ps
	$t_{R(dx)}$	Rise time, output abe_mcbspx_dx	400	6500	400	6500	ps
	$t_{F(dx)}$	Fall time, output abe_mcbspx_dx	400	6500	400	6500	ps

(1) Related to the output abe_mcbspx_clkx / abe_mcbspx_clkr maximum and minimum frequency programmable in McBSP module by setting the configuration register SRGR1_REG[7..0].
For more information regarding the registers configuration see the Serial Communication Interface / Multichannel Buffered Serial Port (McBSP) / MCBSP Register Manual / MCBSP Registers / MCBSP Register Summary Table section of the OMAP4430 TRM.
(2) P = abe_mcbspx_clkx / abe_mcbspx_clkr output clk period in ns.
(3) The jitter probability density can be approximated by a Gaussian function.
(4) The timings apply to all configurations regardless of abe_mcbspx_clk polarity and which clock edges are used to drive output data and capture input data.
(5) abe_mcbspx_clk corresponds to either abe_mcbspx_clkx or abe_mcbspx_clkr; abe_mcbspx_clkr is available in 6-pin mode only.
(6) abe_mcbspx_fs corresponds to either abe_mcbspx_fsx or abe_mcbspx_fsr; abe_mcbspx_fsr is available in 6-pin mode only.
(7) In abe_mcbspx, x is equal to 1 or 2.
(8) This McBSP1, 2 output clock frequency is based on an output ABE DPLL configured at 196.608 MHz.
For more information regarding the registers configuration, see the Power, Reset and Clock Management / Clock Management Functional Description / Internal Clock Sources/Generators / DPLL_ABE Description section of the OMAP4430 TRM.
(9) See DM Operating Condition Addendum for CORE OPP voltages.

6.6.1.1.1.2 McBSP1 and McBSP2—I2S/PCM Full and Half Cycle—Slave Mode—12 MHz

Table 6-42. McBSP1, 2 Timing Requirements—I2S/PCM—Slave Mode(4)(5)(8)(9)

NO.	PARAMETER		OPP100		OPP50		UNIT
			MIN	MAX	MIN	MAX	
BS0	$1 / t_{c(clk)}$	Frequency(1), abe_mcbspx_clk(6)		12.288		6.144	MHz
BS1	$t_{w(clkL)}$	Typical pulse duration, abe_mcbspx_clk(6) low	0.5*P(2)		0.5*P(2)		ns
BS2	$t_{w(clkH)}$	Typical pulse duration, abe_mcbspx_clk(6) high	0.5*P(2)		0.5*P(2)		ns
	$t_{dc(clk)}$	Duty cycle error, abe_mcbspx_clk(6)	–2035	2035	–4069	4069	ps
	$t_{j(clk)}$	Cycle jitter(3), abe_mcbspx_clk(6)		1221		2000	ps
BS3	$t_{su(fsV-clkAE)}$	Setup time, abe_mcbspx_fs(7) valid before abe_mcbspx_clk(6) active edge	14.3		30.4		ns
BS4	$t_{h(clkAE-fsV)}$	Hold time, abe_mcbspx_fs(7) valid after abe_mcbspx_clk(6) active edge	14.3		30.4		ns
BS6	$t_{su(drV-clkAE)}$	Setup time, abe_mcbspx_dr valid before abe_mcbspx_clk(6) active edge	14.3		30.4		ns

Table 6-42. McBSP1, 2 Timing Requirements—I2S/PCM—Slave Mode[(4)(5)(8)(9)] (continued)

NO.	PARAMETER		OPP100		OPP50		UNIT
			MIN	MAX	MIN	MAX	
BS7	$t_{h(clkAE-drV)}$	Hold time, abe_mcbspx_dr valid after abe_mcbspx_clk[(6)] active edge	14.3		30.4		ns

(1) Related to the input maximum frequency supported by the McBSP module.
(2) P = abe_mcbspx_clkx / abe_mcbspx_clkr period in ns
(3) Maximum cycle jitter supported by abe_mcbspx_clkx / abe_mcbspx_clkr input clock.
(4) The timing requirements are assured for the cycle jitter and duty cycle error conditions specified.
(5) The timings apply to all configurations regardless of abe_mcbspx_clk polarity and which clock edges are used to drive output data and capture input data.
(6) abe_mcbspx_clk corresponds to either abe_mcbspx_clkx or abe_mcbspx_clkr; abe_mcbspx_clkr is available in 6-pin mode only.
(7) abe_mcbspx_fs corresponds to either abe_mcbspx_fsx or abe_mcbspx_fsr; abe_mcbspx_fsr is available in 6-pin mode only.
(8) In abe_mcbspx, x is equal to 1 or 2.
(9) See DM Operating Condition Addendum for CORE OPP voltages.

Table 6-43. McBSP1, 2 Switching Characteristics—I2S/PCM—Slave Mode[(1)(2)(3)]

NO.	PARAMETER		OPP100		OPP50		UNIT
			MIN	MAX	MIN	MAX	
BS5	$t_{d(clkxAE-dxV)}$	Delay time, input abe_mcbspx_clkx active edge to output abe_mcbspx_dx valid	–16.4	20.3	–34.0	36.1	ns
	$t_{R(dx)}$	Rise time, output abe_mcbspx_dx	400	6500	400	6500	ps
	$t_{F(dx)}$	Fall time, output abe_mcbspx_dx	400	6500	400	6500	ps

(1) The timings apply to all configurations regardless of abe_mcbspx_clk polarity and which clock edges are used to drive output data and capture input data.
(2) In abe_mcbspx, x is equal to 1 or 2.
(3) See DM Operating Condition Addendum for CORE OPP voltages.

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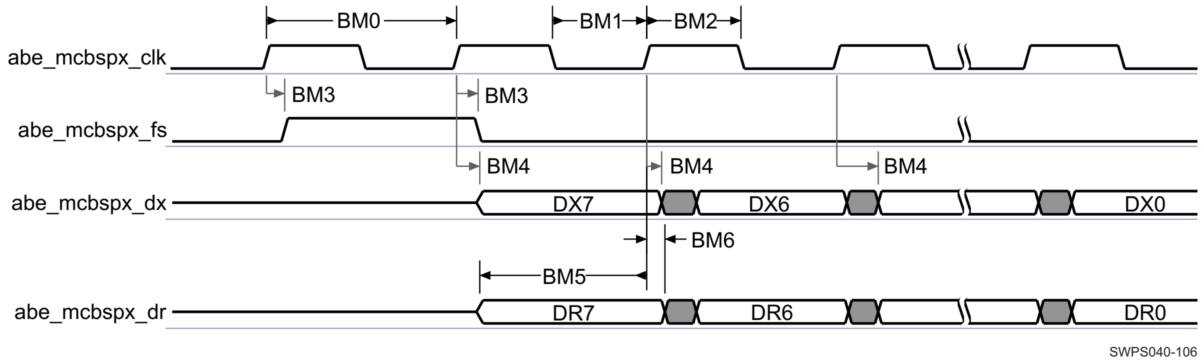

Figure 6-55. McBSP1, 2—I2S/PCM—Master Mode(1)(2)(3)(4)(5)(6)

(1) abe_mcbspx_clk corresponds to either abe_mcbspx_clkx or abe_mcbspx_clkr; abe_mcbspx_fs corresponds to either abe_mcbspx_fsx or abe_mcbspx_fsr.
McBSP in 6-pin mode: dx and dr as data pins; clkx, clkr, fsx, and fsr as control pins.
McBSP in 4-pin mode: dx and dr as data pins; clkx and fsx pins as control pins. The clkx and fsx pins are internally looped back, via software configuration, respectively to the clkr and fsr internal signals for data receive.

(2) The polarity of McBSP frame synchronization is software configurable.

(3) The active clock edge selection of abe_mcbspx_clk (rising or falling) on which abe_mcbspx_dx data is latched and abe_mcbspx_dr data is sampled is software configurable.

(4) Timing diagrams are for data delay set to 1.

(5) For more information regarding the registers configuration see the Serial Communication Interface / Multichannel Buffered Serial Port (McBSP) / MCBSP Register Manual / MCBSP Registers / MCBSP Register Summary Table section of the OMAP4430 TRM.

(6) In abe_mcbspx, x is equal to 1 or 2.

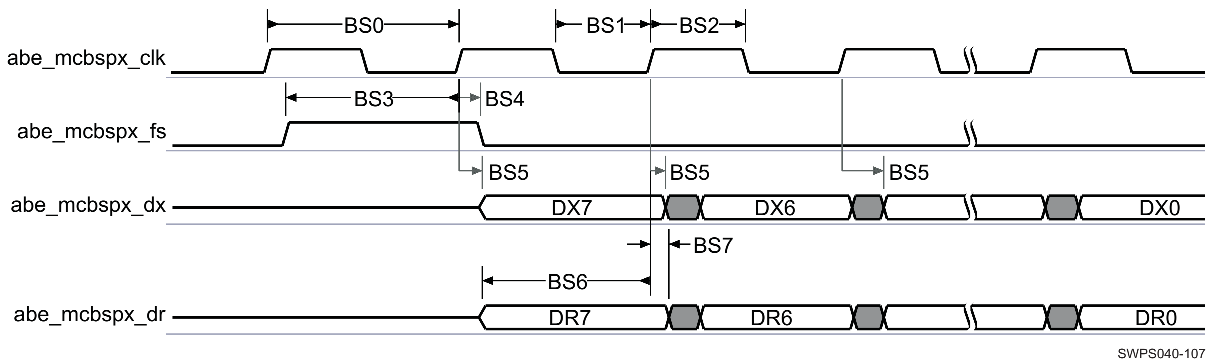

Figure 6-56. McBSP1, 2—I2S/PCM—Slave Mode(1)(2)(3)(4)(5)(6)

(1) abe_mcbspx_clk corresponds to either abe_mcbspx_clkx or abe_mcbspx_clkr; abe_mcbspx_fs corresponds to either abe_mcbspx_fsx or abe_mcbspx_fsr. McBSP in 6-pin mode: dx and dr as data pins; clkx, clkr, fsx, and fsr as control pins. McBSP in 4-pin mode: dx and dr as data pins; clkx and fsx pins as control pins. The clkx and fsx pins are internally looped back, via software configuration, respectively to the clkr and fsr internal signals for data receive.

(2) The polarity of McBSP frame synchronization is software configurable.

(3) The active clock edge selection of abe_mcbspx_clk (rising or falling) on which abe_mcbspx_dx data is latched and abe_mcbspx_dr data is sampled is software configurable.

(4) Timing diagrams are for data delay set to 1.

(5) For more information regarding the registers configuration see the Serial Communication Interface / Multichannel Buffered Serial Port (McBSP) / MCBSP Register Manual / MCBSP Registers / MCBSP Register Summary Table section of the OMAP4430 TRM.

(6) In abe_mcbspx, x is equal to 1 or 2.

6.6.1.1.2 McBSP1, McBSP2, and McBSP3 Set#1—TDM / Half-Cycle

6.6.1.1.2.1 McBSP1, McBSP2, and McBSP3 Set#1—TDM / Half-Cycle—6MHz, 40-pF Load Capacitance

Table 6-45 through Table 6-48 assume testing over the recommended operating conditions and electrical characteristic conditions below (see Figure 6-57 and Figure 6-58).

Table 6-44. McBSP1, McBSP2, and McBSP3 Set#1 Timing Conditions—TDM / Half-Cycle(1)(2)(3)

SYSTEM CONDITION PARAMETER		VALUE		UNIT
		MIN	MAX	
Input Conditions				
t_R	Input signal rise time	1000	11100	ps
t_F	Input signal fall time	1000	11100	ps
PCB Conditions				
	Number of external peripherals		1	
	Far end load		40	pF
	Trace length		9	cm
	Characteristics impedance	20	60	Ω

(1) IO settings: MB[1:0] = 10 and LB0 = 0 McBSP3 Set#1 means the following balls: AG25, AF25, AE25, AF26.
For more information, see Control Module / Control Module Functional Description/ Functional Register Description / Signal Integrity Parameter Control Registers with Pad Group Assignment / 50-Ω Output Buffer I/Os with Combined Mode and Load Settings section of the OMAP4430 TRM.

(2) In this table the rise and fall times are calculated for 10% to 90% of VDDS. For more information on the corresponding OMAP4 VDDS power supply name, see Table 2-1, POWER [9] column with the ball name.

(3) To have an idea of the output OMAP4 ball load supported for this application, you can consider the following:
Output OMAP4 ball load = Far End load + 1.34 pF/cm typical x trace length (cm).

6.6.1.1.2.1.1 McBSP1, McBSP2, and McBSP3 Set#1—TDM / Half-Cycle—Master Mode

Table 6-45. McBSP1, McBSP2, and McBSP3 Set#1 Timing Requirements—TDM / Half-Cycle—Master Mode(1)(3)(4)

NO.	PARAMETER		OPP100		OPP50		UNIT
			MIN	MAX	MIN	MAX	
BM5	$t_{su(drV-clkAE)}$	Setup time, abe_mcbspx_dr valid before abe_mcbspx_clk(2) active edge	22.6		48.6		ns
BM6	$t_{h(clkAE-drV)}$	Hold time, abe_mcbspx_dr valid after abe_mcbspx_clk(2) active edge	22.3		48.4		ns

(1) The timings apply to all configurations regardless of abe_mcbspx_clk polarity and which clock edges are used to drive output data and capture input data.

(2) abe_mcbspx_clk corresponds to either abe_mcbspx_clkx or abe_mcbspx_clkr; abe_mcbspx_clkr is available in 6-pin mode only.

(3) In abe_mcbspx, x is equal to 1, or 2, or 3 Set#1 (Balls: AG25, AF25, AE25, AF26).

(4) See DM Operating Condition Addendum for CORE OPP voltages.

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Table 6-46. McBSP1, McBSP2, and McBSP3 Set#1 Switching Characteristics—TDM / Half-Cycle—Master Mode(4)(7)(9)

NO.	PARAMETER		OPP100		OPP50		UNIT
			MIN	MAX	MIN	MAX	
BM0	$1 / t_{c(clk)}$	Frequency(1), output abe_mcbspx_clk(5) clock		6.144(8)		3.072(8)	MHz
BM1	$t_{w(clkL)}$	Typical pulse duration, output abe_mcbspx_clk(5) low	0.5*P(2)		0.5*P(2)		ns
BM2	$t_{w(clkH)}$	Typical pulse duration, output abe_mcbspx_clk(5) high	0.5*P(2)		0.5*P(2)		ns
	$t_{dc(clk)}$	Duty cycle error, output abe_mcbspx_clk(5)	–8138	8138	–16276	16276	ps
	$t_{j(clk)}$	Jitter standard deviation(3), output abe_mcbspx_clk(5)		65		65	ps
	$t_{R(clk)}$	Rise time, output abe_mcbspx_clk(5)	1000	11100	1000	11100	ps
	$t_{F(clk)}$	Fall time, output abe_mcbspx_clk(5)	1000	11100	1000	11100	ps
BM3	$t_{d(clkAE-fsV)}$	Delay time, output abe_mcbspx_clk(5) active edge to output abe_mcbspx_fs(6) valid	–30.9	46.4	–63.5	94.4	ns
BM4	$t_{d(clkxAE-dxV)}$	Delay time, output abe_mcbspx_clkx active edge to output abe_mcbspx_dx valid	–30.9	46.4	–63.5	94.4	ns
	$t_{R(fs)}$	Rise time, output abe_mcbspx_fs(6)	1000	11100	1000	11100	ps
	$t_{F(fs)}$	Fall time, output abe_mcbspx_fs(6)	1000	11100	1000	11100	ps
	$t_{R(dx)}$	Rise time, output abe_mcbspx_dx	1000	11100	1000	11100	ps
	$t_{F(dx)}$	Fall time, output abe_mcbspx_dx	1000	11100	1000	11100	ps

(1) Related to the output abe_mcbspx_clkx / abe_mcbspx_clkr maximum and minimum frequency programmable in McBSP module by setting the configuration register SRGR1_REG[7..0].
For more information regarding the registers configuration see the Serial Communication Interface / Multichannel Buffered Serial Port (McBSP) / MCBSP Register Manual / MCBSP Registers / MCBSP Register Summary Table section of the OMAP4430 TRM.

(2) P = abe_mcbspx_clkx / abe_mcbspx_clkr output clk period in ns

(3) The jitter probability density can be approximated by a Gaussian function.

(4) The timings apply to all configurations regardless of abe_mcbspx_clk polarity and which clock edges are used to drive output data and capture input data.

(5) abe_mcbspx_clk corresponds to either abe_mcbspx_clkx or abe_mcbspx_clkr; abe_mcbspx_clkr is available in 6-pin mode only.

(6) abe_mcbspx_fs corresponds to either abe_mcbspx_fsx or abe_mcbspx_fsr; abe_mcbspx_fsr is available in 6-pin mode only.

(7) In abe_mcbspx, x is equal to 1, 2, or 3 Set#1 (Balls: AG25, AF25, AE25, AF26).

(8) This McBSP1, 2 output clock frequency is based on an output ABE DPLL configured at 196.608 MHz.
For more information regarding the registers configuration, see the Power, Reset and Clock Management / Clock Management Functional Description / Internal Clock Sources/Generators / DPLL_ABE Description section of the OMAP4430 TRM.

(9) See DM Operating Condition Addendum for CORE OPP voltages.

6.6.1.1.2.1.2 McBSP1, McBSP2, and McBSP3 Set#1—TDM / Half-Cycle—Slave Mode

Table 6-47. McBSP1, 2, and 3 Set#1 Timing Requirements—TDM / Half-Cycle—Slave Mode(4)(5)(8)(9)

NO.	PARAMETER		OPP100		OPP50		UNIT
			MIN	MAX	MIN	MAX	
BS0	$1 / t_{c(clk)}$	Frequency(1), abe_mcbspx_clk(6)		6.144		3.072	MHz
BS1	$t_{w(clkL)}$	Typical pulse duration, abe_mcbspx_clk(6) low	0.5*P(2)		0.5*P(2)		ns
BS2	$t_{w(clkH)}$	Typical pulse duration, abe_mcbspx_clk(6) high	0.5*P(2)		0.5*P(2)		ns
	$t_{dc(clk)}$	Duty cycle error, abe_mcbspx_clk(6)	–8138	8138	–16276	16276	ps
	$t_{j(clk)}$	Cycle jitter(3), abe_mcbspx_clk(6)		2000		2000	ps
BS3	$t_{su(fsV-clkAE)}$	Setup time, abe_mcbspx_fs(7) valid before abe_mcbspx_clk(6) active edge	26.5		55.8		ns
BS4	$t_{h(clkAE-fsV)}$	Hold time, abe_mcbspx_fs(7) valid after abe_mcbspx_clk(6) active edge	26.5		55.8		ns

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Table 6-47. McBSP1, 2, and 3 Set#1 Timing Requirements—TDM / Half-Cycle—Slave Mode[(4)(5)(8)(9)] (continued)

NO.	PARAMETER		OPP100		OPP50		UNIT
			MIN	MAX	MIN	MAX	
BS6	$t_{su(drV-clkAE)}$	Setup time, abe_mcbspx_dr valid before abe_mcbspx_clk[(6)] active edge	26.5		55.8		ns
BS7	$t_{h(clkAE-drV)}$	Hold time, abe_mcbspx_dr valid after abe_mcbspx_clk[(6)] active edge	26.5		55.8		ns

(1) Related to the input maximum frequency supported by the McBSP module.
(2) P = abe_mcbspx_clkx / abe_mcbspx_clkr period in ns
(3) Maximum cycle jitter supported by abe_mcbspx_clkx / abe_mcbspx_clkr input clock.
(4) The timing requirements are assured for the cycle jitter and duty cycle error conditions specified.
(5) The timings apply to all configurations regardless of abe_mcbspx_clk polarity and which clock edges are used to drive output data and capture input data.
(6) abe_mcbspx_clk corresponds to either abe_mcbspx_clkx or abe_mcbspx_clkr; abe_mcbspx_clkr is available in 6-pin mode only.
(7) abe_mcbspx_fs corresponds to either abe_mcbspx_fsx or abe_mcbspx_fsr; abe_mcbspx_fsr is available in 6-pin mode only.
(8) In abe_mcbspx, x is equal to 1, 2, or 3 Set#1 (Balls: AG25, AF25, AE25, AF26).
(9) See DM Operating Condition Addendum for CORE OPP voltages.

Table 6-48. McBSP1, 2, and 3 Set#1 Switching Characteristics—TDM / Half-Cycle—Slave Mode[(1)(2)(3)]

NO.	PARAMETER		OPP100		OPP50		UNIT
			MIN	MAX	MIN	MAX	
BS5	$t_{d(clkxAE-dxV)}$	Delay time, input abe_mcbspx_clkx active edge to output abe_mcbspx_dx valid	–25.2	33.6	–57.7	74.3	ns
	$t_{R(dx)}$	Rise time, output abe_mcbspx_dx	1000	11100	1000	11100	ps
	$t_{F(dx)}$	Fall time, output abe_mcbspx_dx	1000	11100	1000	11100	ps

(1) The timings apply to all configurations regardless of abe_mcbspx_clk polarity and which clock edges are used to drive output data and capture input data.
(2) In abe_mcbspx, x is equal to 1, 2, or 3 Set #1 (Balls: AG25, AF25, AE25, AF26).
(3) See DM Operating Condition Addendum for CORE OPP voltages.

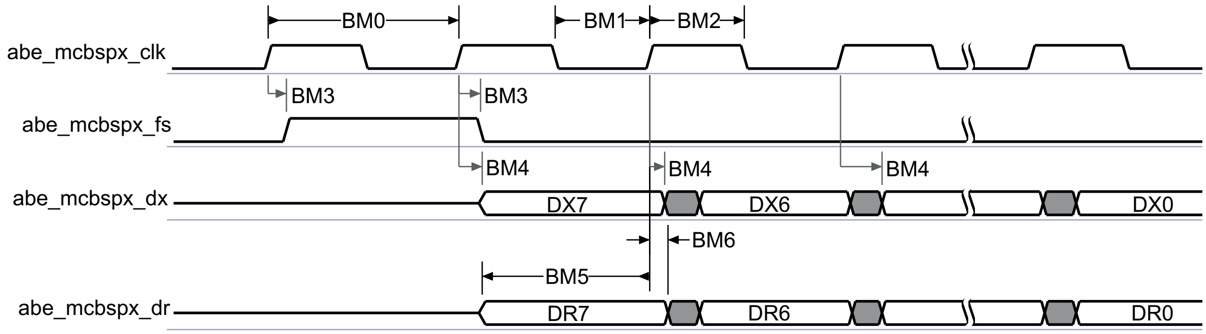

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Figure 6-57. McBSP1, 2, and 3 Set#1—TDM / Half-Cycle—Master Mode(1)(2)(3)(4)(5)(6)

(1) abe_mcbspx_clk corresponds to either abe_mcbspx_clkx or abe_mcbspx_clkr; abe_mcbspx_fs corresponds to either abe_mcbspx_fsx or abe_mcbspx_fsr.
McBSP in 6-pin mode: dx and dr as data pins; clkx, clkr, fsx, and fsr as control pins.
McBSP in 4-pin mode: dx and dr as data pins; clkx and fsx pins as control pins. The clkx and fsx pins are internally looped back, via software configuration, respectively to the clkr and fsr internal signals for data receive.

(2) The polarity of McBSP frame synchronization is software configurable.

(3) The active clock edge selection of abe_mcbspx_clk (rising or falling) on which abe_mcbspx_dx data is latched and abe_mcbspx_dr data is sampled is software configurable.

(4) Timing diagrams are for data delay set to 1.

(5) For more information regarding the registers configuration see the Serial Communication Interface / Multichannel Buffered Serial Port (McBSP) / MCBSP Register Manual / MCBSP Registers / MCBSP Register Summary Table section of the OMAP4430 TRM.

(6) In abe_mcbspx, x is equal to 1, 2, or 3 Set#1 (Balls: AG25, AF25, AE25, AF26).

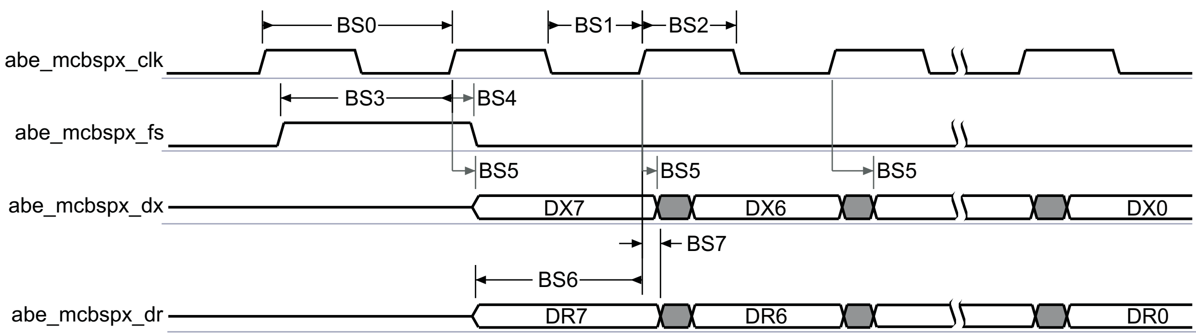

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Figure 6-58. McBSP1, 2, and 3 Set#1—TDM / Half-Cycle—Slave Mode(1)(2)(3)(4)(5)(6)

(1) abe_mcbspx_clk corresponds to either abe_mcbspx_clkx or abe_mcbspx_clkr; abe_mcbspx_fs corresponds to either abe_mcbspx_fsx or abe_mcbspx_fsr.
McBSP in 6-pin mode: dx and dr as data pins; clkx, clkr, fsx, and fsr as control pins.
McBSP in 4-pin mode: dx and dr as data pins; clkx and fsx pins as control pins. The clkx and fsx pins are internally looped back, via software configuration, respectively to the clkr and fsr internal signals for data receive.

(2) The polarity of McBSP frame synchronization is software configurable.

(3) The active clock edge selection of abe_mcbspx_clk (rising or falling) on which abe_mcbspx_dx data is latched and abe_mcbspx_dr data is sampled is software configurable.

(4) Timing diagrams are for data delay set to 1.

(5) For more information regarding the registers configuration see the Serial Communication Interface / Multichannel Buffered Serial Port (McBSP) / MCBSP Register Manual / MCBSP Registers / MCBSP Register Summary Table section of the OMAP4430 TRM.

(6) In abe_mcbspx, x is equal to 1, 2, or 3 Set#1 (Balls: AG25, AF25, AE25, AF26).

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6.6.1.1.2.2 McBSP1, McBSP2, and McBSP3 Set#1—TDM / Half-Cycle—12MHz, 5-pF Load Capacitance

Table 6-50 through Table 6-53 assume testing over the recommended operating conditions and electrical characteristic conditions below (see Figure 6-59 and Figure 6-60).

Table 6-49. McBSP1, McBSP2, and McBSP3 Set#1 Timing Conditions—TDM / Half-Cycle(1)(2)(3)

SYSTEM CONDITION PARAMETER		VALUE		UNIT
		MIN	MAX	
Input Conditions				
t_R	Input signal rise time	600	6500	ps
t_F	Input signal fall time	600	6500	ps
PCB Conditions				
	Number of external peripherals		1	
	Far end load		5	pF
	Trace length		9	cm
	Characteristics impedance	20	60	Ω

(1) IO settings: MB[1:0] = 10 and LB0 = 0 McBSP3 Set#1 means the following balls: AG25, AF25, AE25, AF26. For more information, see Control Module / Control Module Functional Description/ Functional Register Description / Signal Integrity Parameter Control Registers with Pad Group Assignment / 50-Ω Output Buffer I/Os with Combined Mode and Load Settings section of the OMAP4430 TRM.

(2) In this table the rise and fall times are calculated for 10% to 90% of VDDS. For more information on the corresponding OMAP4 VDDS power supply name, see Table 2-1, POWER [9] column with the ball name.

(3) To have an idea of the output OMAP4 ball load supported for this application, you can consider the following: Output OMAP4 ball load = Far End load + 1.34 pF/cm typical x trace length (cm).

6.6.1.1.2.2.1 McBSP1, McBSP2, and McBSP3 Set#1—TDM / Half-Cycle—Master Mode

Table 6-50. McBSP1, McBSP2, and McBSP3 Set#1 Timing Requirements—TDM / Half-Cycle—Master Mode(1)(3)(4)

NO.	PARAMETER		OPP100		OPP50		UNIT
			MIN	MAX	MIN	MAX	
BM5	$t_{su(drV-clkAE)}$	Setup time, abe_mcbspx_dr valid before abe_mcbspx_clk(2) active edge	11.3		24.3		ns
BM6	$t_{h(clkAE-drV)}$	Hold time, abe_mcbspx_dr valid after abe_mcbspx_clk(2) active edge	–2.4		–2.4		ns

(1) The timings apply to all configurations regardless of abe_mcbspx_clk polarity and which clock edges are used to drive output data and capture input data.

(2) abe_mcbspx_clk corresponds to either abe_mcbspx_clkx or abe_mcbspx_clkr; abe_mcbspx_clkr is available in 6-pin mode only.

(3) In abe_mcbspx, x is equal to 1, or 2, or 3 Set#1 (Balls: AG25, AF25, AE25, AF26).

(4) See DM Operating Condition Addendum for CORE OPP voltages.

Table 6-51. McBSP1, McBSP2, and McBSP3 Set#1 Switching Characteristics—TDM / Half-Cycle—Master Mode[(4)(7)(9)]

NO.	PARAMETER		OPP100		OPP50		UNIT
			MIN	MAX	MIN	MAX	
BM0	1 / $t_{c(clk)}$	Frequency[(1)], output abe_mcbspx_clk[(5)] clock		12.288[(8)]		6.144[(8)]	MHz
BM1	$t_{w(clkL)}$	Typical Pulse duration, output abe_mcbspx_clk[(5)] low	0.5*P[(2)]		0.5*P[(2)]		ns
BM2	$t_{w(clkH)}$	Typical Pulse duration, output abe_mcbspx_clk[(5)] high	0.5*P[(2)]		0.5*P[(2)]		ns
	$t_{dc(clk)}$	Duty cycle error, output abe_mcbspx_clk[(5)]	–4069	4069	–8138	8138	ps
	$t_{J(clk)}$	Jitter standard deviation[(3)], output abe_mcbspx_clk[(5)]		65		65	ps
	$t_{R(clk)}$	Rise time, output abe_mcbspx_clk[(5)]	600	6500	600	6500	ps
	$t_{F(clk)}$	Fall time, output abe_mcbspx_clk[(5)]	600	6500	600	6500	ps
BM3	$t_{d(clkAE-fsV)}$	Delay time, output abe_mcbspx_clk[(5)] active edge to output abe_mcbspx_fs[(6)] valid	–14.6	22.4	–30.9	46.4	ns
BM4	$t_{d(clkxAE-dxV)}$	Delay time, output abe_mcbspx_clkx active edge to output abe_mcbspx_dx valid	–14.6	22.4	–30.9	46.4	ns
	$t_{R(fs)}$	Rise time, output abe_mcbspx_fs[(6)]	600	6500	600	6500	ps
	$t_{F(fs)}$	Fall time, output abe_mcbspx_fs[(6)]	600	6500	600	6500	ps
	$t_{R(dx)}$	Rise time, output abe_mcbspx_dx	600	6500	600	6500	ps
	$t_{F(dx)}$	Fall time, output abe_mcbspx_dx	600	6500	600	6500	ps

(1) Related to the output abe_mcbspx_clkx / abe_mcbspx_clkr maximum and minimum frequency programmable in McBSP module by setting the configuration register SRGR1_REG[7..0].
For more information regarding the registers configuration see Serial Communication Interface / Multichannel Buffered Serial Port (McBSP) MCBSP Register Manual / MCBSP Registers / MCBSP Register Summary Table section of the OMAP4430 TRM.

(2) P = abe_mcbspx_clkx / abe_mcbspx_clkr output clk period in ns

(3) The jitter probability density can be approximated by a Gaussian function.

(4) The timings apply to all configurations regardless of abe_mcbsp_clk polarity and which clock edges are used to drive output data and capture input data.

(5) abe_mcbspx_clk corresponds to either abe_mcbspx_clkx or abe_mcbspx_clkr; abe_mcbspx_clkr is available in 6-pin mode only.

(6) abe_mcbspx_fs corresponds to either abe_mcbspx_fsx or abe_mcbspx_fsr; abe_mcbspx_fsr is available in 6-pin mode only.

(7) In abe_mcbspx, x is equal to 1, or 2, or 3 Set#1 (Balls: AG25, AF25, AE25, AF26).

(8) This McBSP1, 2 output clock frequency is based on an output ABE DPLL configured at 196.608 MHz.
For more information regarding the registers configuration, see Power, Reset and Clock Management / Clock Management Functional Description / Internal Clock Sources/Generators / DPLL_ABE Description section of the OMAP4430 TRM.

(9) See DM Operating Condition Addendum for CORE OPP voltages.

6.6.1.1.2.2.2 McBSP1, McBSP2, and McBSP3 Set#1—TDM / Half-Cycle—Slave Mode

Table 6-52. McBSP1, McBSP2, and McBSP3 Set#1 Timing Requirements—TDM / Half-Cycle—Slave Mode[(5)(8)(9)]

NO.	PARAMETER		OPP100		OPP50		UNIT
			MIN	MAX	MIN	MAX	
BS0	1 / $t_{c(clk)}$	Frequency[(1)], abe_mcbspx_clk[(6)]		12.288		6.144	MHz
BS1	$t_{w(clkL)}$	Typical Pulse duration, abe_mcbspx_clk[(6)] low	0.5*P[(2)]		0.5*P[(2)]		ns
BS2	$t_{w(clkH)}$	Typical Pulse duration, abe_mcbspx_clk[(6)] high	0.5*P[(2)]		0.5*P[(2)]		ns
	$t_{dc(clk)}$	Duty cycle error, abe_mcbspx_clk[(6)]	–4069	4069	–8138	8138	ps
	$t_{J(clk)}$	Cycle jitter[(3)], abe_mcbspx_clk[(6)]		2000		2000	ps
BS3	$t_{su(fsV-clkAE)}$	Setup time, abe_mcbspx_fs[(7)] valid before abe_mcbspx_clk[(6)] active edge	11.9		26.5		ns
BS4	$t_{h(clkAE-fsV)}$	Hold time, abe_mcbspx_fs[(7)] valid after abe_mcbspx_clk[(6)] active edge	11.9		26.5		ns

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Table 6-52. McBSP1, McBSP2, and McBSP3 Set#1 Timing Requirements—TDM / Half-Cycle—Slave Mode(5)(8)(9) (continued)

NO.	PARAMETER		OPP100		OPP50		UNIT
			MIN	MAX	MIN	MAX	
BS6	$t_{su(drV-clkAE)}$	Setup time, abe_mcbspx_dr valid before abe_mcbspx_clk(6) active edge	9.4		21.6		ns
BS7	$t_{h(clkAE-drV)}$	Hold time, abe_mcbspx_dr valid after abe_mcbspx_clk(6) active edge	11.9		26.5		ns

(1) Related to the input maximum frequency supported by the McBSP module.
(2) P = abe_mcbspx_clkx / abe_mcbspx_clkr period in ns
(3) Maximum cycle jitter supported by abe_mcbspx_clkx / abe_mcbspx_clkr input clock.
(4) The timing requirements are assured for the cycle jitter and duty cycle error conditions specified.
(5) The timings apply to all configurations regardless of abe_mcbspx_clk polarity and which clock edges are used to drive output data and capture input data.
(6) abe_mcbspx_clk corresponds to either abe_mcbspx_clkx or abe_mcbspx_clkr; abe_mcbspx_clkr is available in 6-pin mode only.
(7) abe_mcbspx_fs corresponds to either abe_mcbspx_fsx or abe_mcbspx_fsr; abe_mcbspx_fsr is available in 6-pin mode only.
(8) In abe_mcbspx, x is equal to 1, or 2, or 3 Set#1 (Balls: AG25, AF25, AE25, AF26).
(9) See DM Operating Condition Addendum for CORE OPP voltages.

Table 6-53. McBSP1, 2, and 3 Set#1 Switching Characteristics—TDM / Half-Cycle—Slave Mode(1)(2)(3)

NO.	PARAMETER		OPP100		OPP50		UNIT
			MIN	MAX	MIN	MAX	
BS5	$t_{d(clkxAE-dxV)}$	Delay time, input abe_mcbspx_clkx active edge to output abe_mcbspx_dx valid	–7.1	20.3	–23.4	43.0	ns
	$t_{R(dx)}$	Rise time, output abe_mcbspx_dx	600	6500	600	6500	ps
	$t_{F(dx)}$	Fall time, output abe_mcbspx_dx	600	6500	600	6500	ps

(1) The timings apply to all configurations regardless of mcbsp_clk polarity and which clock edges are used to drive output data and capture input data.
(2) In abe_mcbspx, x is equal to 1, or 2, or 3 Set#1 (Balls: AG25, AF25, AE25, AF26).
(3) See DM Operating Condition Addendum for CORE OPP voltages.

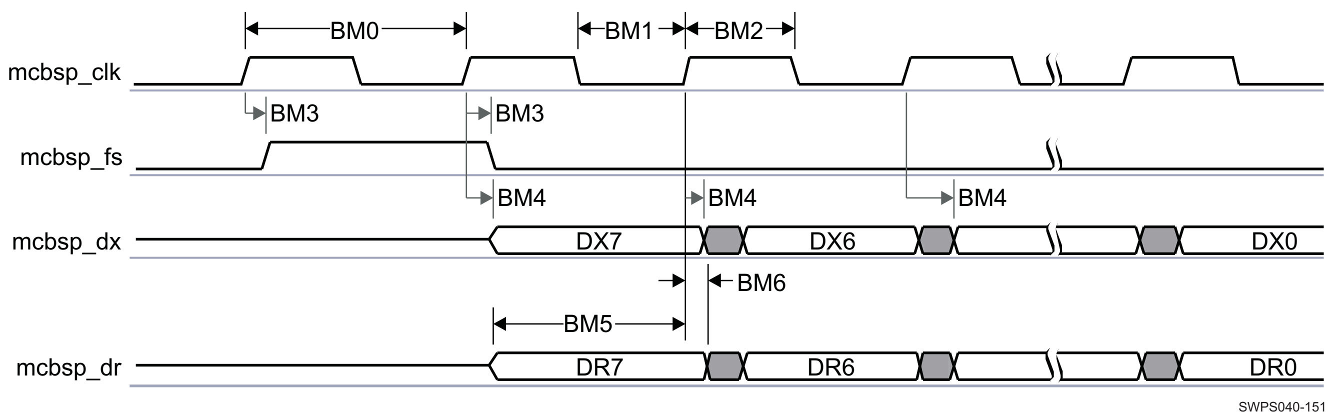

Figure 6-59. McBSP1, 2, and 3 Set#1—TDM / Half-Cycle—Master Mode(1)(2)(3)(4)(5)(6)

(1) abe_mcbspx_clk corresponds to either abe_mcbspx_clkx or abe_mcbspx_clkr; abe_mcbspx_fs corresponds to either abe_mcbspx_fsx or abe_mcbspx_fsr.
McBSP in 6-pin mode: dx and dr as data pins; clkx, clkr, fsx, and fsr as control pins.
McBSP in 4-pin mode: dx and dr as data pins; clkx and fsx pins as control pins. The clkx and fsx pins are internally looped back, via software configuration, respectively to the clkr and fsr internal signals for data receive.
(2) The polarity of McBSP frame synchronization is software configurable.
(3) The active clock edge selection of abe_mcbspx_clk (rising or falling) on which abe_mcbspx_dx data is latched and abe_mcbspx_dr data is sampled is software configurable.

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(4) Timing diagrams are for data delay set to 1.

(5) For more information regarding the registers configuration see Serial Communication Interface / Multichannel Buffered Serial Port (McBSP) MCBSP Register Manual / MCBSP Registers / MCBSP Register Summary Table section of the OMAP4430 TRM.

(6) In abe_mcbspx, x is equal to 1, or 2, or 3 Set#1 (Balls: AG25, AF25, AE25, AF26).

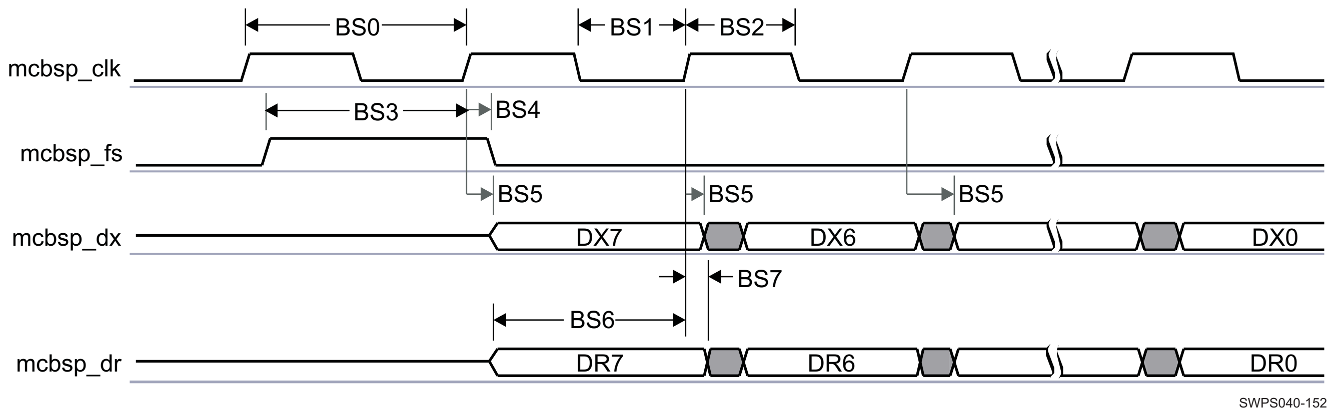

Figure 6-60. McBSP1, 2, and 3 Set#1—TDM / Half-Cycle—Slave Mode(1)(2)(3)(4)(5)(6)

(1) abe_mcbspx_clk corresponds to either abe_mcbspx_clkx or abe_mcbspx_clkr; abe_mcbspx_fs corresponds to either abe_mcbspx_fsx or abe_mcbspx_fsr.
McBSP in 6-pin mode: dx and dr as data pins; clkx, clkr, fsx, and fsr as control pins.
McBSP in 4-pin mode: dx and dr as data pins; clkx and fsx pins as control pins. The clkx and fsx pins are internally looped back, via software configuration, respectively to the clkr and fsr internal signals for data receive.

(2) The polarity of McBSP frame synchronization is software configurable.

(3) The active clock edge selection of abe_mcbspx_clk (rising or falling) on which abe_mcbspx_dx data is latched and abe_mcbspx_dr data is sampled is software configurable.

(4) Timing diagrams are for data delay set to 1.

(5) For more information regarding the registers configuration see Serial Communication Interface / Multichannel Buffered Serial Port (McBSP) MCBSP Register Manual / MCBSP Registers / MCBSP Register Summary Table section of the OMAP4430 TRM.

(6) In abe_mcbspx, x is equal to 1, or 2, or 3 Set#1 (Balls: AG25, AF25, AE25, AF26).

6.6.1.2 McBSP3—I2S/PCM

Table 6-55 through Table 6-58 assume testing over the recommended operating conditions and electrical characteristic conditions below (see Figure 6-61 and Figure 6-62).

Table 6-54. McBSP3 Timing Conditions—I2S/PCM(1)(2)(3)

SYSTEM CONDITION PARAMETER		VALUE		UNIT
		MIN	MAX	
Input Conditions				
t_R	Input signal rise time	400	6500	ps
t_F	Input signal fall time	400	6500	ps
PCB Conditions				
Bottom Balls: AG25 / AF25 / AE25 / AF26				
	Number of external peripherals		1	
	Far end load		5	pF
	Trace length, point-to-point interconnect		9	cm
	Characteristics impedance	30	55	Ω
Bottom Balls: AH17 / AE16 / AF16 / AG16				
	Number of external peripherals		1	
	Far end load		5	pF
	Trace length, point-to-point interconnect		9	cm

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Table 6-54. McBSP3 Timing Conditions—I2S/PCM(1)(2)(3) (continued)

SYSTEM CONDITION PARAMETER		VALUE		UNIT
		MIN	MAX	
	Characteristics impedance	30	45	Ω

(1) IO settings: MB[1:0] = 10 and LB0 = 0.
For more information, see:
- For balls AG25 / AF25 / AE25 / AF26, Control Module / Control Module Functional Description/ Functional Register Description / Signal Integrity Parameter Control Registers with Pad Group Assignment / 50-Ω Output Buffer I/Os with Combined Mode and Load Settings section of the OMAP4430 TRM
- For balls AH17 / AE16 / AF16 / AG16, Control Module / Control Module Functional Description/ Functional Register Description / Signal Integrity Parameter Control Registers with Pad Group Assignment / I/Os with Combined Mode and Load Settings section of the OMAP4430 TRM.

(2) In this table the rise and fall times are calculated for 10% to 90% of VDDS. For more information on the corresponding OMAP4 VDDS power supply name, see Table 2-1, POWER [9] column with the ball name.

(3) To have an idea of the output OMAP4 ball load supported for this application, you can consider the following:
Output OMAP4 ball load = Far End load + 1.34 pF/cm typical x trace length (cm).

6.6.1.2.1 McBSP3—I2S/PCM Full and Half Cycle—Master Mode—24 MHz

Table 6-55. McBSP3 Timing Requirements—I2S/PCM—Master Mode(1)(3)

NO.	PARAMETER		OPP100		OPP50		UNIT
			MIN	MAX	MIN	MAX	
For balls: AH17 / AE16 / AF16 / AG16 (abe_mcbsp3_dr / abe_mcbsp3_dx / abe_mcbsp3_clkx / abe_mcbsp3_fsx)—Multiplexing mode 2							
BM5	$t_{su(drV-clkAE)}$	Setup time, abe_mcbsp3_dr valid before abe_mcbsp3_clk(2) active edge	5.6		11.5		ns
BM6	$t_{h(clkAE-drV)}$	Hold time, abe_mcbsp3_dr valid after abe_mcbsp3_clk(2) active edge	0.8		0.7		ns
For balls: AG25 / AF25 / AE25 / AF26 (abe_mcbsp3_dr / abe_mcbsp3_dx / abe_mcbsp3_clkx / abe_mcbsp3_fsx)—Multiplexing mode 1							
BM5	$t_{su(drV-clkAE)}$	Setup time, abe_mcbsp3_dr valid before abe_mcbsp3_clk(2) active edge	4.6		10.5		ns
BM6	$t_{h(clkAE-drV)}$	Hold time, abe_mcbsp3_dr valid after abe_mcbsp3_clk(2) active edge	0.7		0.6		ns

(1) The timings apply to all configurations regardless of abe_mcbsp3_clk polarity and which clock edges are used to drive output data and capture input data.

(2) abe_mcbsp3_clk corresponds to either abe_mcbsp3_clkx or abe_mcbsp3_clkr; abe_mcbsp3_clkr is available in 6-pin mode only.

(3) See DM Operating Condition Addendum for CORE OPP voltages.

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Table 6-56. McBSP3 Switching Characteristics—I2S/PCM—Master Mode[(4)][(8)]

NO.	PARAMETER		OPP100		OPP50		UNIT
			MIN	MAX	MIN	MAX	
For balls: AE16 / AF16 / AG16 (abe_mcbsp3_dx / abe_mcbsp3_clkx / abe_mcbsp3_fsx)—Multiplexing mode 2							
BM0	$1 / t_{c(clk)}$	Frequency[(1)], output abe_mcbsp3_clk[(5)] clock		24.576[(7)]		12.288[(7)]	MHz
BM1	$t_{w(clkL)}$	Typical pulse duration, output abe_mcbsp3_clk[(5)] low	0.5*P[(2)]		0.5*P[(2)]		ns
BM2	$t_{w(clkH)}$	Typical pulse duration, output abe_mcbsp3_clk[(5)] high	0.5*P[(2)]		0.5*P[(2)]		ns
	$t_{dc(clk)}$	Duty cycle error, output abe_mcbsp3_clk[(5)]	–2035	2035	–4069	4069	ps
	$t_{j(clk)}$	Jitter standard deviation[(3)], output abe_mcbsp3_clk[(5)]		65		65	ps
	$t_{R(clk)}$	Rise time, output abe_mcbsp3_clk[(5)]	400	6500	400	6500	ps
	$t_{F(clk)}$	Fall time, output abe_mcbsp3_clk[(5)]	400	6500	400	6500	ps
BM3	$t_{d(clkAE-fsV)}$	Delay time, output abe_mcbsp3_clk[(5)] active edge to output abe_mcbsp3_fs[(6)] valid	0.9	11.4	1.1	23.1	ns
BM4	$t_{d(clkxAE-dxV)}$	Delay time, output abe_mcbsp3_clkx active edge to output abe_mcbsp3_dx valid	0.9	11.4	1.1	23.1	ns
	$t_{R(fs)}$	Rise time, output abe_mcbsp3_fs[(6)]	400	6500	400	6500	ps
	$t_{F(fs)}$	Fall time, output abe_mcbsp3_fs[(6)]	400	6500	400	6500	ps
	$t_{R(dx)}$	Rise time, output abe_mcbsp3_dx	400	6500	400	6500	ps
	$t_{F(dx)}$	Fall time, output abe_mcbsp3_dx	400	6500	400	6500	ps
For balls: AF25 / AE25 / AF26 (abe_mcbsp3_dx / abe_mcbsp3_clkx / abe_mcbsp3_fsx)—Multiplexing mode 1							
BM0	$1 / t_{c(clk)}$	Frequency[(1)], output abe_mcbsp3_clk[(5)] clock		24.576[(7)]		12.288[(7)]	MHz
BM1	$t_{w(clkL)}$	Typical pulse duration, output abe_mcbsp3_clk[(5)] low	0.5*P[(2)]		0.5*P[(2)]		ns
BM2	$t_{w(clkH)}$	Typical pulse duration, output abe_mcbsp3_clk[(5)] high	0.5*P[(2)]		0.5*P[(2)]		ns
	$t_{dc(clk)}$	Duty cycle error, output abe_mcbsp3_clk[(5)]	–2035	2035	–4069	4069	ps
	$t_{j(clk)}$	Jitter standard deviation[(3)], output abe_mcbsp3_clk[(5)]		65		65	ps
	$t_{R(clk)}$	Rise time, output abe_mcbsp3_clk[(5)]	400	6500	400	6500	ps
	$t_{F(clk)}$	Fall time, output abe_mcbsp3_clk[(5)]	400	6500	400	6500	ps
BM3	$t_{d(clkAE-fsV)}$	Delay time, output abe_mcbsp3_clk[(5)] active edge to output abe_mcbsp3_fs[(6)] valid	0.9	11.0	1.0	22.6	ns
BM4	$t_{d(clkxAE-dxV)}$	Delay time, output abe_mcbsp3_clkx active edge to output abe_mcbsp3_dx valid	0.9	11.0	1.0	22.6	ns
	$t_{R(fs)}$	Rise time, output abe_mcbsp3_fs[(6)]	400	6500	400	6500	ps
	$t_{F(fs)}$	Fall time, output abe_mcbsp3_fs[(6)]	400	6500	400	6500	ps
	$t_{R(dx)}$	Rise time, output abe_mcbsp3_dx	400	6500	400	6500	ps
	$t_{F(dx)}$	Fall time, output abe_mcbsp3_dx	400	6500	400	6500	ps

(1) Related to the output abe_mcbsp3_clkx / abe_mcbsp3_clkr maximum and minimum frequency programmable in McBSP module by setting the configuration register SRGR1_REG[7..0].
For more information regarding the registers configuration see the Serial Communication Interface / Multichannel Buffered Serial Port (McBSP) / MCBSP Register Manual / MCBSP Registers / MCBSP Register Summary Table section of the OMAP4430 TRM.

(2) P = abe_mcbsp3_clkx / abe_mcbsp3_clkr output clk period in ns

(3) The jitter probability density can be approximated by a Gaussian function.

(4) The timings apply to all configurations regardless of abe_mcbsp3_clk polarity and which clock edges are used to drive output data and capture input data.

(5) abe_mcbsp3_clk corresponds to either abe_mcbsp3_clkx or abe_mcbsp3_clkr; abe_mcbsp3_clkr is available in 6-pin mode only.

(6) abe_mcbsp3_fs corresponds to either abe_mcbsp3_fsx or abe_mcbsp3_fsr; abe_mcbsp3_fsr is available in 6-pin mode only.

(7) This McBSP3 output clock frequency is based on an output ABE DPLL configured at 196.608 MHz.
For more information regarding the registers configuration, see the Power, Reset and Clock Management / Clock Management Functional Description / Internal Clock Sources/Generators / DPLL_ABE Description section of the OMAP4430 TRM

(8) See DM Operating Condition Addendum for CORE OPP voltages.

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6.6.1.2.2 McBSP3—I2S/PCM Full and Half Cycle—Slave Mode—12 MHz

Table 6-57. McBSP3 Timing Requirements—I2S/PCM—Slave Mode[(4)(5)(8)]

NO.	PARAMETER		OPP100		OPP50		UNIT
			MIN	MAX	MIN	MAX	
For balls: AH17 / AE16 / AF16 / AG16 (abe_mcbsp3_dr / abe_mcbsp3_dx / abe_mcbsp3_clkx / abe_mcbsp3_fsx)—Multiplexing mode 2							
BS0	$1 / t_{c(clk)}$	Frequency[(1)], abe_mcbsp3_clk[(6)]		12.288		6.144	MHz
BS1	$t_{w(clkL)}$	Typical pulse duration, abe_mcbsp3_clk[(6)] low	0.5*P[(2)]		0.5*P[(2)]		ns
BS2	$t_{w(clkH)}$	Typical pulse duration, abe_mcbsp3_clk[(6)] high	0.5*P[(2)]		0.5*P[(2)]		ns
	$t_{dc(clk)}$	Duty cycle error, abe_mcbsp3_clk[(6)]	–2035	2035	–4069	4069	ps
	$t_{j(clk)}$	Cycle jitter[(3)], abe_mcbsp3_clk[(6)]		1221		2000	ps
BS3	$t_{su(fsV-clkAE)}$	Setup time, abe_mcbsp3_fs[(7)] valid before abe_mcbsp3_clk[(6)] active edge	14.8		30.8		ns
BS4	$t_{h(clkAE-fsV)}$	Hold time, abe_mcbsp3_fs[(7)] valid after abe_mcbsp3_clk[(6)] active edge	14.8		30.8		ns
BS6	$t_{su(drV-clkAE)}$	Setup time, abe_mcbsp3_dr valid before abe_mcbsp3_clk[(6)] active edge	14.8		30.8		ns
BS7	$t_{h(clkAE-drV)}$	Hold time, abe_mcbsp3_dr valid after abe_mcbsp3_clk[(6)] active edge	14.8		30.8		ns
For balls: AG25 / AF25 / AE25 / AF26 (abe_mcbsp3_dr / abe_mcbsp3_dx / abe_mcbsp3_clkx / abe_mcbsp3_fsx)—Multiplexing mode 1							
BS0	$1 / t_{c(clk)}$	Frequency[(1)], abe_mcbsp3_clk[(6)]		12.288		6.144	MHz
BS1	$t_{w(clkL)}$	Typical pulse duration, abe_mcbsp3_clk[(6)] low	0.5*P[(2)]		0.5*P[(2)]		ns
BS2	$t_{w(clkH)}$	Typical pulse duration, abe_mcbsp3_clk[(6)] high	0.5*P[(2)]		0.5*P[(2)]		ns
	$t_{dc(clk)}$	Duty cycle error, abe_mcbsp3_clk[(6)]	–2035	2035	–4069	4069	ps
	$t_{j(clk)}$	Cycle jitter[(3)], abe_mcbsp3_clk[(6)]		1221		2000	ps
BS3	$t_{su(fsV-clkAE)}$	Setup time, abe_mcbsp3_fs[(7)] valid before abe_mcbsp3_clk[(6)] active edge	14.3		30.4		ns
BS4	$t_{h(clkAE-fsV)}$	Hold time, abe_mcbsp3_fs[(7)] valid after abe_mcbsp3_clk[(6)] active edge	14.3		30.4		ns
BS6	$t_{su(drV-clkAE)}$	Setup time, abe_mcbsp3_dr valid before abe_mcbsp3_clk[(6)] active edge	14.3		30.4		ns
BS7	$t_{h(clkAE-drV)}$	Hold time, abe_mcbsp3_dr valid after abe_mcbsp3_clk[(6)] active edge	14.3		30.4		ns

(1) Related to the input maximum frequency supported by the McBSP module.
(2) P = abe_mcbsp3_clkx / abe_mcbsp3_clkr period in ns
(3) Maximum cycle jitter supported by abe_mcbsp3_clkx / abe_mcbsp3_clkr input clock.
(4) The timing requirements are assured for the cycle jitter and duty cycle error conditions specified.
(5) The timings apply to all configurations regardless of abe_mcbsp3_clk polarity and which clock edges are used to drive output data and capture input data.
(6) abe_mcbsp3_clk corresponds to either abe_mcbsp3_clkx or abe_mcbsp3_clkr; abe_mcbsp3_clkr is available in 6-pin mode only.
(7) abe_mcbsp3_fs corresponds to either abe_mcbsp3_fsx or abe_mcbsp3_fsr; abe_mcbsp3_fsr is available in 6-pin mode only.
(8) See DM Operating Condition Addendum for CORE OPP voltages.

Table 6-58. McBSP3 Switching Characteristics—I2S/PCM—Slave Mode(1)(2)

NO.	PARAMETER		OPP100		OPP50		UNIT
			MIN	MAX	MIN	MAX	
For balls: AE16 / AF16 / AG16 (abe_mcbsp3_dx / abe_mcbsp3_clkx / abe_mcbsp3_fsx)—Multiplexing mode 2							
BS5	$t_{d(clkxAE-dxV)}$	Delay time, input abe_mcbsp3_clkx active edge to output abe_mcbsp3_dx valid	–16.4	22.3	–34.1	38.1	ns
	$t_{R(dx)}$	Rise time, output abe_mcbsp3_dx	400	6500	400	6500	ps
	$t_{F(dx)}$	Fall time, output abe_mcbsp3_dx	400	6500	400	6500	ps
For balls: AF25 / AE25 / AF26 (abe_mcbsp3_dx / abe_mcbsp3_clkx / abe_mcbsp3_fsx)—Multiplexing mode 1							
BS5	$t_{d(clkxAE-dxV)}$	Delay time, input abe_mcbsp3_clkx active edge to output abe_mcbsp3_dx valid	–16.4	20.3	–34.0	36.1	ns
	$t_{R(dx)}$	Rise time, output abe_mcbsp3_dx	400	6500	400	6500	ps
	$t_{F(dx)}$	Fall time, output abe_mcbsp3_dx	400	6500	400	6500	ps

(1) The timings apply to all configurations regardless of abe_mcbsp3_clk polarity and which clock edges are used to drive output data and capture input data.

(2) See DM Operating Condition Addendum for CORE OPP voltages.

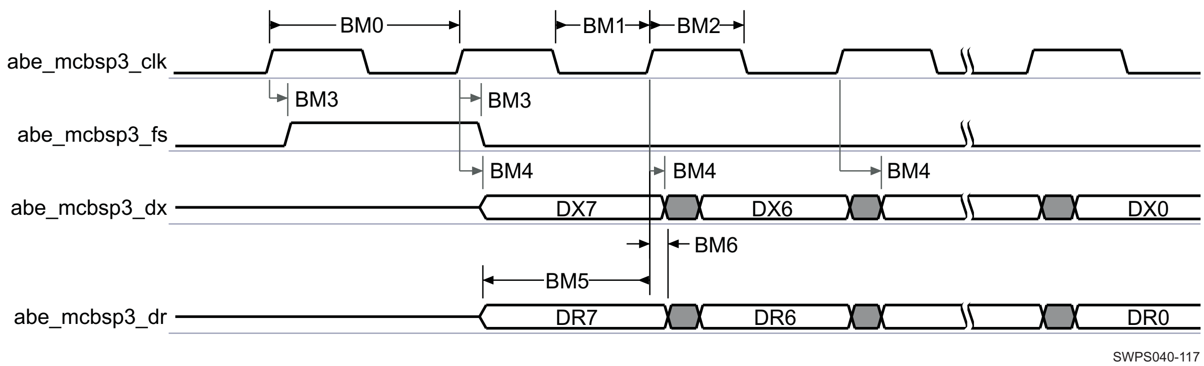

Figure 6-61. McBSP3—I2S/PCM—Master Mode(1)(2)(3)(4)(5)

(1) abe_mcbsp3_clk corresponds to either abe_mcbsp3_clkx or abe_mcbsp3_clkr; abe_mcbsp3_fs corresponds to either abe_mcbsp3_fsx or abe_mcbsp3_fsr.
McBSP in 6-pin mode: dx and dr as data pins; clkx, clkr, fsx, and fsr as control pins.
McBSP in 4-pin mode: dx and dr as data pins; clkx and fsx pins as control pins. The clkx and fsx pins are internally looped back, via software configuration, respectively to the clkr and fsr internal signals for data receive.

(2) The polarity of McBSP frame synchronization is software configurable.

(3) The active clock edge selection of abe_mcbsp3_clk (rising or falling) on which abe_mcbsp3_dx data is latched and abe_mcbsp3_dr data is sampled is software configurable.

(4) Timing diagrams are for data delay set to 1.

(5) For more information regarding the registers configuration see the Serial Communication Interface / Multichannel Buffered Serial Port (McBSP) MCBSP Register Manual / MCBSP Registers / MCBSP Register Summary Table section of the OMAP4430 TRM.

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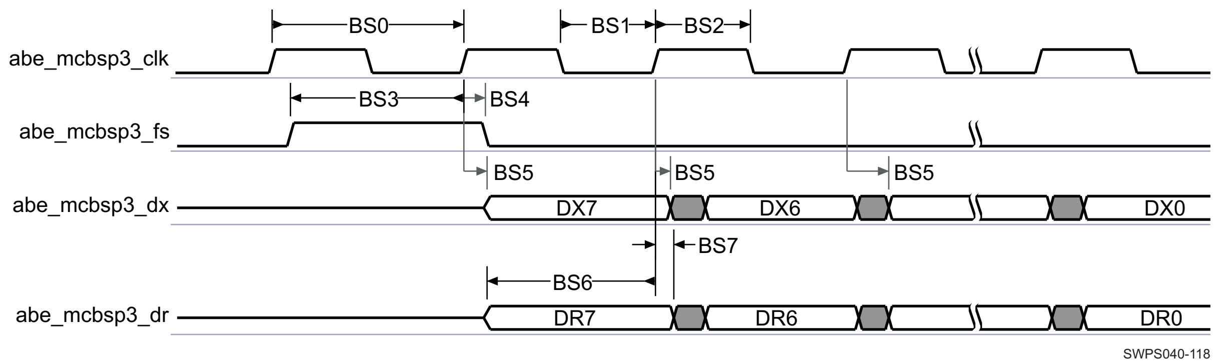

Figure 6-62. McBSP3—I2S/PCM—Slave Mode(1)(2)(3)(4)(5)

(1) mcbsp3_clk corresponds to either mcbsp3_clkx or mcbsp3_clkr; mcbsp3_fs corresponds to either mcbsp3_fsx or mcbsp3_fsr.
McBSP in 6-pin mode: dx and dr as data pins; clkx, clkr, fsx, and fsr as control pins.
McBSP in 4-pin mode: dx and dr as data pins; clkx and fsx pins as control pins. The clkx and fsx pins are internally looped back, via software configuration, respectively to the clkr and fsr internal signals for data receive.

(2) The polarity of McBSP frame synchronization is software configurable.

(3) The active clock edge selection of mcbsp3_clk (rising or falling) on which mcbsp3_dx data is latched and mcbsp3_dr data is sampled is software configurable.

(4) Timing diagrams are for data delay set to 1.

(5) For more information regarding the registers configuration see the Serial Communication Interface / Multichannel Buffered Serial Port (McBSP) MCBSP Register Manual / MCBSP Registers / MCBSP Register Summary Table section of the OMAP4430 TRM.

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6.6.1.3 McBSP4—I2S/PCM

6.6.1.3.1 McBSP4—I2S/PCM—Full Cycle—48-MHz Master and 24-MHz Slave

Table 6-60 through Table 6-63 assume testing over the recommended operating conditions and electrical characteristic conditions below (see Figure 6-63 and Figure 6-64).

Table 6-59. McBSP4 Timing Conditions—I2S/PCM(1)(2)(3)

SYSTEM CONDITION PARAMETER		VALUE		UNIT
		MIN	MAX	
Input Conditions				
t_R	Input signal rise time	400	4000	ps
t_F	Input signal fall time	400	4000	ps
PCB Conditions				
	Number of external peripherals		1	
	Far end load		5	pF
	Trace length, point-to-point interconnect		6	cm
	Characteristics impedance	30	45	Ω

(1) IO settings: MB[1:0] = 10 and LB0 = 0
For more information, see Control Module / Control Module Functional Description/ Functional Register Description / Signal Integrity Parameter Control Registers with Pad Group Assignment / I/Os with Combined Mode and Load Settings section of the OMAP4430 TRM.

(2) In this table the rise and fall times are calculated for 10% to 90% of VDDS. For more information on the corresponding OMAP4 VDDS power supply name, see Table 2-1, POWER [9] column with the ball name.

(3) To have an idea of the output OMAP4 ball load supported for this application, you can consider the following:
Output OMAP4 ball load = Far End load + 1.34 pF/cm typical x trace length (cm).

6.6.1.3.1.1 McBSP4—I2S/PCM—Full Cycle—48-MHz Master Mode

Table 6-60. McBSP4 Timing Requirements—I2S/PCM—Master Mode(1)(3)

NO.	PARAMETER		OPP100		OPP50		UNIT
			MIN	MAX	MIN	MAX	
BM5	$t_{su(drV-clkAE)}$	Setup time, mcbsp4_dr valid before mcbsp4_clk(2) active edge	3.8		6.6		ns
BM6	$t_{h(clkAE-drV)}$	Hold time, mcbsp4_dr valid after mcbsp4_clk(2) active edge	0.3		0.3		ns

(1) The timings apply to all configurations regardless of mcbsp4_clk polarity and which clock edges are used to drive output data and capture input data.

(2) mcbsp4_clk corresponds to either mcbsp4_clkx or mcbsp4_clkr; mcbsp4_clkr is available in 6-pin mode only.

(3) See DM Operating Condition Addendum for CORE OPP voltages.

Table 6-61. McBSP4 Switching Characteristics—I2S/PCM—Master Mode(4)(8)

NO.	PARAMETER		OPP100		OPP50		UNIT
			MIN	MAX	MIN	MAX	
BM0	$1 / t_{c(clk)}$	Frequency(1), output mcbsp4_clk(5) clock		48(7)		24(7)	MHz
BM1	$t_{w(clkL)}$	Typical pulse duration, output mcbsp4_clk(5) low	0.5*P(2)		0.5*P(2)		ns
BM2	$t_{w(clkH)}$	Typical pulse duration, output mcbsp4_clk(5) high	0.5*P(2)		0.5*P(2)		ns
	$t_{dc(clk)}$	Duty cycle error, output mcbsp4_clk(5)	–1042	1042	–2083	2083	ps
	$t_{j(clk)}$	Jitter standard deviation(3), output mcbsp4_clk(5)		65		65	ps
	$t_{R(clk)}$	Rise time, output mcbsp4_clk(5)	400	4000	400	4000	ps
	$t_{F(clk)}$	Fall time, output mcbsp4_clk(5)	400	4000	400	4000	ps

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Table 6-61. McBSP4 Switching Characteristics—I2S/PCM—Master Mode[(4)(8)] (continued)

NO.	PARAMETER		OPP100		OPP50		UNIT
			MIN	MAX	MIN	MAX	
BM3	$t_{d(clkAE-fsV)}$	Delay time, output mcbsp4_clk[(5)] active edge to output mcbsp4_fs[(6)] valid	0.6	9.4	0.9	19.5	ns
BM4	$t_{d(clkxAE-dxV)}$	Delay time, output mcbsp4_clkx active edge to output mcbsp4_dx valid	0.6	9.4	0.9	19.5	ns
	$t_{R(fs)}$	Rise time, output mcbsp4_fs[(6)]	400	4000	400	4000	ps
	$t_{F(fs)}$	Fall time, output mcbsp4_fs[(6)]	400	4000	400	4000	ps
	$t_{R(dx)}$	Rise time, output mcbsp4_dx	400	4000	400	4000	ps
	$t_{F(dx)}$	Fall time, output mcbsp4_dx	400	4000	400	4000	ps

(1) Related to the output mcbsp4_clkx / mcbsp4_clkr maximum and minimum frequency programmable in McBSP module by setting the configuration register SRGR1_REG[7..0].
For more information regarding the registers configuration see Serial Communication Interface / Multichannel Buffered Serial Port (McBSP) / MCBSP Register Manual / MCBSP Registers / MCBSP Register Summary Table section of the OMAP4430 TRM.

(2) P = mcbsp4_clkx / mcbsp4_clkr output clk period in ns

(3) The jitter probability density can be approximated by a Gaussian function.

(4) The timings apply to all configurations regardless of mcbsp4_clk polarity and which clock edges are used to drive output data and capture input data.

(5) mcbsp4_clk corresponds to either mcbsp4_clkx or mcbsp4_clkr; mcbsp4_clkr is available in 6-pin mode only.

(6) mcbsp4_fs corresponds to either mcbsp4_fsx or mcbsp4_fsr; mcbsp4_fsr is available in 6-pin mode only.

(7) This McBSP4 output clock frequency is based on an output PER DPLL configured at 96 MHz.
For more information regarding the registers configuration, see Power, Reset and Clock Management / Clock Management Functional Description / Internal Clock Sources/Generators / DPLL_PER Description section of the OMAP4430 TRM.

(8) See DM Operating Condition Addendum for CORE OPP voltages.

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6.6.1.3.1.2 McBSP4—I2S/PCM—Full Cycle—24-MHz Slave Mode

Table 6-62. McBSP4 Timing Requirements—I2S/PCM—Slave Mode[(4)(5)(8)]

NO.	PARAMETER		OPP100		OPP50		UNIT
			MIN	MAX	MIN	MAX	
BS0	$1 / t_{c(clk)}$	Frequency[(1)], mcbsp4_clk[(6)]		24		12	MHz
BS1	$t_{w(clkL)}$	Typical pulse duration, mcbsp4_clk[(6)] low	0.5*P[(2)]		0.5*P[(2)]		ns
BS2	$t_{w(clkH)}$	Typical pulse duration, mcbsp4_clk[(6)] high	0.5*P[(2)]		0.5*P[(2)]		ns
	$t_{dc(clk)}$	Duty cycle error, mcbsp4_clk[(6)]	–2035	2035	–4069	4069	ps
	$t_{j(clk)}$	Cycle jitter[(3)], mcbsp4_clk[(6)]		1221		2000	ps
BS3	$t_{su(fsV-clkAE)}$	Setup time, mcbsp4_fs[(7)] valid before mcbsp4_clk[(6)] active edge	6.0		11.9		ns
BS4	$t_{h(clkAE-fsV)}$	Hold time, mcbsp4_fs[(7)] valid after mcbsp4_clk[(6)] active edge	0.2		0.3		ns
BS6	$t_{su(drV-clkAE)}$	Setup time, mcbsp4_dr valid before mcbsp4_clk[(6)] active edge	6.0		11.9		ns
BS7	$t_{h(clkAE-drV)}$	Hold time, mcbsp4_dr valid after mcbsp4_clk[(6)] active edge	0.2		0.3		ns

(1) Related to the input maximum frequency supported by the McBSP module.

(2) P = mcbsp4_clkx / mcbsp4_clkr period in ns

(3) Maximum cycle jitter supported by mcbsp4_clkx / mcbsp4_clkr input clock.

(4) The timing requirements are assured for the cycle jitter and duty cycle error conditions specified.

(5) The timings apply to all configurations regardless of mcbsp4_clk polarity and which clock edges are used to drive output data and capture input data.

(6) mcbsp4_clk corresponds to either mcbsp4_clkx or mcbsp4_clkr; mcbsp4_clkr is available in 6-pin mode only.

(7) mcbsp4_fs corresponds to either mcbsp4_fsx or mcbsp4_fsr; mcbsp4_fsr is available in 6-pin mode only.

(8) See DM Operating Condition Addendum for CORE OPP voltages.

Table 6-63. McBSP4 Switching Characteristics—I2S/PCM—Slave Mode(1)(2)

NO.	PARAMETER		OPP100		OPP50		UNIT
			MIN	MAX	MIN	MAX	
BS5	$t_{d(clkxAE-dxV)}$	Delay time, input mcbsp4_clkx active edge to output mcbsp4_dx valid	0.9	23.2	1.0	40.0	ns
	$t_{R(dx)}$	Rise time, output mcbsp4_dx	400	6500	400	6500	ps
	$t_{F(dx)}$	Fall time, output mcbsp4_dx	400	6500	400	6500	ps

(1) The timings apply to all configurations regardless of mcbsp4_clk polarity and which clock edges are used to drive output data and capture input data.

(2) See DM Operating Condition Addendum for CORE OPP voltages.

6.6.1.3.2 McBSP4—I2S/PCM—Half-Cycle—24-MHz Master and 12-MHz Slave

Table 6-65 through Table 6-68 assume testing over the recommended operating conditions and electrical characteristic conditions below.

Table 6-64. McBSP4 Timing Conditions—I2S/PCM(1)(2)(3)

SYSTEM CONDITION PARAMETER		VALUE		UNIT
		MIN	MAX	
Input Conditions				
t_R	Input signal rise time	400	6500	ps
t_F	Input signal fall time	400	6500	ps
PCB Conditions				
	Number of external peripherals		1	
	Far end load		5	pF
	Trace length, point-to-point interconnect		9	cm
	Characteristics impedance	30	55	Ω

(1) IO settings: MB[1:0] = 10 and LB0 = 0.
For more information, see Control Module / Control Module Functional Description/ Functional Register Description / Signal Integrity Parameter Control Registers with Pad Group Assignment / I/Os with Combined Mode and Load Settings section of the OMAP4430 TRM.

(2) In this table the rise and fall times are calculated for 10% to 90% of VDDS. For more information on the corresponding OMAP4 VDDS power supply name, see Table 2-1, POWER [9] column with the ball name.

(3) To have an idea of the output OMAP4 ball load supported for this application, you can consider the following:
Output OMAP4 ball load = Far End load + 1.34 pF/cm typical x trace length (cm).

6.6.1.3.2.1 McBSP4—I2S/PCM—Half-Cycle—24-MHz Master Mode

Table 6-65. McBSP4 Timing Requirements—I2S/PCM—Master Mode(1)(3)

NO.	PARAMETER		OPP100		OPP50		UNIT
			MIN	MAX	MIN	MAX	
BM5	$t_{su(drV-clkAE)}$	Setup time, mcbsp4_dr valid before mcbsp4_clk(2) active edge	5.3		11.6		ns
BM6	$t_{h(clkAE-drV)}$	Hold time, mcbsp4_dr valid after mcbsp4_clk(2) active edge	5.3		11.3		ns

(1) The timings apply to all configurations regardless of mcbsp4_clk polarity and which clock edges are used to drive output data and capture input data.

(2) mcbsp4_clk corresponds to either mcbsp4_clkx or mcbsp4_clkr; mcbsp4_clkr is available in 6-pin mode only.

(3) See DM Operating Condition Addendum for CORE OPP voltages.

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Table 6-66. McBSP4 Switching Characteristics—I2S/PCM—Master Mode[(4)(8)]

NO.	PARAMETER		OPP100		OPP50		UNIT
			MIN	MAX	MIN	MAX	
BM0	$1 / t_{c(clk)}$	Frequency[(1)], output mcbsp4_clk clock		24[(7)]		12[(7)]	MHz
BM1	$t_{w(clkL)}$	Typical pulse duration, output mcbsp4_clk low	0.5*P[(2)]		0.5*P[(2)]		ns
BM2	$t_{w(clkH)}$	Typical pulse duration, output mcbsp4_clk high	0.5*P[(2)]		0.5*P[(2)]		ns
	$t_{dc(clk)}$	Duty cycle error, output mcbsp4_clk	–2035	2035	–4069	4069	ps
	$t_{j(clk)}$	Jitter standard deviation[(3)], output mcbsp4_clk		65		65	ps
	$t_{R(clk)}$	Rise time, output mcbsp4_clk	400	6500	400	6500	ps
	$t_{F(clk)}$	Fall time, output mcbsp4_clk	400	6500	400	6500	ps
BM3	$t_{d(clkAE-fsV)}$	Delay time, output mcbsp4_clk active edge to output mcbsp4_fs[(6)] valid	–7.1	11.7	–15.2	23.6	ns
BM4	$t_{d(clkxAE-dxV)}$	Delay time, output mcbsp4_clkx active edge to output mcbsp4_dx valid	–7.1	11.7	–15.2	23.6	ns
	$t_{R(fs)}$	Rise time, output mcbsp4_fs[(6)]	400	6500	400	6500	ps
	$t_{F(fs)}$	Fall time, output mcbsp4_fs[(6)]	400	6500	400	6500	ps
	$t_{R(dx)}$	Rise time, output mcbsp4_dx	400	6500	400	6500	ps
	$t_{F(dx)}$	Fall time, output mcbsp4_dx	400	6500	400	6500	ps

(1) Related to the output mcbsp4_clkx / mcbsp4_clkr maximum and minimum frequency programmable in McBSP module by setting the configuration register SRGR1_REG[7..0].
For more information regarding the registers configuration see the Serial Communication Interface / Multichannel Buffered Serial Port (McBSP) / MCBSP Register Manual / MCBSP Registers / MCBSP Register Summary Table section of the OMAP4430 TRM.

(2) P = mcbsp4_clkx / mcbsp4_clkr output clk period in ns.

(3) The jitter probability density can be approximated by a Gaussian function.

(4) The timings apply to all configurations regardless of mcbsp4_clk polarity and which clock edges are used to drive output data and capture input data.

(5) mcbsp4_clk corresponds to either mcbsp4_clkx or mcbsp4_clkr; mcbsp4_clkr is available in 6-pin mode only.

(6) mcbsp4_fs corresponds to either mcbsp4_fsx or mcbsp4_fsr; mcbsp4_fsr is available in 6-pin mode only.

(7) This McBSP4 output clock frequency is based on an output PER DPLL configured at 96 MHz.
For more information regarding the registers configuration, see the Power, Reset and Clock Management / Clock Management Functional Description / Internal Clock Sources/Generators / DPLL_PER Description section of the OMAP4430 TRM.

(8) See DM Operating Condition Addendum for CORE OPP voltages.

6.6.1.3.2.2 McBSP4—I2S/PCM—Half-Cycle—12-MHz Slave Mode

Table 6-67. McBSP4 Timing Requirements—I2S/PCM—Slave Mode[(4)(5)(8)]

NO.	PARAMETER		OPP100		OPP50		UNIT
			MIN	MAX	MIN	MAX	
BS0	$1 / t_{c(clk)}$	Frequency[(1)], mcbsp4_clk[(6)]		12		6	MHz
BS1	$t_{w(clkL)}$	Typical pulse duration, mcbsp4_clk[(6)] low	0.5*P[(2)]		0.5*P[(2)]		ns
BS2	$t_{w(clkH)}$	Typical pulse duration, mcbsp4_clk[(6)] high	0.5*P[(2)]		0.5*P[(2)]		ns
	$t_{dc(clk)}$	Duty cycle error, mcbsp4_clk[(6)]	–4069	4069	–8138	8138	ps
	$t_{j(clk)}$	Cycle jitter[(3)], mcbsp4_clk[(6)]		2000		2000	ps
BS3	$t_{su(fsV-clkAE)}$	Setup time, mcbsp4_fs[(7)] valid before mcbsp4_clk[(6)] active edge	13.2		26.7		ns
BS4	$t_{h(clkAE-fsV)}$	Hold time, mcbsp4_fs[(7)] valid after mcbsp4_clk[(6)] active edge	0.3		0.3		ns
BS6	$t_{su(drV-clkAE)}$	Setup time, mcbsp4_dr valid before mcbsp4_clk[(6)] active edge	13.2		26.7		ns
BS7	$t_{h(clkAE-drV)}$	Hold time, mcbsp4_dr valid after mcbsp4_clk[(6)] active edge	0.3		0.3		ns

(1) Related to the input maximum frequency supported by the McBSP module.
(2) P = mcbsp4_clkx / mcbsp4_clkr period in ns
(3) Maximum cycle jitter supported by mcbsp4_clkx / mcbsp4_clkr input clock.
(4) The timing requirements are assured for the cycle jitter and duty cycle error conditions specified.
(5) The timings apply to all configurations regardless of mcbsp4_clk polarity and which clock edges are used to drive output data and capture input data.
(6) mcbsp4_clk corresponds to either mcbsp4_clkx or mcbsp4_clkr; mcbsp4_clkr is available in 6-pin mode only.
(7) mcbsp4_fs corresponds to either mcbsp4_fsx or mcbsp4_fsr; mcbsp4_fsr is available in 6-pin mode only.
(8) See DM Operating Condition Addendum for CORE OPP voltages.

Table 6-68. McBSP4 Switching Characteristics—I2S/PCM—Slave Mode[(1)(2)]

NO.	PARAMETER		OPP100		OPP50		UNIT
			MIN	MAX	MIN	MAX	
BS5	$t_{d(clkxAE-dxV)}$	Delay time, input mcbsp4_clkx active edge to output mcbsp4_dx valid	1.0	23.2	1.1	40.0	ns
	$t_{R(dx)}$	Rise time, output mcbsp4_dx	400	6500	400	6500	ps
	$t_{F(dx)}$	Fall time, output mcbsp4_dx	400	6500	400	6500	ps

(1) The timings apply to all configurations regardless of mcbsp4_clk polarity and which clock edges are used to drive output data and capture input data.
(2) See DM Operating Condition Addendum for CORE OPP voltages.

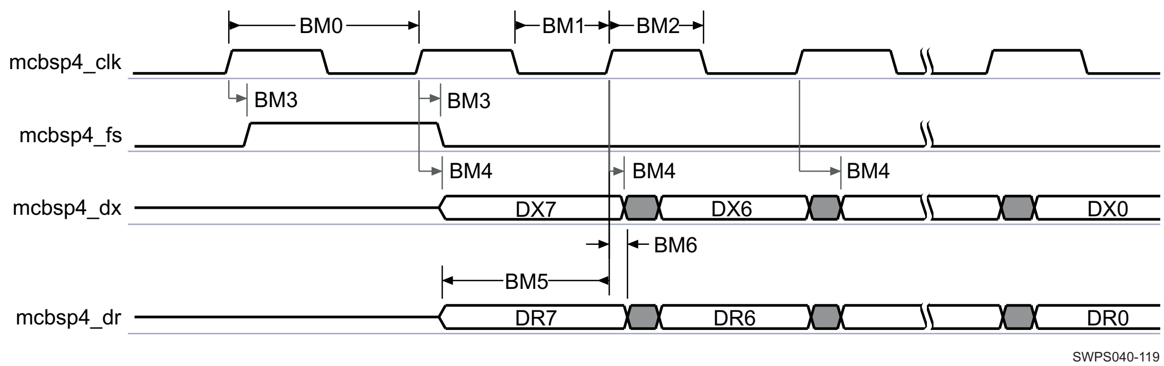

Figure 6-63. McBSP4—I2S/PCM—Master Mode[(1)(2)(3)(4)(5)]

(1) mcbsp4_clk corresponds to either mcbsp4_clkx or mcbsp4_clkr; mcbsp4_fs corresponds to either mcbsp4_fsx or mcbsp4_fsr.
McBSP in 6-pin mode: dx and dr as data pins; clkx, clkr, fsx, and fsr as control pins.
McBSP in 4-pin mode: dx and dr as data pins; clkx and fsx pins as control pins. The clkx and fsx pins are internally looped back, via software configuration, respectively to the clkr and fsr internal signals for data receive.
(2) The polarity of McBSP frame synchronization is software configurable.
(3) The active clock edge selection of mcbsp4_clk (rising or falling) on which mcbsp4_dx data is latched and mcbsp4_dr data is sampled is software configurable.
(4) Timing diagrams are for data delay set to 1.
(5) For more information regarding the registers configuration see the Serial Communication Interface / Multichannel Buffered Serial Port (McBSP) MCBSP Register Manual / MCBSP Registers / MCBSP Register Summary Table section of the OMAP4430 TRM.

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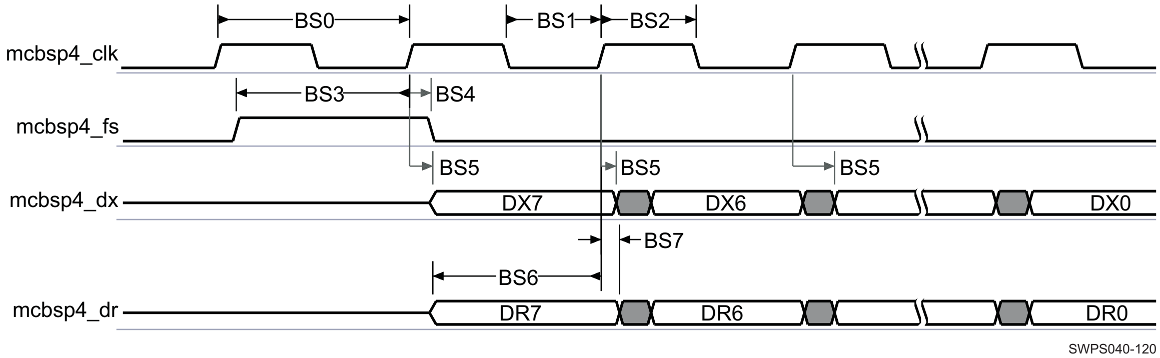

Figure 6-64. McBSP4—I2S/PCM—Slave Mode(1)(2)(3)(4)(5)

(1) mcbsp4_clk corresponds to either mcbsp4_clkx or mcbsp4_clkr; mcbsp4_fs corresponds to either mcbsp4_fsx or mcbsp4_fsr.
McBSP in 6-pin mode: dx and dr as data pins; clkx, clkr, fsx, and fsr as control pins.
McBSP in 4-pin mode: dx and dr as data pins; clkx and fsx pins as control pins. The clkx and fsx pins are internally looped back, via software configuration, respectively to the clkr and fsr internal signals for data receive.

(2) The polarity of McBSP frame synchronization is software configurable.

(3) The active clock edge selection of mcbsp4_clk (rising or falling) on which mcbsp4_dx data is latched and mcbsp4_dr data is sampled is software configurable.

(4) Timing diagrams are for data delay set to 1.

(5) For more information regarding the registers configuration see Serial Communication Interface / Multichannel Buffered Serial Port (McBSP) MCBSP Register Manual / MCBSP Registers / MCBSP Register Summary Table section of the OMAP4430 TRM.

6.6.2 Multichannel Buffered Serial Port (McASP)

NOTE

For more information, see the Serial Communication Interface section of the OMAP4430 TRM.

Table 6-70 assumes testing over the recommended operating conditions and electrical characteristic conditions below (see Figure 6-65).

Table 6-69. McASP Timing Conditions(1)(2)(3)

SYSTEM CONDITION PARAMETER		VALUE		UNIT
		MIN	MAX	
PCB Conditions				
	Number of external peripherals		1	
	Far end load		7	pF
	Trace length, point-to-point interconnect		10	cm
	Characteristics impedance	30	60	Ω

(1) O settings: MB[1:0] = 10 and LB0 = 0.
For more information, see Control Module / Control Module Functional Description/ Functional Register Description / Signal Integrity Parameter Control Registers with Pad Group Assignment / 50-Ω Output Buffer I/Os with Combined Mode and Load Settings section of the OMAP4430 TRM.

(2) In this table the rise and fall times are calculated for 10% to 90% of VDDS. For more information on the corresponding OMAP4 VDDS power supply name, see Table 2-1, POWER [9] column with the ball name.

(3) To have an idea of the output OMAP4 ball load supported for this application, you can consider the following:
Output OMAP4 ball load = Far End load + 1.34 pF/cm typical x trace length (cm).

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Table 6-70. McASP Switching Characteristics[4]

NO.	PARAMETER		OPP100		OPP50		UNIT
			MIN	MAX	MIN	MAX	
9	$1 / t_{c(AHCLKX)}$	Frequency[1], abe_mcasp_ahclkx		24.576[3]		24.576[3]	MHz
10	$t_{w(AHCLKX)}$	Typical pulse duration, abe_mcasp_ahclkx high or low	0.5*P[2] – 2.5		0.5*P[2] – 2.5		ns
11	$1 / t_{c(ACLKX)}$	Frequency[1], abe_mcasp_aclkx		24.576[3]		24.576[3]	MHz
12	$t_{w(ACLKX)}$	Typical pulse duration, abe_mcasp_aclkx high or low	0.5*P[2] – 2.5		0.5*P[2] – 2.5		ns
13	$t_{d(ACLKX-AFSX)}$	Delay time, abe_mcasp_aclkx transmit edge to abe_mcasp_afsx output valid	0	6	0	6	ns
14	$t_{d(ACLKX-AXR)}$	Delay time, abe_mcasp_aclkx transmit edge to abe_mcasp_axr output valid	0	6	0	6	ns
15	$t_{dis(AXR-ACLKX)}$	Disable time, abe_mcasp_aclkx transmit edge to abe_mcasp_axr output high impedance	0	6	0	6	ns

(1) Related to the input maximum frequency supported by the McASP module.

(2) P = AHCLKR/X period

(3) This McASP output clock frequency is based on an output ABE DPLL configured at 196.608 MHz.
For more information regarding the registers configuration, see the Power, Reset and Clock Management / Clock Management Functional Description / Internal Clock Sources/Generators / DPLL_ABE Description section of the OMAP4430 TRM.

(4) See DM Operating Condition Addendum for CORE OPP voltages.

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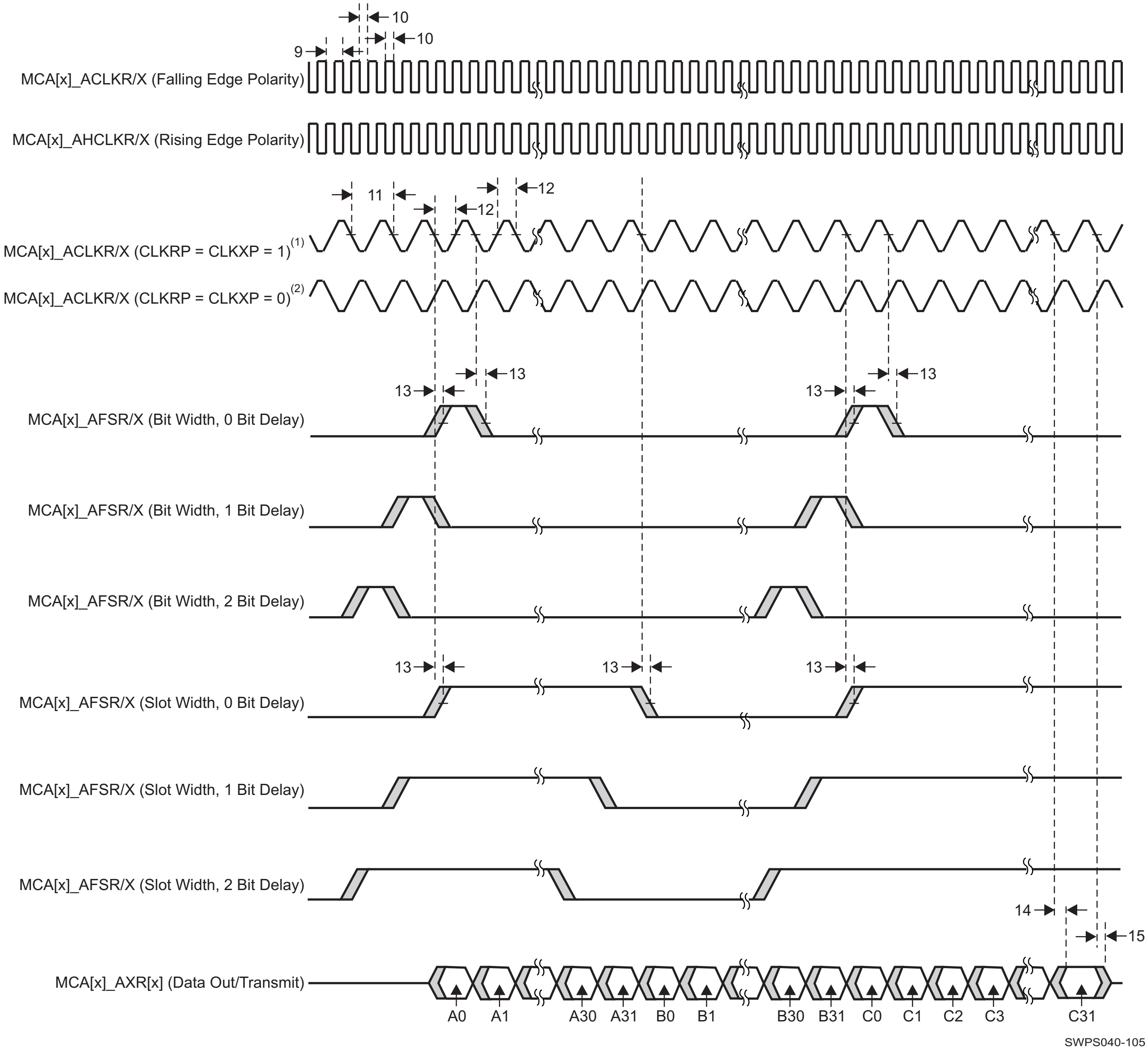

Figure 6-65. McASP Output Timing(1)(2)

(1) For CLKRP = CLKXP = 1, the McASP transmitter is configured for falling edge (to shift data out) and the McASP receiver is configured for rising edge (to shift data in).

(2) For CLKRP = CLKXP = 0, the McASP transmitter is configured for rising edge (to shift data out) and the McASP receiver is configured for falling edge (to shift data in).

6.6.3 Multichannel Serial Port Interface (McSPI)

NOTE

For more information, see the Serial Communication Interface section of the OMAP4430 TRM.

McSPI allows a duplex, synchronous, serial communication between a local host and SPI compliant external devices. The following timings are applicable to the different configurations of McSPI in master/slave mode for any McSPI and any channel (n).

6.6.3.1 McSPI—MCSPI Interface in Transmit and Receive—Slave Mode

In slave mode, McSPI initiates data transfer on the data lines (mcspix_somi, mcspix_simo) when it receives an SPI clock (mcspix_clk) from the external SPI master device.

NOTE

With other system conditions (for instance with a less jitter and duty cycle error source clock), 24 MHz of clock frequency could be reached.

6.6.3.1.1 McSPI1

Table 6-72 and Table 6-73 assume testing over the recommended operating conditions and electrical characteristic conditions below (see Figure 6-66 and Figure 6-67).

Table 6-71. McSPI1 Timing Conditions—Slave Mode(1)(2)(3)

SYSTEM CONDITION PARAMETER		VALUE MIN	VALUE MAX	UNIT
Input Conditions				
t_R	Input signal rise time	1.00	3.00	ns
t_F	Input signal fall time	1.00	3.00	ns
PCB Conditions				
	Number of external peripherals		-	
	Far end load		5	pF
	Trace length	2	5	cm
	Characteristics impedance	20	70	Ω

(1) McSPI1:
- Balls AF22 / AE22 / AG22 / AE23 / AF23 (mcspi1_clk / mcspi1_somi / mcspi1_simo / mcspi1_cs0 / mcspi1_cs1):
SC[1:0] = 00 and LB[1:0] = 10
For more information, see Control Module / Control Module Functional Description/ Functional Register Description / Signal Integrity Parameter Control Registers with Pad Group Assignment / Low Speed I/Os Combined Slew Rate vs TL Length and Load Settings section of the OMAP4430 TRM.
- Balls AG23 / AH23 (mcspi1_cs2 / mcspi1_cs3):
MB[1:0] = 11 and LB0 = 0
For more information, see Control Module / Control Module Functional Description/ Functional Register Description / Signal Integrity Parameter Control Registers with Pad Group Assignment / 50-Ω Output Buffer I/Os with Combined Mode and Load Settings of the OMAP4430 TRM.

(2) In this table the rise and fall times are calculated for 10% to 90% of VDDS. For more information on the corresponding OMAP4 VDDS power supply name, see Table 2-1, POWER [9] column with the ball name.

(3) To have an idea of the output OMAP4 ball load supported for this application, you can consider the following:
Output OMAP4 ball load = Far End load + 1.34 pF/cm typical x trace length (cm).

Table 6-72. McSPI1 Timing Requirements—Slave Mode(4)(7)

NO.	PARAMETER		16 MHz SET MIN	16 MHz SET MAX	8 MHz SET MIN	8 MHz SET MAX	UNIT
SS1	$1 / t_{c(clk)}$	Frequency(1), mcspi1_clk(5)		16(7)		8(7)	MHz
SS2	$t_{w(clkL)}$	Typical pulse duration, mcspi1_clk(5) low	0.5*P(2)		0.5*P(2)		ns
SS3	$t_{w(clkH)}$	Typical pulse duration, mcspi1_clk(5) high	0.5*P(2)		0.5*P(2)		ns
	$t_{dc(clk)}$	Duty cycle error, mcspi1_clk	–3125	3125	–6250	6250	ps
	$t_{j(clk)}$	Cycle jitter(3), mcspi1_clk	–1875	1875	–2000	2000	ps
	$t_{R(clk)}$	Rise time, mcspi1_clk		3000		3000	ps
	$t_{F(clk)}$	Fall time, mcspi1_clk		3000		3000	ps
SS4	$t_{su(SIMO-CLKAE)}$	Setup time, mcspi1_simo valid before mcspi1_clk(5) active edge	12.82		28.61		ns

Table 6-72. McSPI1 Timing Requirements—Slave Mode[(4)(7)] (continued)

NO.	PARAMETER		16 MHz SET		8 MHz SET		UNIT
			MIN	MAX	MIN	MAX	
SS5	$t_{h(clkAE-SIMO)}$	Hold time, mcspi1_simo valid after mcspi1_clk[(5)] active edge	12.82		28.61		ns
SS8	$t_{su(CS-CLKAE)}$	Setup time, mcspi1_cs0 valid before mcspi1_clk[(5)] first edge	12.82		28.61		ns
SS9	$t_{h(clkAE-CS)}$	Hold time, mcspi1_cs0 valid after mcspi1_clk[(5)] last edge	12.82		28.61		ns

(1) Related to the input maximum frequency supported by the McSPI module.
(2) P = mcspi1_clk period in ns
(3) Maximum cycle jitter supported by mcspi1_clk input clock.
(4) The timing requirements are assured for the cycle jitter and duty cycle error conditions specified.
(5) This timing applies to all configurations regardless of mcspi1_clk polarity and which clock edges are used to drive output data and capture input data.
(6) With other system conditions (for instance with a less jitter and duty cycle error source clock), 24 MHz of clock frequency could be reached.
(7) The timings requirements described are applicable to both CORE OPP50 and OPP100 operating points.

Table 6-73. McSPI1 Switching Characteristics—Slave Mode[(3)]

NO.	PARAMETER			16 MHz SET[(3)]		8 MHz SET[(3)]		UNIT
				MIN	MAX	MIN	MAX	
SS6	$t_{d(clk-SOMI)}$	Delay time, mcspi1_clk[(1)] active edge to mcspi1_somi transition		–4.66	18.41	–12.01	37.32	ns
SS7	$t_{d(CS-SOMI)}$	Delay time, mcspi1_cs0 active edge to mcspi1_somi transition	PHA = 0[(2)]		18.41		37.32	ns
	$t_{R(SOMI)}$	Rise time, mcspi1_somi			4000.0		4000.0	ps
	$t_{F(SOMI)}$	Fall time, mcspi1_somi			4000.0		4000.0	ps

(1) The polarity of mcspi1_clk and the active edge (rising or falling) on which mcspi1_simo is driven and mcspi1_somi is latched is all software configurable:
– mcspi1_clk phase programmable with the bit PHA of MCSPI_Ch(i)CONF register: PHA = 0 (Modes 0 and 2).

For more information, see the McSPI environment chapter, Data Format Configurations section of the OMAP4430 TRM for modes and phase correspondence description.
(2) This timing applies to all configurations regardless of mcspi1_clk polarity and which clock edges are used to drive output data and capture input data.
(3) The timings requirements described are applicable to both CORE OPP50 and OPP100 operating points.

6.6.3.1.2 McSPI2 and McSPI4

Table 6-75 and Table 6-76 assume testing over the recommended operating conditions and electrical characteristic conditions below (see Figure 6-66 and Figure 6-67).

Table 6-74. McSPI2 and McSPI4 Timing Conditions—Slave Mode[(1)(2)(3)]

SYSTEM CONDITION PARAMETER		VALUE		UNIT
		MIN	MAX	
Input Conditions				
t_R	Input signal rise time	1.00	4.00	ns
t_F	Input signal fall time	1.00	4.00	ns
PCB Conditions				
	Number of external peripherals		-	
	Far end load		5	pF
	Trace length	2	5	cm
	Characteristics impedance	20	60	Ω

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(1) IO settings: LB0 = 0 and MB[1:0] = 11.
For more information, see Control Module / Control Module Functional Description/ Functional Register Description / Signal Integrity Parameter Control Registers with Pad Group Assignment / 50-Ω Output Buffer I/Os with Combined Mode and Load Settings section of the OMAP4430 TRM.

(2) In this table the rise and fall times are calculated for 10% to 90% of VDDS. For more information on the corresponding OMAP4 VDDS power supply name, see Table 2-1, POWER [9] column with the ball name.

(3) To have an idea of the output OMAP4 ball load supported for this application, you can consider the following:
Output OMAP4 ball load = Far End load + 1.34 pF/cm typical x trace length (cm).

Table 6-75. McSPI2 and McSPI4 Timing Requirements—Slave Mode(4)(7)

NO.	PARAMETER		OPP100		OPP50		UNIT
			MIN	MAX	MIN	MAX	
SS1	$1 / t_{c(clk)}$	Frequency(1), mcspix_clk(5)		16(6)		8	MHz
SS2	$t_{w(clkL)}$	Typical pulse duration, mcspix_clk(5) low	0.5*P(2)		0.5*P(2)		ns
SS3	$t_{w(clkH)}$	Typical pulse duration, mcspix_clk(5) high	0.5*P(2)		0.5*P(2)		ns
	$t_{dc(clk)}$	Duty cycle error, mcspix_clk	–3125	3125	–6250	6250	ps
	$t_{j(clk)}$	Cycle jitter(3), mcspix_clk	–1875	1875	–2000	2000	ps
	$t_{R(clk)}$	Rise time, mcspix_clk		4000		4000	ps
	$t_{F(clk)}$	Fall time, mcspix_clk		4000		4000	ps
SS4	$t_{su(SIMO-clkAE)}$	Setup time, mcspix_simo valid before mcspix_clk(5) active edge	12.95		28.74		ns
SS5	$t_{h(clkAE-SIMO)}$	Hold time, mcspix_simo valid after mcspix_clk(5) active edge	12.95		28.74		ns
SS8	$t_{su(CS-clkAE)}$	Setup time, mcspix_cs0 valid before mcspix_clk(5) first edge	12.95		28.74		ns
SS9	$t_{h(clkAE-CS)}$	Hold time, mcspix_cs0 valid after mcspix_clk(5) last edge	12.95		28.74		ns

(1) Related to the input maximum frequency supported by the McSPI module.
(2) P = mcspix_clk period in ns
(3) Maximum cycle jitter supported by mcspix_clk input clock.
(4) The timing requirements are assured for the cycle jitter and duty cycle error conditions specified.
(5) This timing applies to all configurations regardless of mcspix_clk polarity and which clock edges are used to drive output data and capture input data.
(6) With other system conditions (for instance with a less jitter and duty cycle error source clock), 24 MHz of clock frequency could be reached.
(7) See DM Operating Condition Addendum for CORE OPP voltages.

Table 6-76. McSPI2 and McSPI4 Switching Characteristics—Slave Mode(2)(3)

NO.	PARAMETER			OPP100		OPP50		UNIT
				MIN	MAX	MIN	MAX	
SS6	$t_{d(clk-SOMI)}$	Delay time, mcspi2_clk(1) active edge to mcspi2_somi transition		–3.48	16.60	–10.83	36.14	ns
SS7	$t_{d(CS-SOMI)}$	Delay time, mcspi2_cs0 active edge to mcspi2_somi transition	PHA = 0(2)		16.60		36.14	ns
	$t_{R(SOMI)}$	Rise time, mcspi2_somi			5545		5545	ps
	$t_{F(SOMI)}$	Fall time, mcspi2_somi			5545		5545	ps

(1) The polarity of mcspi2_clk and the active edge (rising or falling) on which mcspi2_simo is driven and mcspi2_somi is latched is all software configurable:
– mcspi2_clk phase programmable with the bit PHA of MCSPI_Ch(i)CONF register: PHA = 0 (Modes 0 and 2).

For more information, see the McSPI environment chapter, Data Format Configurations section of the OMAP4430 TRM for modes and phase correspondence description.
(2) This timing applies to all configurations regardless of mcspi2_clk polarity and which clock edges are used to drive output data and capture input data.
(3) See DM Operating Condition Addendum for CORE OPP voltages.

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6.6.3.1.3 McSPI3

Table 6-78 and Table 6-79 assume testing over the recommended operating conditions and electrical characteristic conditions below (see Figure 6-66 and Figure 6-67).

Table 6-77. McSPI3 Timing Conditions—Slave Mode(1)(2)(3)

SYSTEM CONDITION PARAMETER		VALUE		UNIT
		MIN	MAX	
Input Conditions				
t_R	Input signal rise time	1.00	4.00	ns
t_F	Input signal fall time	1.00	4.00	ns
PCB Conditions				
	Number of external peripherals		-	
	Far end load		5	pF
	Trace length	2	5	cm
	Characteristics impedance	20	50	Ω

(1) IO settings: DS0 = 0.
For more information, see Control Module / Control Module Functional Description/ Functional Register Description / Signal Integrity Parameter Control Registers with Pad Group Assignment / I/O cells with Configurable Output Driver Impedance of the OMAP4430 TRM.

(2) In this table the rise and fall times are calculated for 10% to 90% of VDDS. For more information on the corresponding OMAP4 VDDS power supply name, see Table 2-1, POWER [9] column with the ball name.

(3) To have an idea of the output OMAP4 ball load supported for this application, you can consider the following:
Output OMAP4 ball load = Far End load + 1.34 pF/cm typical x trace length (cm).

Table 6-78. McSPI3 Timing Requirements—Slave Mode(4)(7)

NO.	PARAMETER		OPP100		OPP50		UNIT
			MIN	MAX	MIN	MAX	
SS1	$1 / t_{c(clk)}$	Frequency(1), mcspi3_clk(5)		16(6)		8	MHz
SS2	$t_{w(clkL)}$	Typical pulse duration, mcspi3_clk(5) low	0.5*P(2)		0.5*P(2)		ns
SS3	$t_{w(clkH)}$	Typical pulse duration, mcspi3_clk(5) high	0.5*P(2)		0.5*P(2)		ns
	$t_{dc(clk)}$	Duty cycle error, mcspi3_clk	–3125	3125	–6250	6250	ps
	$t_{j(clk)}$	Cycle jitter(3), mcspi3_clk	–1875	1875	–2000	2000	ps
	$t_{R(clk)}$	Rise time, mcspi3_clk		4000		4000	ps
	$t_{F(clk)}$	Fall time, mcspi3_clk		4000		4000	ps
SS4	$t_{su(SIMO-CLKAE)}$	Setup time, mcspi3_simo valid before mcspi3_clk(5) active edge	12.92		28.70		ns
SS5	$t_{h(clkAE-SIMO)}$	Hold time, mcspi3_simo valid after mcspi3_clk(5) active edge	12.92		28.70		ns
SS8	$t_{su(CS-CLKAE)}$	Setup time, mcspi3_cs0 valid before mcspi3_clk(5) first edge	12.92		28.70		ns
SS9	$t_{h(clkAE-CS)}$	Hold time, mcspi3_cs0 valid after mcspi3_clk(5) last edge	12.92		28.70		ns

(1) Related to the input maximum frequency supported by the McSPI module.

(2) P = mcspi3_clk period in ns

(3) Maximum cycle jitter supported by mcspi3_clk input clock.

(4) The timing requirements are assured for the cycle jitter and duty cycle error conditions specified.

(5) This timing applies to all configurations regardless of mcspi3_clk polarity and which clock edges are used to drive output data and capture input data.

(6) With other system conditions (for instance with a less jitter and duty cycle error source clock), 24 MHz of clock frequency could be reached.

(7) See DM Operating Condition Addendum for CORE OPP voltages.

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Table 6-79. McSPI3 Switching Characteristics—Slave Mode(2)(3)

NO.	PARAMETER			OPP100		OPP50		UNIT
				MIN	MAX	MIN	MAX	
SS6	$t_{d(clk-SOMI)}$	Delay time, mcspi3_clk(1) active edge to mcspi3_somi transition		–3.99	17.12	–11.34	36.66	ns
SS7	$t_{d(CS-SOMI)}$	Delay time, mcspi3_cs0 active edge to mcspi3_somi transition	PHA = 0		17.12		36.66	ns
	$t_{R(SOMI)}$	Rise time, mcspi3_somi			5001		5001	ps
	$t_{F(SOMI)}$	Fall time, mcspi3_somi			5001		5001	ps

(1) The polarity of mcspi3_clk and the active edge (rising or falling) on which mcspi3_simo is driven and mcspi3_somi is latched is all software configurable:

– mcspi3_clk phase programmable with the bit PHA of MCSPI_Ch(i)CONF register: PHA = 0 (Modes 0 and 2).

For more information, see the McSPI environment chapter, Data Format Configurations section of the OMAP4430 TRM for modes and phase correspondence description.

(2) This timing applies to all configurations regardless of mcspi3_clk polarity and which clock edges are used to drive output data and capture input data.

(3) See DM Operating Condition Addendum for CORE OPP voltages.

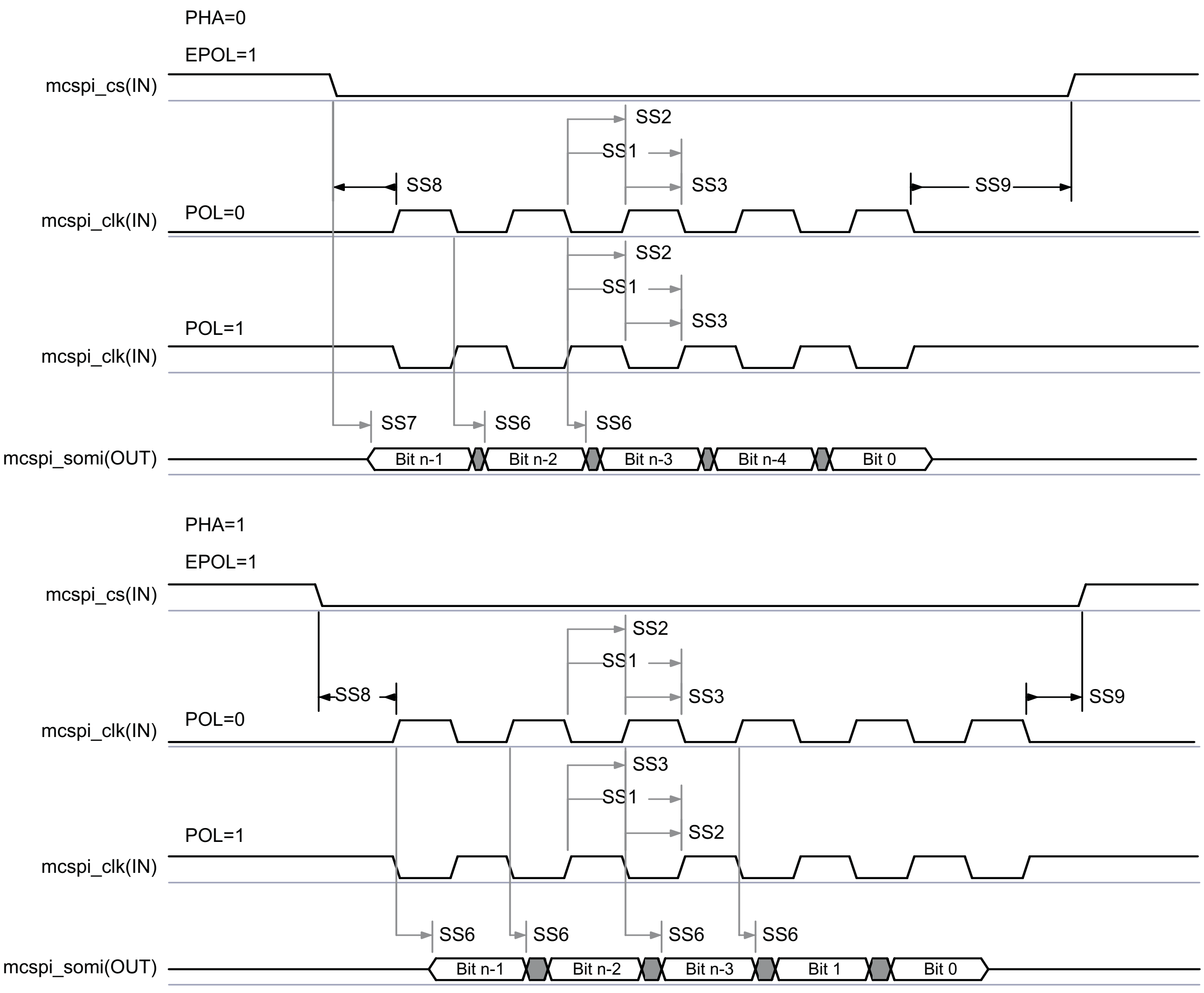

Figure 6-66. McSPI—Slave Mode—Transmit(1)(2)(3)

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(1) The active clock edge selection of mcspix_clk (rising or falling) on which mcspix_simo is driven and mcspix_somi data is latched is software configurable with the bit MCSPI_Ch(i)CONF[1] = POL and the bit MCSPI_Ch(i)CONF[0] = PHA.

(2) The polarity of mcspix_cs is software configurable with the bit MCSPI_Ch(i)CONF[6] = EPOL.

(3) In mcspix, x is equal to 1, 2, 3, or 4.

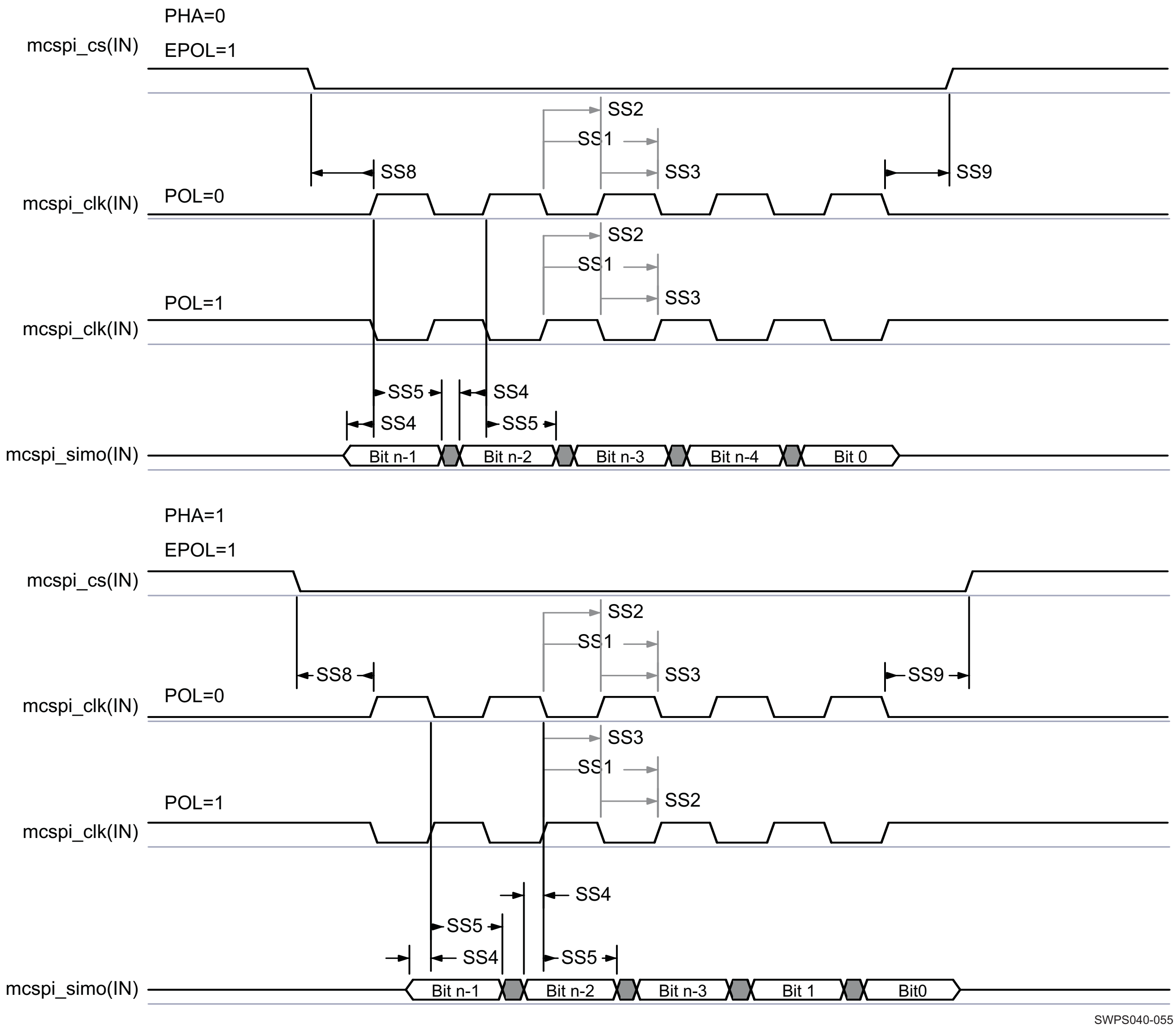

Figure 6-67. McSPI—Slave Mode—Receive(1)(2)(3)

(1) The active clock edge selection of mcspix_clk (rising or falling) on which mcspix_simo is driven and mcspix_somi data is latched is software configurable with the bit MCSPI_Ch(i)CONF[1] = POL and the bit MCSPI_Ch(i)CONF[0] = PHA.

(2) The polarity of mcspix_cs is software configurable with the bit MCSPI_Ch(i)CONF[6] = EPOL.

(3) In mcspix, x is equal to 1, 2, 3, or 4.

6.6.3.2 McSPI—McSPI Interface in Transmit and Receive—Master Mode

In master mode, McSPI supports multichannel communication. McSPI initiates a data transfer on the data lines (SPIDAT [1:0]) and generates clock (SPICLK) and control signals (SPIEN) to a single SPI slave device at a time.

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6.6.3.2.1 McSPI1 and McSPI2—Master Mode—24-MHz Frequency Clock

Table 6-81 and Table 6-82 assume testing over the recommended operating conditions and electrical characteristic conditions below (see Figure 6-68 and Figure 6-69).

Table 6-80. McSPI1 Timing Conditions—Master Mode(1)(2)(3)

SYSTEM CONDITION PARAMETER		VALUE		UNIT
		MIN	MAX	
Input Conditions				
t_R	Input signal rise time	0.4	5	ns
t_F	Input signal fall time	0.4	5	ns
PCB Conditions				
	Number of external peripherals		4	
	Far end load		25	pF
	Trace length	1	10	cm
	Characteristics impedance	30	60	Ω

(1) IO settings:
- McSPI1:
  - Balls AF22 / AE22 / AG22 / AE23 / AF23 (mcspi1_clk / mcspi1_somi / mcspi1_simo / mcspi1_cs0 / mcspi1_cs1): SC[1:0] = 00 and LB[1:0] = 10
    For more information, see Control Module / Control Module Functional Description/ Functional Register Description / Signal Integrity Parameter Control Registers with Pad Group Assignment / Low Speed I/Os Combined Slew Rate vs TL Length and Load Settings section of the OMAP4430 TRM.
  - Balls AG23 / AH23 (mcspi1_cs2 / mcspi1_cs3): MB[1:0] = 11 and LB0 = 0
    For more information, see Control Module / Control Module Functional Description/ Functional Register Description / Signal Integrity Parameter Control Registers with Pad Group Assignment / 50-Ω Output Buffer I/Os with Combined Mode and Load Settings of the OMAP4430 TRM.

(2) In this table the rise and fall times are calculated for 10% to 90% of VDDS. For more information on the corresponding OMAP4 VDDS power supply name, see Table 2-1, POWER [9] column with the ball name.

(3) To have an idea of the output OMAP4 ball load supported for this application, you can consider the following:
Output OMAP4 ball load = Far End load + 1.34 pF/cm typical x trace length (cm).

Table 6-81. McSPI1 Timing Requirements—Master Mode(2)

NO.	PARAMETER		OPP100		OPP50		UNIT
			MIN	MAX	MIN	MAX	
SM4	$t_{su(SOMI-CLKAE)}$	Setup time, mcspi1_somi valid before mcspi1_clk(1) active edge	3.02		3.02		ns
SM5	$t_{h(clkAE-SOMI)}$	Hold time, mcspi1_somi valid after mcspi1_clk(1) active edge	2.76		2.76		ns

(1) This timing applies to all configurations regardless of mcspi_clk polarity and which clock edges are used to drive output data and capture input data.

(2) See DM Operating Condition Addendum for CORE OPP voltages.

Table 6-82. McSPI1 Switching Requirements—Master Mode(8)

NO.	PARAMETER		OPP100		OPP50		UNIT
			MIN	MAX	MIN	MAX	
SM1	$1 / t_{c(clk)}$	Frequency(1), mcspi1_clk(4)		24(7)		24(7)	MHz
SM2	$t_{w(clkL)}$	Typical pulse duration, mcspi1_clk(4) low	0.5*P(2)		0.5*P(2)		ns
SM3	$t_{w(clkH)}$	Typical pulse duration, mcspi1_clk(4) high	0.5*P(2)		0.5*P(2)		ns
	$t_{dc(clk)}$	Duty cycle error, mcspi1_clk	–2083	2083	–2083	2083	ps
	$t_{j(clk)}$	Jitter standard deviation(3), mcspi1_clk		65		65	ps
	$t_{R(clk)}$	Rise time, mcspi1_clk		10685		10685	ps
	$t_{F(clk)}$	Fall time, mcspi1_clk		10685		10685	ps

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Table 6-82. McSPI1 Switching Requirements—Master Mode[(8)] (continued)

NO.	PARAMETER			OPP100		OPP50		UNIT
				MIN	MAX	MIN	MAX	
SM6	$t_{d(clk\text{-}SIMO)}$	Delay time, mcspi1_clk[(4)] active edge to mcspi1_simo transition		–4.62	4.62	–4.62	4.62	ns
SM7	$t_{d(CS\text{-}SIMO)}$	Delay time, mcspi1_cs[3:0] active edge to mcspi1_simo transition	PHA = 0[(1)]		4.62		4.62	ns
SM8	$t_{d(CS\text{-}clk)}$	Delay time, mcspi1_cs[3:0] active to mcspi1_clk[(4)] first edge	PHA = 1[(1)]	A[(5)] – 2.54		A[(5)] – 2.54		ns
			PHA = 0[(1)]	B[(6)] – 2.54		B[(6)] – 2.54		ns
SM9	$t_{d(clk\text{-}CS)}$	Delay time, mcspi1_clk[(4)] last edge to mcspi1_cs[3:0] inactive	PHA = 1[(1)]	B[(6)] – 2.54		B[(6)] – 2.54		ns
			PHA = 0[(1)]	A[(5)] – 2.54		A[(5)] – 2.54		ns
	$t_{R(SIMO)}$	Rise time, mcspi1_simo			10685		10685	ps
	$t_{F(SIMO)}$	Fall time, mcspi1_simo			10685		10685	ps
	$t_{R(CS)}$	Rise time, mcspi1_cs[3:0]			10685		10685	ps
	$t_{F(CS)}$	Fall time, mcspi1_cs[3:0]			10685		10685	ps

(1) The polarity of mcspi1_clk and the active edge (rising or falling) on which mcspi1_simo is driven and mcspi1_somi is latched is all software configurable:
– mcspi1_clk phase programmable with the bit PHA of MCSPI_Ch(i)CONF register: PHA = 1 (Modes 1 and 3).
– mcspi1_clk phase programmable with the bit PHA of MCSPI_Ch(i)CONF register: PHA = 0 (Modes 0 and 2).

For more information, see the McSPI environment chapter, Data Format Configurations section of the OMAP4430 TRM for modes and phase correspondence description.

(2) P = mcspi1_clk clock period

(3) The jitter probability density can be approximated by a Gaussian function.

(4) This timing applies to all configurations regardless of mcspi1_clk polarity and which clock edges are used to drive output data and capture input data.

(5) Case P = 48 MHz: A = (TCS + 1) * $T_{SPICLKREF}$ (TCS is a bit field of MCSPI_Ch(i)CONF register)
Case P < 48 MHz: A = (TCS + 0.5) * F_{RATIO} * $T_{SPICLKREF}$ (TCS is a bit field of MCSPI_Ch(i)CONF register)
For more information, see the McSPI chapter of the OMAP4430 TRM.

(6) B = (TCS + 0.5) * $T_{SPICLKREF}$ * F_{RATIO} (TCS is a bit field of MCSPI_Ch(i)CONF register, F_{RATIO}: Even ≥ 2).
For more information, see the McSPI chapter of the OMAP4430 TRM.

(7) This McSPI1 output clock frequency is based on an output PER DPLL configured at 96 MHz.
For more information regarding the registers configuration, see Power, Reset and Clock Management / Clock Management Functional Description / Internal Clock Sources/Generators / DPLL_PER Description section of the OMAP4430 TRM.

(8) See DM Operating Condition Addendum for CORE OPP voltages.

Table 6-84 and Table 6-85 assume testing over the recommended operating conditions and electrical characteristic conditions below (see Figure 6-68 and Figure 6-69).

Table 6-83. McSPI2 Timing Conditions—Master Mode—24 MHz[(1)(2)(3)]

SYSTEM CONDITION PARAMETER		VALUE		UNIT
		MIN	MAX	
Input Conditions				
t_R	Input signal rise time	100.00	12500.00	ps
t_F	Input signal fall time	100.00	12500.00	ps
PCB Conditions				
	Number of external peripherals		2	
	Far end load		20	pF
	Trace length	1	10	cm
	Characteristics impedance	30	55	Ω

(1) IO settings: MB[1:0] = 10 and LB0 = 1
For more information, see Control Module / Control Module Functional Description/ Functional Register Description / Signal Integrity Parameter Control Registers with Pad Group Assignment / 50-Ω Output Buffer I/Os with Combined Mode and Load Settings section of the OMAP4430 TRM.

(2) In this table the rise and fall times are calculated for 10% to 90% of VDDS. For more information on the corresponding OMAP4 VDDS power supply name, see Table 2-1, POWER [9] column with the ball name.

(3) To have an idea of the output OMAP4 ball load supported for this application, you can consider the following:
Output OMAP4 ball load = Far End load + 1.34 pF/cm typical x trace length (cm).

Table 6-84. McSPI2 Timing Requirements—Master Mode[(2)]

NO.	PARAMETER		OPP100		OPP50		UNIT
			MIN	MAX	MIN	MAX	
SM4	$t_{su(SOMI-clkAE)}$	Setup time, mcspi2_somi valid before mcspi2_clk[(1)] active edge	2.72		2.72		ns
SM5	$t_{h(clkAE-SOMI)}$	Hold time, mcspi2_somi valid after mcspi2_clk[(1)] active edge	2.23		2.23		ns

(1) This timing applies to all configurations regardless of mcspi2_clk polarity and which clock edges are used to drive output data and capture input data.

(2) See DM Operating Condition Addendum for CORE OPP voltages.

Table 6-85. McSPI2 Switching Requirements—Master Mode[(8)]

NO.	PARAMETER			OPP100		OPP50		UNIT
				MIN	MAX	MIN	MAX	
SM1	$1 / t_{c(clk)}$	Frequency[(1)], mcspi2_clk[(4)]			24[(7)]		24[(7)]	MHz
SM2	$t_{w(clkL)}$	Typical pulse duration, mcspi2_clk[(4)] low		0.5*P[(2)]		0.5*P[(2)]		ns
SM3	$t_{w(clkH)}$	Typical pulse duration, mcspi2_clk[(4)] high		0.5*P[(2)]		0.5*P[(2)]		ns
	$t_{dc(clk)}$	Duty cycle error, mcspi2_clk		–2083	2083	–2083	2083	ps
	$t_{j(clk)}$	Jitter standard deviation[(3)], mcspi2_clk			65		65	ps
	$t_{R(clk)}$	Rise time, mcspi2_clk			11853		11853	ps
	$t_{F(clk)}$	Fall time, mcspi2_clk			10446		10446	ps
SM6	$t_{d(clk-SIMO)}$	Delay time, mcspi2_clk[(4)] active edge to mcspi2_simo transition		–4.76	4.76	–4.76	4.76	ns
SM7	$t_{d(CS-SIMO)}$	Delay time, mcspi2_cs[1:0] active edge to mcspi2_simo transition			4.76		4.76	ns
SM8	$t_{d(CS-clk)}$	Delay time, mcspi2_cs[1:0] active to mcspi2_clk[(4)] first edge	PHA = 1[(1)]	A[(5)] – 2.68		A[(5)] – 2.68		ns
			PHA = 0[(1)]	B[(6)] – 2.68		B[(6)] – 2.68		ns
SM9	$t_{d(clk-CS)}$	Delay time, mcspi2_clk[(4)] last edge to mcspi2_cs inactive	PHA = 1[(1)]	B[(6)] – 2.68		B[(6)] – 2.68		ns
			PHA = 0[(1)]	A[(5)] – 2.68		A[(5)] – 2.68		ns
	$t_{R(SIMO)}$	Rise time, mcspi2_simo			11853		11853	ps
	$t_{F(SIMO)}$	Fall time, mcspi2_simo			10446		10446	ps
	$t_{R(CS)}$	Rise time, mcspi2_cs[1:0]			11853		11853	ps
	$t_{F(CS)}$	Fall time, mcspi2_cs[1:0]			10446		10446	ps

(1) The polarity of mcspi2_clk and the active edge (rising or falling) on which mcspi2_simo is driven and mcspi2_somi is latched is all software configurable:

– mcspi2_clk phase programmable with the bit PHA of MCSPI_Ch(i)CONF register: PHA = 1 (Modes 1 and 3).
– mcspi2_clk phase programmable with the bit PHA of MCSPI_Ch(i)CONF register: PHA = 0 (Modes 0 and 2).

For more information, see the McSPI environment chapter, Data Format Configurations section of the OMAP4430 TRM for modes and phase correspondence description.

(2) P = mcspi2_clk clock period

(3) The jitter probability density can be approximated by a Gaussian function.

(4) This timing applies to all configurations regardless of mcspi2_clk polarity and which clock edges are used to drive output data and capture input data.

(5) Case P = 48 MHz: A = (TCS + 1) * $T_{SPICLKREF}$ (TCS is a bit field of MCSPI_Ch(i)CONF register)
Case P < 48 MHz: A = (TCS + 0.5) * F_{RATIO} * $T_{SPICLKREF}$ (TCS is a bit field of MCSPI_Ch(i)CONF register)
For more information, see the McSPI chapter of the OMAP4430 TRM.

(6) B = (TCS + 0.5) * $T_{SPICLKREF}$ * F_{RATIO} (TCS is a bit field of MCSPI_Ch(i)CONF register, F_{RATIO}: Even ≥ 2).
For more information, see the McSPI chapter of the OMAP4430 TRM.

(7) This McSPI2 output clock frequency is based on an output PER DPLL configured at 96 MHz.
For more information regarding the registers configuration, see Power, Reset and Clock Management / Clock Management Functional Description / Internal Clock Sources/Generators / DPLL_PER Description section of the OMAP4430 TRM.

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(8) See DM Operating Condition Addendum for CORE OPP voltages.

6.6.3.2.2 McSPI2, McSPI3, and McSPI4—Master Mode—48-MHz Frequency Clock

6.6.3.2.2.1 McSPI2

Table 6-87 and Table 6-88 assume testing over the recommended operating conditions and electrical characteristic conditions below (see Figure 6-68 and Figure 6-69).

Table 6-86. McSPI2 Timing Conditions—Master Mode—48 MHz(1)(2)(3)

SYSTEM CONDITION PARAMETER		VALUE		UNIT
		MIN	MAX	
Input Conditions				
t_R	Input signal rise time	1.00	4.00	ns
t_F	Input signal fall time	1.00	4.00	ns
PCB Conditions				
	Number of external peripherals		1	
	Far end load		5	pF
	Trace length	1	5	cm
	Characteristics impedance	30	60	Ω

(1) IO settings: LB0 = 1 and MB[1:0] = 11
For more information, see Control Module / Control Module Functional Description/ Functional Register Description / Signal Integrity Parameter Control Registers with Pad Group Assignment / 50-Ω Output Buffer I/Os with Combined Mode and Load Settings section of the OMAP4430 TRM.

(2) In this table the rise and fall times are calculated for 10% to 90% of VDDS. For more information on the corresponding OMAP4 VDDS power supply name, see Table 2-1, POWER [9] column with the ball name.

(3) To have an idea of the output OMAP4 ball load supported for this application, you can consider the following:
Output OMAP4 ball load = Far End load + 1.34 pF/cm typical x trace length (cm).

Table 6-87. McSPI2 Timing Requirements—Master Mode(2)

NO.	PARAMETER		OPP100		OPP50		UNIT
			MIN	MAX	MIN	MAX	
SM4	$t_{su(SOMI-CLKAE)}$	Setup time, mcspi2_somi valid before mcspi2_clk(1) active edge	2.57		2.57		ns
SM5	$t_{h(clkAE-SOMI)}$	Hold time, mcspi2_somi valid after mcspi2_clk(1) active edge	2.53		2.53		ns

(1) This timing applies to all configurations regardless of mcspi_clk polarity and which clock edges are used to drive output data and capture input data.

(2) See DM Operating Condition Addendum for CORE OPP voltages.

Table 6-88. McSPI2 Switching Requirements—Master Mode(8)

NO.	PARAMETER		OPP100		OPP50		UNIT
			MIN	MAX	MIN	MAX	
SM1	$1 / t_{c(clk)}$	Frequency(1), mcspi2_clk(4)		48(7)		48(7)	MHz
SM2	$t_{w(clkL)}$	Typical pulse duration, mcspi2_clk(4) low	0.5*P(2)		0.5*P(2)		ns
SM3	$t_{w(clkH)}$	Typical pulse duration, mcspi2_clk(4) high	0.5*P(2)		0.5*P(2)		ns
	$t_{dc(clk)}$	Duty cycle error, mcspi2_clk	–1042	1042	–1042	1042	ps
	$t_{j(clk)}$	Jitter standard deviation(3), mcspi2_clk		65		65	ps
	$t_{R(clk)}$	Rise time, mcspi2_clk		4077.0		4077.0	ps
	$t_{F(clk)}$	Fall time, mcspi2_clk		4077.0		4077.0	ps
SM6	$t_{d(clk-SIMO)}$	Delay time, mcspi2_clk(4) active edge to mcspi2_simo transition	–3.55	3.55	–3.55	3.55	ns

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Table 6-88. McSPI2 Switching Requirements—Master Mode[8] (continued)

NO.	PARAMETER			OPP100		OPP50		UNIT
				MIN	MAX	MIN	MAX	
SM7	$t_{d(CS-SIMO)}$	Delay time, mcspi2_cs0 active edge to mcspi2_simo transition	PHA = 0[1]		3.55		3.55	ns
SM8	$t_{d(CS-clk)}$	Delay time, mcspi2_cs0 active to mcspi2_clk[4] first edge	PHA = 1[1]	A[5] – 4.18		A[5] – 4.18		
			PHA = 0[1]	B[6] – 4.18		B[6] – 4.18		
SM9	$t_{d(clk-CS)}$	Delay time, mcspi2_clk[4] last edge to mcspi2_cs0 inactive	PHA = 1[1]	B[6] – 4.18		B[6] – 4.18		
			PHA = 0[1]	A[5] – 4.18		A[5] – 4.18		
	$t_{R(SIMO)}$	Rise time, mcspi2_simo			4077.0		4077.0	ps
	$t_{F(SIMO)}$	Fall time, mcspi2_simo			4077.0		4077.0	ps
	$t_{R(CS)}$	Rise time, mcspi2_cs0			4077.0		4077.0	ps
	$t_{F(CS)}$	Fall time, mcspi2_cs0			4077.0		4077.0	ps

(1) The polarity of mcspi2_clk and the active edge (rising or falling) on which mcspi2_simo is driven and mcspi2_somi is latched is all software configurable:
- mcspi2_clk phase programmable with the bit PHA of MCSPI_Ch(i)CONF register: PHA = 1 (Modes 1 and 3).
- mcspi2_clk phase programmable with the bit PHA of MCSPI_Ch(i)CONF register: PHA = 0 (Modes 0 and 2).

For more information, see the McSPI environment chapter, Data Format Configurations section of the OMAP4430 TRM for modes and phase correspondence descriptions.

(2) P = mcspi2_clk clock period

(3) The jitter probability density can be approximated by a Gaussian function.

(4) This timing applies to all configurations regardless of mcspi2_clk polarity and which clock edges are used to drive output data and capture input data.

(5) Case P = 48 MHz: A = (TCS + 1) * $T_{SPICLKREF}$ (TCS is a bit field of MCSPI_Ch(i)CONF register)
Case P < 48 MHz: A = (TCS + 0.5) * F_{RATIO} * $T_{SPICLKREF}$ (TCS is a bit field of MCSPI_Ch(i)CONF register)
For more information, see the McSPI chapter of the OMAP4430 TRM.

(6) B = (TCS + 0.5) * $T_{SPICLKREF}$ * F_{RATIO} (TCS is a bit field of MCSPI_Ch(i)CONF register, F_{RATIO}: Even ≥ 2).
For more information, see the McSPI chapter of the OMAP4430 TRM.

(7) This McSPI2 output clock frequency is based on an output PER DPLL configured at 96 MHz.
For more information regarding the registers configuration, see Power, Reset and Clock Management / Clock Management Functional Description / Internal Clock Sources/Generators / DPLL_PER Description section of the OMAP4430 TRM.

(8) See DM Operating Condition Addendum for CORE OPP voltages.

6.6.3.2.2.2 McSPI3

Table 6-90 and Table 6-91 assume testing over the recommended operating conditions and electrical characteristic conditions below (see Figure 6-68 and Figure 6-69).

Table 6-89. McSPI3 Timing Conditions—Master Mode[1][2][3]

SYSTEM CONDITION PARAMETER		VALUE		UNIT
		MIN	MAX	
Input Conditions				
t_R	Input signal rise time	1000	4000	ps
t_F	Input signal fall time	1000	4000	ps
PCB Conditions				
	Number of external peripherals		1	
	Far end load		5	pF
	Trace length	1	7	cm
	Characteristics impedance	40	55	Ω

(1) IO settings: DS0 = 0.
For more information, see Control Module / Control Module Functional Description/ Functional Register Description / Signal Integrity Parameter Control Registers with Pad Group Assignment / I/O cells with Configurable Output Driver Impedance section of the OMAP4430 TRM.

(2) In this table the rise and fall times are calculated for 10% to 90% of VDDS. For more information on the corresponding OMAP4 VDDS power supply name, see Table 2-1, POWER [9] column with the ball name.

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(3) To have an idea of the output OMAP4 ball load supported for this application, you can consider the following: Output OMAP4 ball load = Far End load + 1.34 pF/cm typical x trace length (cm).

Table 6-90. McSPI3 Timing Requirements—Master Mode[(2)]

NO.	PARAMETER		OPP100		OPP50		UNIT
			MIN	MAX	MIN	MAX	
SM4	$t_{su(SOMI-CLKAE)}$	Setup time, mcspi3_somi valid before mcspi3_clk[(1)] active edge	2.29		2.29		ns
SM5	$t_{h(clkAE-SOMI)}$	Hold time, mcspi3_somi valid after mcspi3_clk[(1)] active edge	2.67		2.67		ns

(1) This timing applies to all configurations regardless of mcspi_clk polarity and which clock edges are used to drive output data and capture input data.

(2) See DM Operating Condition Addendum for CORE OPP voltages.

Table 6-91. McSPI3 Switching Requirements—Master Mode[(8)]

NO.	PARAMETER			OPP100		OPP50		UNIT
				MIN	MAX	MIN	MAX	
SM1	$1 / t_{c(clk)}$	Frequency[(1)], mcspi3_clk[(4)]			48[(7)]		48[(7)]	MHz
SM2	$t_{w(clkL)}$	Typical pulse duration, mcspi3_clk[(4)] low		0.5*P[(2)]		0.5*P[(2)]		ns
SM3	$t_{w(clkH)}$	Typical pulse duration, mcspi3_clk[(4)] high		0.5*P[(2)]		0.5*P[(2)]		ns
	$t_{dc(clk)}$	Duty cycle error, mcspi3_clk		–1042	1042	–1042	1042	ps
	$t_{j(clk)}$	Jitter standard deviation[(3)], mcspi3_clk			65		65	ps
	$t_{R(clk)}$	Rise time, mcspi3_clk			3820.4		3820.4	ps
	$t_{F(clk)}$	Fall time, mcspi3_clk			3442.4		3442.4	ps
SM6	$t_{d(clk-SIMO)}$	Delay time, mcspi3_clk[(4)] active edge to mcspi3_simo transition		–3.57	3.57	–3.57	3.57	ns
SM7	$t_{d(CS-SIMO)}$	Delay time, mcspi3_cs0 active edge to mcspi3_simo transition			3.57		3.57	ns
SM8	$t_{d(CS-clk)}$	Delay time, mcspi3_cs0 active to mcspi3_clk[(4)] first edge	PHA = 1[(1)]	A[(5)] – 4.2		A[(5)] – 4.2		ns
			PHA = 0[(1)]	B[(6)] – 4.2		B[(6)] – 4.2		ns
SM9	$t_{d(clk-CS)}$	Delay time, mcspi3_clk[(4)] last edge to mcspi3_cs0 inactive	PHA = 1[(1)]	B[(6)] – 4.2		B[(6)] – 4.2		ns
			PHA = 0[(1)]	A[(5)] – 4.2		A[(5)] – 4.2		ns
	$t_{R(SIMO)}$	Rise time, mcspi3_simo			3820.4		3820.4	ps
	$t_{F(SIMO)}$	Fall time, mcspi3_simo			3442.4		3442.4	ps
	$t_{R(CS)}$	Rise time, mcspi3_cs0			3820.4		3820.4	ps
	$t_{F(CS)}$	Fall time, mcspi3_cs0			3442.4		3442.4	ps

(1) The polarity of mcspi3_clk and the active edge (rising or falling) on which mcspi3_simo is driven and mcspi3_somi is latched is all software configurable:

– mcspi3_clk phase programmable with the bit PHA of MCSPI_Ch(i)CONF register: PHA = 1 (Modes 1 and 3).
– mcspi3_clk phase programmable with the bit PHA of MCSPI_Ch(i)CONF register: PHA = 0 (Modes 0 and 2).

For more information, see the McSPI environment chapter, Data Format Configurations section of the OMAP4430 TRM for modes and phase correspondence descriptions.

(2) P = mcspi3_clk clock period

(3) The jitter probability density can be approximated by a Gaussian function.

(4) This timing applies to all configurations regardless of mcspi3_clk polarity and which clock edges are used to drive output data and capture input data.

(5) Case P = 48 MHz: A = (TCS + 1) * $T_{SPICLKREF}$ (TCS is a bit field of MCSPI_Ch(i)CONF register)
Case P < 48 MHz: A = (TCS + 0.5) * F_{RATIO} * $T_{SPICLKREF}$ (TCS is a bit field of MCSPI_Ch(i)CONF register)
For more information, see the McSPI chapter of the OMAP4430 TRM.

(6) B = (TCS + 0.5) * $T_{SPICLKREF}$ * F_{RATIO} (TCS is a bit field of MCSPI_Ch(i)CONF register, F_{RATIO}: Even ≥ 2).
For more information, see the McSPI chapter of the OMAP4430 TRM.

(7) This McSPI3 output clock frequency is based on an output PER DPLL configured at 96 MHz.
For more information regarding the registers configuration, see Power, Reset and Clock Management / Clock Management Functional Description / Internal Clock Sources/Generators / DPLL_PER Description section of the OMAP4430 TRM.

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(8) See DM Operating Condition Addendum for CORE OPP voltages.

6.6.3.2.2.3 McSPI4

Table 6-93 and Table 6-94 assume testing over the recommended operating conditions and electrical characteristic conditions below (see Figure 6-68 and Figure 6-69).

Table 6-92. McSPI4 Timing Conditions—Master Mode[2][3]

SYSTEM CONDITION PARAMETER		VALUE		UNIT
		MIN	MAX	
Input Conditions				
t_R	Input signal rise time	1.00	4.00	ns
t_F	Input signal fall time	1.00	4.00	ns
PCB Conditions				
	Number of external peripherals		1	
	Far end load		5	pF
	Trace length	1	8	cm
	Characteristics impedance	40	55	Ω

(1) IO settings: LB0 = 1 and MB[1:0] = 11
For more information, see Control Module / Control Module Functional Description/ Functional Register Description / Signal Integrity Parameter Control Registers with Pad Group Assignment / 50-Ω Output Buffer I/Os with Combined Mode and Load Settings section of the OMAP4430 TRM.

(2) In this table the rise and fall times are calculated for 10% to 90% of VDDS. For more information on the corresponding OMAP4 VDDS power supply name, see Table 2-1, POWER [9] column with the ball name.

(3) To have an idea of the output OMAP4 ball load supported for this application, you can consider the following:
Output OMAP4 ball load = Far End load + 1.34 pF/cm typical x trace length (cm).

Table 6-93. McSPI4 Timing Requirements—Master Mode[2]

NO.	PARAMETER		OPP100		OPP50		UNIT
			MIN	MAX	MIN	MAX	
SM4	$t_{su(SOMI-CLKAE)}$	Setup time, mcspi4_somi valid before mcspi4_clk[1] active edge	2.27		2.27		ns
SM5	$t_{h(clkAE-SOMI)}$	Hold time, mcspi4_somi valid after mcspi4_clk[1] active edge	2.67		2.67		ns

(1) This timing applies to all configurations regardless of mcspi_clk polarity and which clock edges are used to drive output data and capture input data.

(2) See DM Operating Condition Addendum for CORE OPP voltages.

Table 6-94. McSPI4 Switching Requirements—Master Mode[8]

NO.	PARAMETER		OPP100		OPP50		UNIT
			MIN	MAX	MIN	MAX	
SM1	$1 / t_{c(clk)}$	Frequency[1], mcspi4_clk[4]		48[7]		48[7]	MHz
SM2	$t_{w(clkL)}$	Typical pulse duration, mcspi4_clk[4] low	0.5*P[2]		0.5*P[2]		ns
SM3	$t_{w(clkH)}$	Typical pulse duration, mcspi4_clk[4] high	0.5*P[2]		0.5*P[2]		ns
	$t_{dc(clk)}$	Duty cycle error, mcspi4_clk	–1042	1042	–1042	1042	ps
	$t_{j(clk)}$	Jitter standard deviation[3], mcspi4_clk		65		65	ps
	$t_{R(clk)}$	Rise time, mcspi4_clk		4085.0		4085.0	ps
	$t_{F(clk)}$	Fall time, mcspi4_clk		4085.0		4085.0	ps
SM6	$t_{d(clk-SIMO)}$	Delay time, mcspi4_clk[4] active edge to mcspi4_simo transition	–3.43	3.43	–3.43	3.43	ns
SM7	$t_{d(CS-SIMO)}$	Delay time, mcspi4_cs0 active edge to mcspi4_simo transition		3.43		3.43	ns

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Table 6-94. McSPI4 Switching Requirements—Master Mode[(8)] (continued)

NO.	PARAMETER			OPP100		OPP50		UNIT
				MIN	MAX	MIN	MAX	
SM8	$t_{d(CS-clk)}$	Delay time, mcspi4_cs0 active to mcspi4_clk[(4)] first edge	PHA = 1[(1)]	A[(5)] – 4.06		A[(5)] – 4.06		ns
			PHA = 0[(1)]	B[(6)] – 4.06		B[(6)] – 4.06		ns
SM9	$t_{d(clk-CS)}$	Delay time, mcspi4_clk[(4)] last edge to mcspi4_cs inactive	PHA = 1[(1)]	B[(6)] – 4.06		B[(6)] – 4.06		ns
			PHA = 0[(1)]	A[(5)] – 4.06		A[(5)] – 4.06		ns
	$t_{R(SIMO)}$	Rise time, mcspi4_simo			4085.0		4085.0	ps
	$t_{F(SIMO)}$	Fall time, mcspi4_simo			4085.0		4085.0	ps
	$t_{R(CS)}$	Rise time, mcspi4_cs0			4085.0		4085.0	ps
	$t_{F(CS)}$	Fall time, mcspi4_cs0			4085.0		4085.0	ps

(1) The polarity of mcspi4_clk and the active edge (rising or falling) on which mcspi4_simo is driven and mcspi4_somi is latched is all software configurable:

– mcspi4_clk phase programmable with the bit PHA of MCSPI_Ch(i)CONF register: PHA = 1 (Modes 1 and 3).
– mcspi4_clk phase programmable with the bit PHA of MCSPI_Ch(i)CONF register: PHA = 0 (Modes 0 and 2).

For more information, see the McSPI environment chapter, Data Format Configurations section of the OMAP4430 TRM for modes and phase correspondence descriptions.

(2) P = mcspi4_clk clock period

(3) The jitter probability density can be approximated by a Gaussian function.

(4) This timing applies to all configurations regardless of mcspi4_clk polarity and which clock edges are used to drive output data and capture input data.

(5) Case P = 48 MHz: A = (TCS + 1) * $T_{SPICLKREF}$ (TCS is a bit field of MCSPI_Ch(i)CONF register)
Case P < 48 MHz: A = (TCS + 0.5) * F_{RATIO} * $T_{SPICLKREF}$ (TCS is a bit field of MCSPI_Ch(i)CONF register)
For more information, see the McSPI chapter of the OMAP4430 TRM.

(6) B = (TCS + 0.5) * $T_{SPICLKREF}$ * F_{RATIO} (TCS is a bit field of MCSPI_Ch(i)CONF register, F_{RATIO}: Even ≥ 2).
For more information, see the McSPI chapter of the OMAP4430 TRM.

(7) This McSPI4 output clock frequency is based on an output PER DPLL configured at 96 MHz.
For more information regarding the registers configuration, see Power, Reset and Clock Management / Clock Management Functional Description / Internal Clock Sources/Generators / DPLL_PER Description section of the OMAP4430 TRM.

(8) See DM Operating Condition Addendum for CORE OPP voltages.

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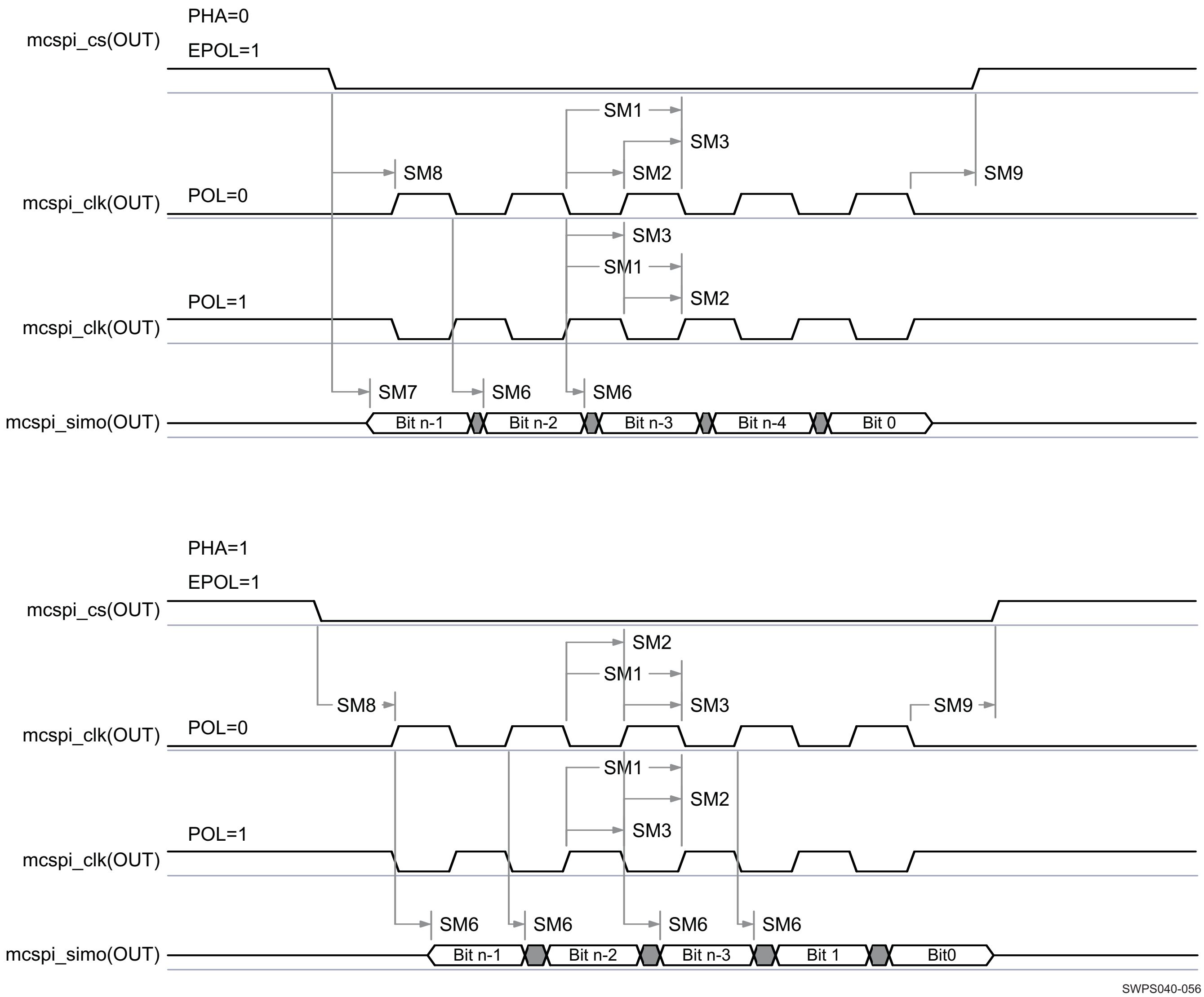

Figure 6-68. McSPI—Master Mode—Transmit(1)(2)(3)

(1) The active clock edge selection of mcspi_clk (rising or falling) on which mcspi_simo is driven and mcspi_somi data is latched is software configurable with the bit MCSPI_Ch(i)CONF[1] = POL and the bit MCSPI_Ch(i)CONF[0] = PHA.

(2) The polarity of mcspi_ncs is software configurable with the bit MCSPI_Ch(i)CONF[6] = EPOL.

(3) In mcspix, x is equal to 1, 2, 3, or 4.

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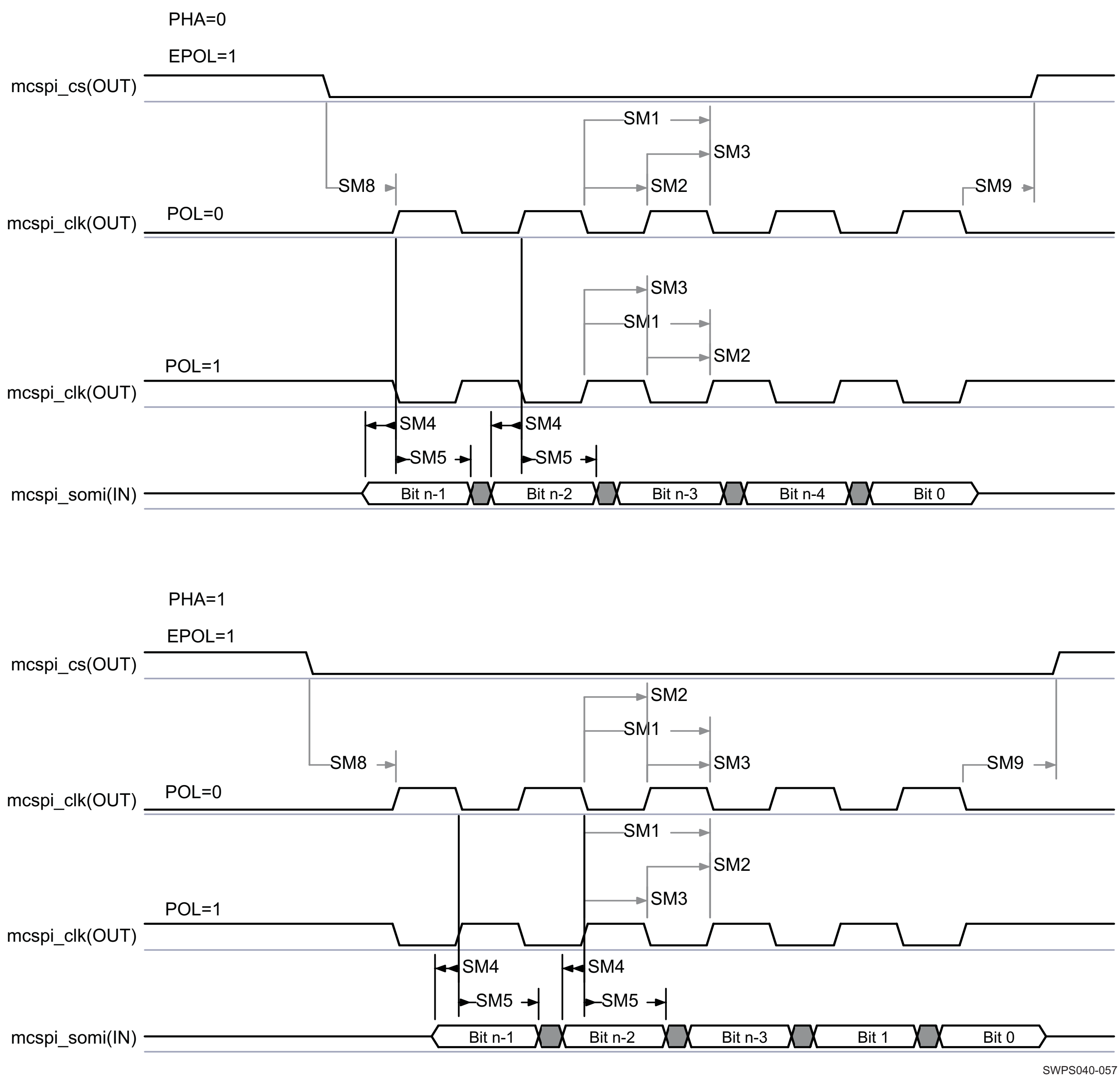

Figure 6-69. McSPI—Master Mode—Transmit(1)(2)(3)

(1) The active clock edge selection of mcspi_clk (rising or falling) on which mcspi_simo is driven and mcspi_somi data is latched is software configurable with the bit MCSPI_Ch(i)CONF[1] = POL and the bit MCSPI_Ch(i)CONF[0] = PHA.

(2) The polarity of mcspi_ncs is software configurable with the bit MCSPI_Ch(i)CONF[6] = EPOL.

(3) In mcspix, x is equal to 1, 2, 3, or 4.

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6.6.4 Digital Microphone (DMIC)

NOTE

For more information, see the Digital Microphone Controller chapter in the OMAP4430 TRM.

The DMIC allows support of up to three digital stereo microphones that send it a pulse-density modulated stream of bits, transferred on one period or one half-period of the clock (over-sampling clock) provided to the DMIC.

Table 6-96 and Table 6-97 assume testing over the recommended operating conditions and electrical characteristic conditions below (see Figure 6-71).

Table 6-95. DMIC Timing Conditions—Master/Receive Mode(1)(2)(4)

TIMING CONDITION PARAMETER		VALUE		UNIT
		MIN	MAX	
Input Conditions				
t_R	Input signal rise time		10	ns
t_F	Input signal fall time		10	ns
PCB Conditions (3)				
	Number of external peripherals		See(5)	
	Far end load when accounting for external ESD protection		20	pF
	Trace length		25	cm
	Characteristics impedance	40	70	Ω

(1) IO settings: LB0 = 0 and MB[1:0] = 10
- For balls AE24 / AF24 / AG24 / AH24 (abe_dmic_clk1 / abe_dmic_din1 / abe_dmic_din2 / abe_dmic_din3 in multiplexing mode 0), for more information see Control Module / Control Module Functional Description/ Functional Register Description / Signal Integrity Parameter Control Registers with Pad Group Assignment / 50-Ω Output Buffer I/Os with Combined Mode and Load Settings section of the OMAP4430 TRM.
- For balls AF16 / AG16 (abe_dmic_din3 / abe_dmic_clk3 in multiplexing mode 5), see Control Module / Control Module Functional Description/ Functional Register Description / Signal Integrity Parameter Control Registers with Pad Group Assignment / I/Os with Combined Mode and Load Settings section of the OMAP4430 TRM.

(2) In this table the rise and fall times are calculated for 20% to 80% of VDDS. For more information on the corresponding OMAP4 VDDS power supply name, see Table 2-1, POWER [9] column with the ball name.

(3) Figure 6-70 shows an example of DMIC implementation.

(4) To have an idea of the output OMAP4 ball load supported for this application, you can consider the following:
Output OMAP4 ball load = Far End load + 1.34 pF/cm typical x trace length (cm).

(5) For more information on the peripheral conditions, see Figure 6-70, *DMIC Implementation Example.*

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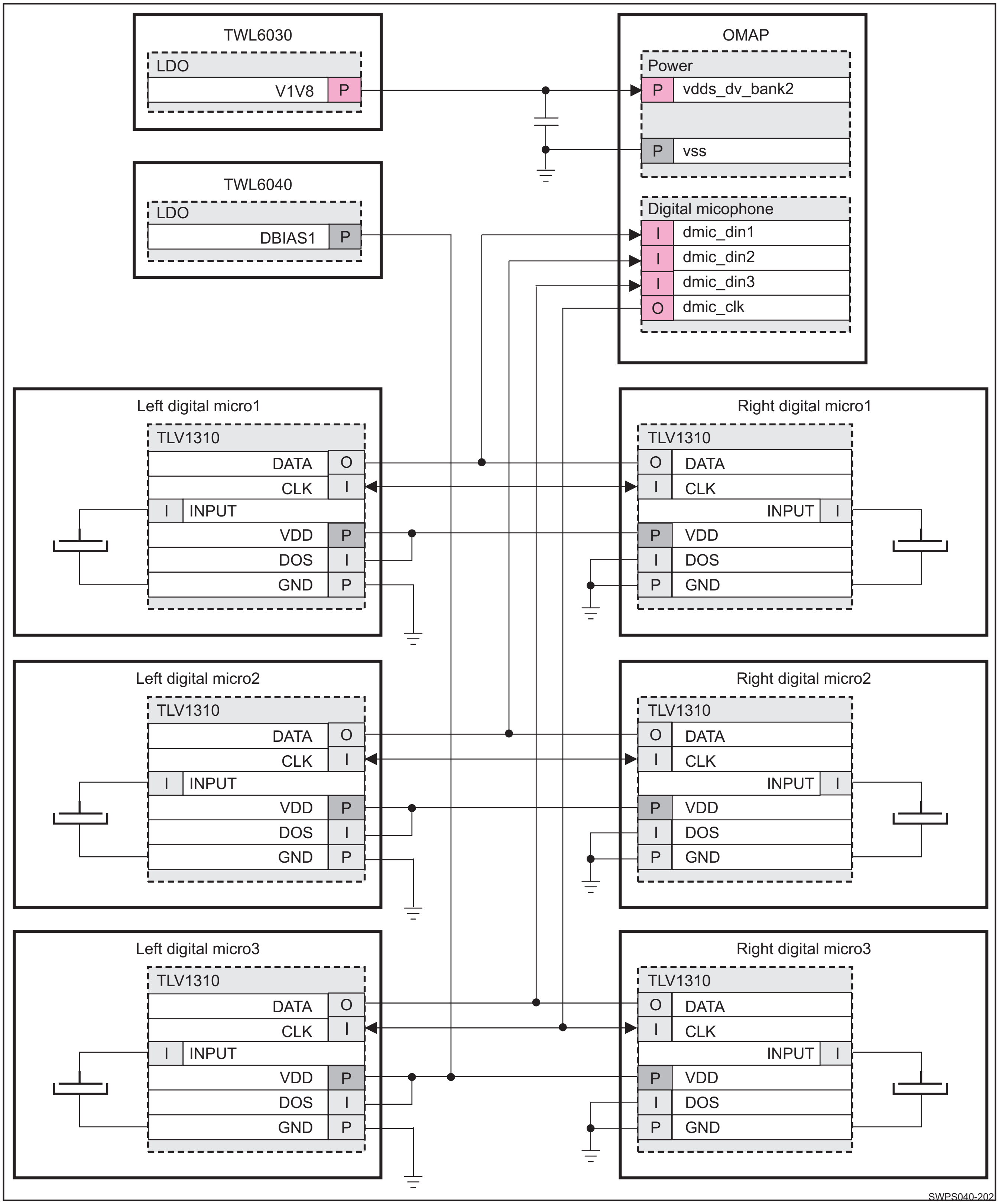

Figure 6-70. DMIC Implementation Example[(1)]

(1) It is also possible to use different PCB guideline clock outputs rather than sharing one as described in above implementation example. In such case, each pair (pair [3:1]) of digital microphone can be connected to a dedicated data and clock signals (dmic_din[3:1],

dmic_clk[3:1]). This way each microphone is turned off independently from each others.

Table 6-96. DMIC Timing Requirements—Master/Receive Mode

NO.	PARAMETER		OPP100		OPP50		UNIT
			MIN	MAX	MIN	MAX	
DMIC4	$t_{su(dV-clkH)}$	Setup time, input abe_dmic_din[3:1] valid before abe_dmic_clk[3:1] rising/falling edge	72.3		72.3		ns
DMIC5	$t_{h(clkH-dV)}$	Hold time, output abe_dmic_din[3:1] valid after abe_dmic_clk[3:1] rising/falling edge	–0.7		–0.7		ns

Table 6-97. DMIC Switching Characteristics—Master/Receive Mode[(4)]

NO.	PARAMETER		OPP100		OPP50		UNIT
			MIN	MAX	MIN	MAX	
DMIC1	$1 / t_{c(clk)}$	Frequency[(1)] output dmic clock abe_dmic_clk[3:1]		3.84		3.84	MHz
DMIC2	$t_{w(clkL)}$	Pulse duration, output dmic clock abe_dmic_clk[3:1] low	0.5*P[(2)]		0.5*P[(2)]		ns
DMIC3	$t_{w(clkH)}$	Pulse duration, output dmic clock abe_dmic_clk[3:1] high	0.5*P[(2)]		0.5*P[(2)]		ns
	$t_{dc(clk)}$	Duty cycle error, output dmic clock abe_dmic_clk[3:1]		13		13	ns
	$t_{j(clk)}$	Jitter standard deviation[(3)], output dmic clock abe_dmic_clk[3:1]		67		67	ns
	$t_{R(clk)}$	Rise time, output dmic clock abe_dmic_clk[3:1]		10		10	ns
	$t_{F(clk)}$	Fall time, output dmic clock abe_dmic_clk[3:1]		10		10	ns

(1) Related to the output abe_dmic_clk[3:1] maximum frequency programmable.
(2) P = output abe_dmic_clk[3:1] period in ns
(3) The jitter probability density can be approximated by a Gaussian function.
(4) See DM Operating Condition Addendum for CORE OPP voltages.

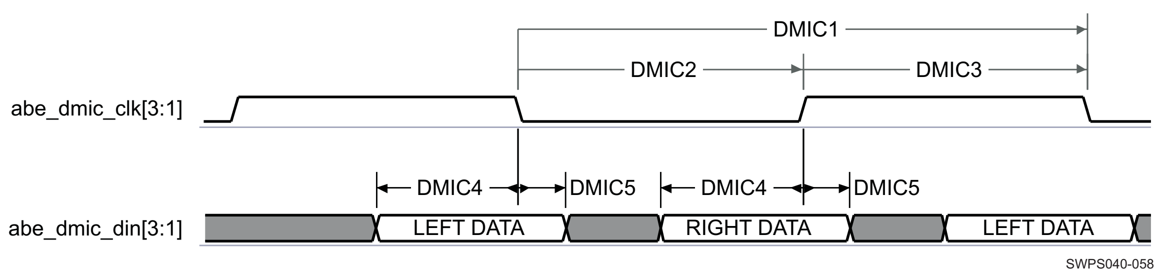

Figure 6-71. DMIC—Master DDR Receive Mode[(1)]

(1) RIGHT/LEFT DATA capturing edges depend on the DOS DMIC pin implementation.

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6.6.5 Multichannel Pulse Density Modulation (McPDM)

Multichannel pulse density modulation interface (McPDM) is an audio module dedicated to mobile telephone terminal. It's composed of uplink and downlink paths both communicating with audio companion chip through a dedicated interface. Aim of the uplink path is to process data from the McPDM interface, decimate and filter the data, and store them in FIFO. FIFO will be controlled by IRQ or DMA request and fed outside from McPDM module following standard OCP format.

Aim of the downlink path is to process data coming from FIFO, through sigma-delta converter and feed it to McPDM interface. The data is also transmitted to audio companion chip by operating a sample frequency conversion.

Table 6-99 and Table 6-100 assume testing over the recommended operating conditions and electrical characteristic conditions below (see Figure 6-72 and Figure 6-73).

Table 6-98. McPDM Timing Conditions(1)(2)(3)

SYSTEM CONDITION PARAMETER		VALUE		UNIT
		MIN	MAX	
Input Conditions				
t_R	Input signal rise time	1.00	6.00	ns
t_F	Input signal fall time	1.00	6.00	ns
PCB Conditions				
	Number of external peripherals		1	
	Far end load		5	pF
	Trace length		5	cm
	Characteristics impedance	20	65	Ω

(1) IO settings: MB[1:0]= 01 and LB0 = 0
For more information, see Control Module / Control Module Functional Description/ Functional Register Description / Signal Integrity Parameter Control Registers with Pad Group Assignment / 50-Ω Output Buffer I/Os with Combined Mode and Load Settings section of the OMAP4430 TRM.

(2) In this table the rise and fall times are calculated for 10% to 90% of VDDS. For more information on the corresponding OMAP4 VDDS power supply name, see Table 2-1, POWER [9] column with the ball name.

(3) To have an idea of the output OMAP4 ball load supported for this application, you can consider the following:
Output OMAP4 ball load = Far End load + 1.34 pF/cm typical x trace length (cm).

Table 6-99. McPDM Timing Requirements—Master and Receive SDR Mode(1)

NO.	PARAMETER		OPP100		OPP50		UNIT
			MIN	MAX	MIN	MAX	
	$f_{c(clks)}$	Input abe_clks frequency		19.2		19.2	MHz
PDM6	$t_{su(ulV-clkH)}$	Setup time, abe_pdm_ul_data valid before abe_pdm_lb_clk rising edge	21.68		21.68		ns
PDM7	$t_{h(clkH-ulV)}$	Hold time, abe_pdm_ul_data valid after abe_pdm_lb_clk rising edge	0.10		0.10		ns
PDM8	$t_{su(frameV-clkH)}$	Setup time, abe_pdm_frame valid before abe_pdm_lb_clk rising edge	21.68		21.68		ns
PDM9	$t_{h(clkH-frameV)}$	Hold time, abe_pdm_frame valid after abe_pdm_lb_clk rising edge	0.10		0.10		ns

(1) See DM Operating Condition Addendum for CORE OPP voltages.

Table 6-100. McPDM Switching Characteristics—Master and Transmit SDR Mode(4)(5)

NO.	PARAMETER		OPP100		OPP50		UNIT
			MIN	MAX	MIN	MAX	
PDM1	$1 / t_{c(clk)}$	Frequency[1] output abe_pdm_lb_clk clock		19.2		19.2	MHz

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Table 6-100. McPDM Switching Characteristics—Master and Transmit SDR Mode(4)(5) (continued)

NO.	PARAMETER		OPP100 MIN	OPP100 MAX	OPP50 MIN	OPP50 MAX	UNIT
PDM2	$t_{w(clkH)}$	Typical pulse duration, output abe_pdm_lb_clk high	0.5*P(2)		0.5*P(2)		ns
PDM3	$t_{w(clkL)}$	Typical pulse duration, output abe_pdm_lb_clk low	0.5*P(2)		0.5*P(2)		ns
	$t_{dc(clk)}$	Duty cycle error, output abe_pdm_lb_clk	–2604	2604	–2604	2604	ps
	$t_{j(clk)}$	Jitter standard deviation(3), output abe_pdm_lb_clk		434		434	ps
	$t_{R(clk)}$	Rise time, output abe_pdm_lb_clk		5		5	ns
	$t_{F(clk)}$	Fall time, output abe_pdm_lb_clk		5		5	ns
PDM4	$t_{d(clkH-dlV)}$	Delay time, output abe_pdm_lb_clk high to output abe_pdm_dl_data valid	1.45	33.03	1.45	33.03	ns
PDM5	$t_{d(clkH-frameV)}$	Delay time, output abe_pdm_lb_clk high to output abe_pdm_frame valid	1.45	33.03	1.45	33.03	ns
	$t_{R(dl)}$	Rise time, output abe_pdm_dl_data		5		5	ns
	$t_{F(dl)}$	Fall time, output abe_pdm_dl_data		5		5	ns
	$t_{R(frame)}$	Rise time, output abe_pdm_frame		5		5	ns
	$t_{F(frame)}$	Fall time, output abe_pdm_frame		5		5	ns

(1) Related to the output clk maximum frequency.
(2) P = output clk period in ns
(3) The jitter probability density can be approximated by a Gaussian function.
(4) The timing requirements are assured for the Jitter standard deviation and duty cycle error conditions specified.
(5) See DM Operating Condition Addendum for CORE OPP voltages.

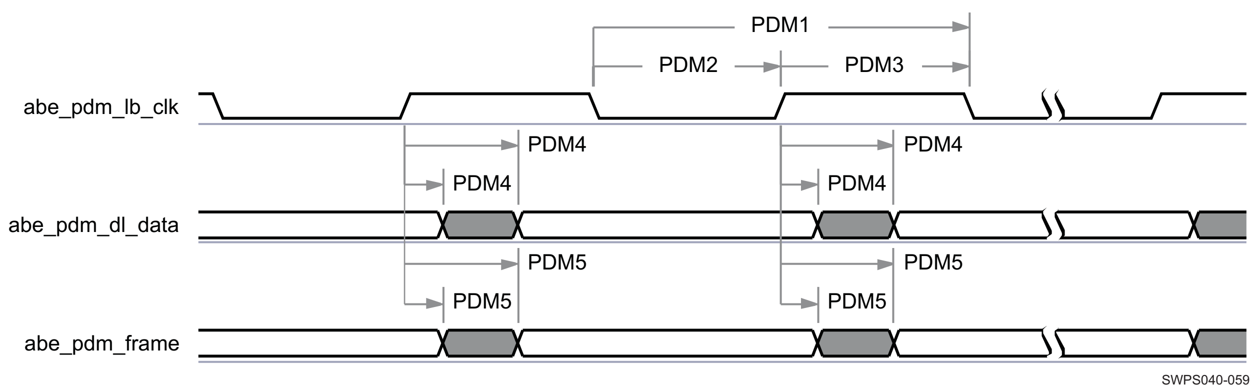

Figure 6-72. McPDM—Master Transmit SDR Mode

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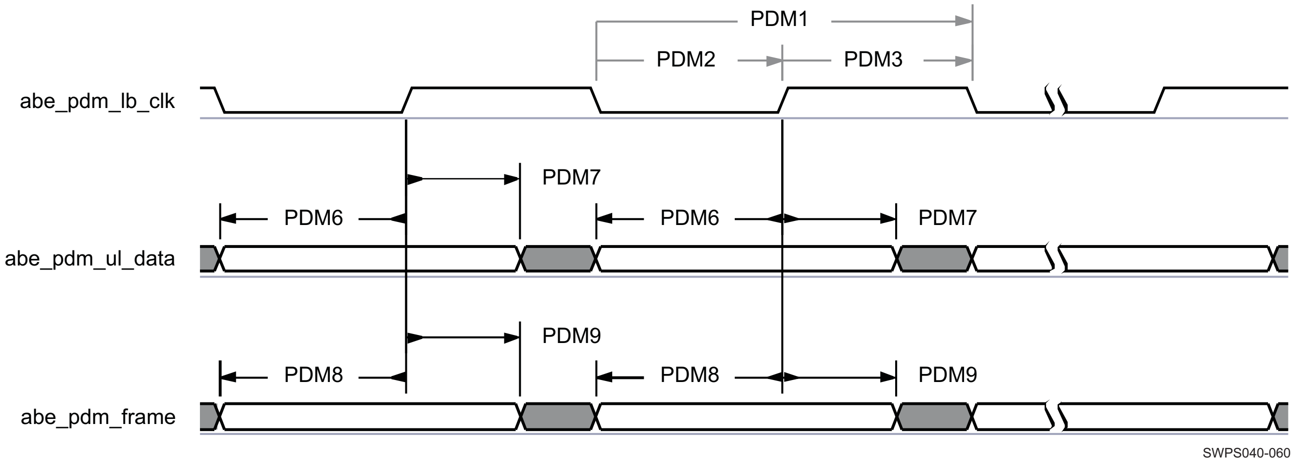

Figure 6-73. McPDM—Master Receive SDR Mode

6.6.6 SlimBus

NOTE

For more information, see the Serial Communication Interface / Serial Low-Power Inter-Chip Media Bus Controller section of the OMAP4430 TRM.

The SlimBus controller provides a bidirectional, multidrop, multichannel, two-line serial interface between the OMAP4430 chip and external components in a system such as audio codecs, Bluetooth® module, FM radio receiver/transmitter. It can accommodate a wide range of peripherals and clocked frame-oriented protocols (I2S, PCM, TDM) due to its high level of versatility.

6.6.6.1 ABE SlimBus1, SlimBus2—SLIMBUS SDR 24.6 MHz

Table 6-102 and Table 6-103 assume testing over the recommended operating conditions and electrical characteristic conditions below (see Figure 6-74 and Figure 6-75).

Table 6-101. ABE SlimBus1, SlimBus2 Timing Conditions(1)(2)(3)

SYSTEM CONDITION PARAMETER		VALUE		UNIT
		MIN	MAX	
Input Conditions				
t_R	Input signal rise time	1.2		ps
t_F	Input signal fall time	1.2		ps
PCB Conditions				
	Number of external peripherals		3	
	Far end load		15	pF
	Trace length		10	cm
	Characteristics impedance	30	60	Ω

(1) IO settings: MB[1:0] = 11 and LB0 = 1.
- Balls: AC26 / AC25 / AG24 / AH24 (abe_slimbus1_clock, abe_slimbus1_data, slimbus2_clock, slimbus2_data)
For more information on IO settings, see Control Module / Control Module Functional Description/ Functional Register Description / Signal Integrity Parameter Control Registers with Pad Group Assignment / 50-Ω Output Buffer I/Os with Combined Mode and Load Settings section of the OMAP4430 TRM.
- Corresponding voltage: 1.8 V.

(2) In this table the rise and fall times are calculated for 20% to 80% of VDDS. For more information on the corresponding OMAP4 VDDS power supply name, see Table 2-1, POWER [9] column with the ball name.

(3) To have an idea of the output OMAP4 ball load supported for this application, you can consider the following:

Output OMAP4 ball load = Far End load + 1.34 pF/cm typical x trace length (cm).

Table 6-102. ABE SlimBus1, SlimBus2 Timing Requirements[(4)(6)]

NO.	PARAMETER		OPP100		OPP50		UNIT
			MIN	MAX	MIN	MAX	
SB1	1 / $t_{c(clk)}$	Frequency[(1)] slimbusx_clock clock period		24.576		12.288	MHz
SB2	$t_{w(clkH)}$	Typical pulse duration, slimbusx_clock clock low	0.5*P[(2)]		0.5*P[(2)]		ns
SB3	$t_{w(clkL)}$	Typical pulse duration, slimbusx_clock clock high	0.5*P[(2)]		0.5*P[(2)]		ns
	$t_{dc(clk)}$	Duty cycle slimbusx_clock clock error		2000		2000	ps
	$t_{j(clk)}$	Cycle slimbusx_clock clock jitter[(3)]		283		283	ps
SB4	$t_{su(dV-clkH)}$	Setup time, slimbusx_data valid before slimbusx_clock falling edge	4.6		8.1		ns
SB5	$t_{h(clkH-dV)}$	Hold time, slimbusx_data valid after slimbusx_clock falling edge	1.3		3.3		ns

(1) Related to the input maximum frequency supported by the SlimBus module
(2) P = slimbusx_clock period in ns
(3) Maximum cycle jitter supported by slimbusx_clock input clock
(4) The timing requirements are assured for the cycle jitter and duty cycle error conditions specified.
(5) slimbusx represents abe_slimbus1 and slimbus2.
(6) See DM Operating Condition Addendum for CORE OPP voltages.

Table 6-103. ABE SlimBus1, SlimBus2 Switching Characteristics[(5)]

NO.	PARAMETER		OPP100		OPP50		UNIT
			MIN	MAX	MIN	MAX	
SB1	1 / $t_{c(clk)}$	Frequency[(1)] slimbusx _clock clock period		24.576		12.288	MHz
SB2	$t_{w(clkH)}$	Typical slimbusx _clock clock low	0.5*P[(2)]		0.5*P[(2)]		ns
SB3	$t_{w(clkL)}$	Typical slimbusx _clock clock high	0.5*P[(2)]		0.5*P[(2)]		ns
	$t_{dc(clk)}$	Duty cycle error, output slimbusx _clock clock		2000		2000	ps
	$t_{R(clk)}$	Rise time, output slimbusx _clock clock		5.488		5.488	ns
	$t_{F(clk)}$	Fall time, output slimbusx _clock clock		5.745		5.745	ns
SB6	$t_{d(clkL-doV)}$	Delay time, output slimbusx _clock clock high to output slimbusx _data valid	0.000	11.528	0.000	31.059	ns
	$t_{R(do)}$	Rising time, output slimbusx _data		5.488		5.488	ns
	$t_{F(do)}$	Falling time, output slimbusx _data		5.745		5.745	ns

(1) Related to the output maximum frequency supported by the SlimBus module
(2) P = output slimbusx _clock period in ns
(3) The jitter probability density can be approximated by a Gaussian function.
(4) slimbusx represents abe_slimbus1 and slimbus2.
(5) See DM Operating Condition Addendum for CORE OPP voltages.

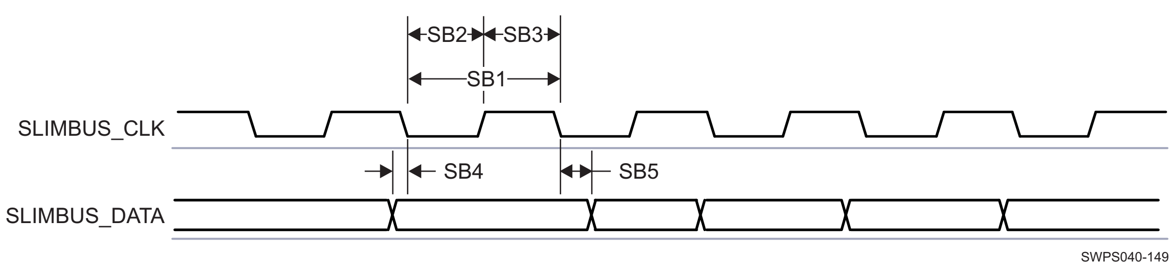

Figure 6-74. ABE SlimBus1, SlimBus2 Master Read Mode[(1)]

(1) slimbusx represents abe_slimbus1 and slimbus2.

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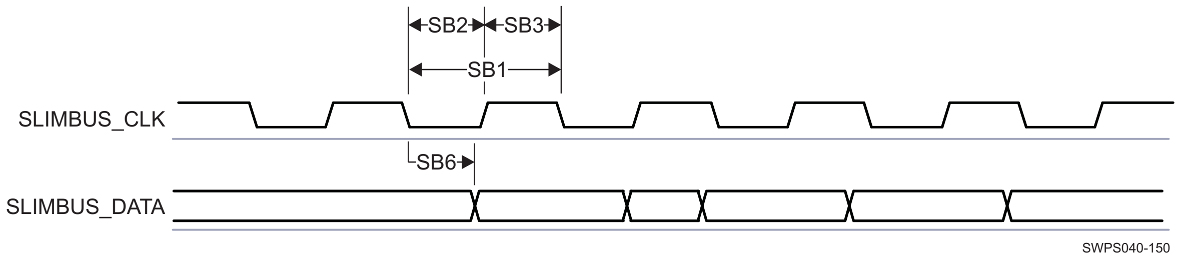

Figure 6-75. ABE SlimBus1, SlimBus2 Master Write Mode(1)(2)

(1) The polarity of signals is software configurable.
For more information, see the Serial Communication Interface / Serial Low-Power Inter-Chip Media Bus Controller section of the OMAP4430 TRM.

(2) slimbusx represents abe_slimbus1 and slimbus2.

6.6.6.2 ABE SlimBus1, SlimBus2—SLIMBUS SDR 19.2 MHz

Table 6-105 and Table 6-106 assume testing over the recommended operating conditions and electrical characteristic conditions below (see Figure 6-76 and Figure 6-77).

Table 6-104. ABE SlimBus1, SlimBus2 Timing Conditions(1)(2)(3)

SYSTEM CONDITION PARAMETER		VALUE		UNIT
		MIN	MAX	
Input Conditions				
t_R	Input signal rise time	1.20		ps
t_F	Input signal fall time	1.20		ps
PCB Conditions				
	Number of external peripherals		4	
	Far end load		20	pF
	Trace length		10	cm
	Characteristics impedance	30	60	Ω

(1) IO settings: MB[1:0] = 11 and LB0 = 1.
- Balls: AC26 / AC25 / AG24 / AH24 (abe_slimbus1_clock, abe_slimbus1_data, slimbus2_clock, slimbus2_data)
For more information on IO settings, see Control Module / Control Module Functional Description/ Functional Register Description / Signal Integrity Parameter Control Registers with Pad Group Assignment / 50-Ω Output Buffer I/Os with Combined Mode and Load Settings section of the OMAP4430 TRM.
- Corresponding voltage: 1.8 V.

(2) In this table the rise and fall times are calculated for 20% to 80% of VDDS. For more information on the corresponding OMAP4 VDDS power supply name, see Table 2-1, POWER [9] column with the ball name.

(3) To have an idea of the output OMAP4 ball load supported for this application, you can consider the following:
Output OMAP4 ball load = Far End load + 1.34 pF/cm typical x trace length (cm).

Table 6-105. ABE SlimBus1, SlimBus2 Timing Requirements(4)(6)

NO.	PARAMETER		OPP100		OPP50		UNIT
			MIN	MAX	MIN	MAX	
SB1	$1 / t_{c(clk)}$	Frequency(1) slimbusx_clock clock period		19.2		9.6	MHz
SB2	$t_{w(clkH)}$	Typical pulse duration, slimbusx_clock clock low	0.5*P(2)		0.5*P(2)		ns
SB3	$t_{w(clkL)}$	Typical pulse duration, slimbusx_clock clock high	0.5*P(2)		0.5*P(2)		ns
	$t_{dc(clk)}$	Duty cycle slimbusx_clock clock error		2000		2000	ps
	$t_{j(clk)}$	Cycle slimbusx_clock clock jitter(3)		283		283	ps
SB4	$t_{su(dV-clkH)}$	Setup time, slimbusx_data valid before slimbusx_clock falling edge	4.6		8.1		ns
SB5	$t_{h(clkH-dV)}$	Hold time, slimbusx_data valid after slimbusx_clock falling edge	0.2		2.2		ns

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(1) Related to the input maximum frequency supported by the SlimBus module
(2) P = slimbusx_clock period in ns
(3) Maximum cycle jitter supported by slimbusx_clock input clock
(4) The timing requirements are assured for the cycle jitter and duty cycle error conditions specified.
(5) slimbusx represents abe_slimbus1 and slimbus2.
(6) See DM Operating Condition Addendum for CORE OPP voltages.

Table 6-106. ABE SlimBus1, SlimBus2 Switching Characteristics(5)

NO.	PARAMETER		OPP100		OPP50		UNIT
			MIN	MAX	MIN	MAX	
SB1	$1 / t_{c(clk)}$	Frequency(1) slimbusx _clock clock period		19.2		9.6	MHz
SB2	$t_{w(clkH)}$	Typical slimbusx _clock clock low	0.5*P(2)		0.5*P(2)		ns
SB3	$t_{w(clkL)}$	Typical slimbusx _clock clock high	0.5*P(2)		0.5*P(2)		ns
	$t_{dc(clk)}$	Duty cycle error, output slimbusx _clock clock		2000		2000	ps
	$t_{R(clk)}$	Rise time, output slimbusx _clock clock		9.052		9.052	ns
	$t_{F(clk)}$	Fall time, output slimbusx _clock clock		10.332		10.332	ns
SB6	$t_{d(clkL-doV)}$	Delay time, output slimbusx _clock clock high to output slimbusx _data valid	0.000	12.964	0.000	39.005	ns
	$t_{R(do)}$	Rising time, output slimbusx _data		9.052		9.052	ns
	$t_{F(do)}$	Falling time, output slimbusx _data		10.332		10.332	ns

(1) Related to the output maximum frequency supported by the SlimBus module
(2) P = output slimbusx _clock period in ns
(3) The jitter probability density can be approximated by a Gaussian function.
(4) slimbusx represents abe_slimbus1 and slimbus2.
(5) See DM Operating Condition Addendum for CORE OPP voltages.

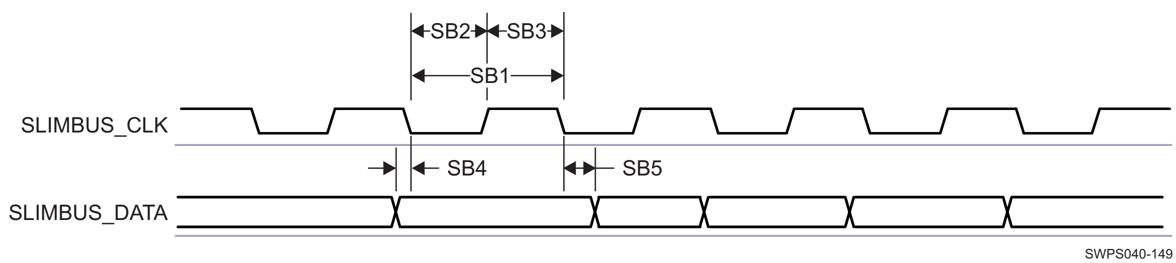

Figure 6-76. ABE SlimBus1, SlimBus2 Master Read Mode(1)

(1) slimbusx represents abe_slimbus1 and slimbus2.

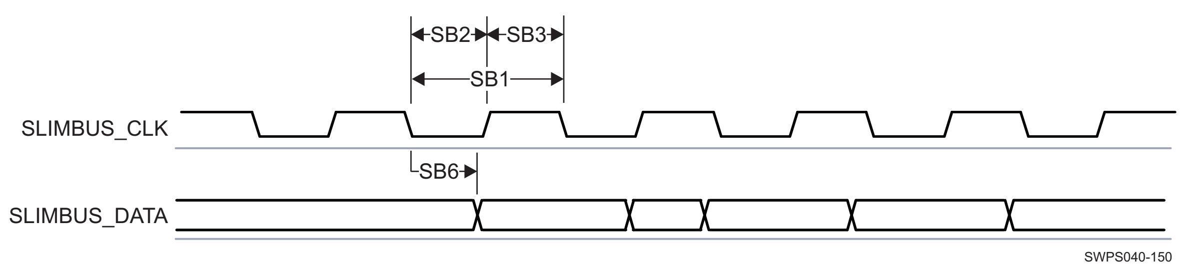

Figure 6-77. ABE SlimBus1, SlimBus2 Master Write Mode(1)(2)

(1) The polarity of signals is software configurable.
For more information, see the Serial Communication Interface / Serial Low-Power Inter-Chip Media Bus Controller section of the OMAP4430 TRM.
(2) slimbusx represents abe_slimbus1 and slimbus2.

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6.6.7 High-Speed Synchronous Interface (HSI)

The MIPI high-speed synchronous serial interface (HSI) module is a multichannel and full duplex serial communications interface, composed of the HSI Transmitter (HSIT) in charge of the transmitted information and the HSI Receiver (HSIR) in charge of the received information. The HSI peripheral is used typically to enable OMAP to exchange information with an external modem. On the modem side, there is also a receiver and a transmitter.

6.6.7.1 High-Speed Synchronous Interface 1

6.6.7.1.1 HSI1 Transmit and Receive Modes—1.2 V

Table 6-108 and Table 6-109 assume testing over the recommended operating conditions and electrical characteristic conditions below (see Figure 6-78 and Figure 6-79).

Table 6-107. HSI1 Timing Conditions—Transmit and Receive Modes—1.2 V(1)(2)(4)

SYSTEM CONDITION PARAMETER		VALUE		UNIT
		MIN	MAX	
Input Conditions				
t_R	Input signal rise time	1000	1300	ps
t_F	Input signal fall time	1000	1200	ps
PCB Conditions(3)				
	Number of external peripherals		1	
	Far end load		5	pF
	Trace length		4	cm
	Characteristics impedance	35	55	Ω

(1) IO settings: MB[1:0] = 11 and LB0 = 1, mode 3.
For more information, see Control Module / Control Module Functional Description/ Functional Register Description / Signal Integrity Parameter Control Registers with Pad Group Assignment / I/Os with Combined Mode and Load Settings section of the OMAP4430 TRM.

(2) In this table the rise and fall times are calculated for 20% to 80% of VDDS. For more information on the corresponding OMAP4 VDDS power supply name, see Table 2-1, POWER [9] column with the ball name.

(3) Minimize the number of vias by layer transitions.

(4) To have an idea of the output OMAP4 ball load supported for this application, you can consider the following:
Output OMAP4 ball load = Far End load + 1.34 pF/cm typical x trace length (cm).
Output load C_{LOAD} or Far end load equals to the total capacitance seen at the Far end of the transmission line.

Table 6-108. HSI1 Timing Requirements—Receive Mode—1.2 V(1)

NO.	PARAMETER		OPP100		OPP50		UNIT
			MIN	MAX	MIN	MAX	
	$1 / t_{c(data,flag)}$	Frequency, hsi_cadata, hsi_caflag		112		56	MHz
HSI1	$1 / t_{c(NomBit)}$	Frequency, nominal bit time	225		112		MHz
HSI2	$t_{d(DAT-FLAG)}$	Delay time, hsi_cadata transition to hsi_caflag transition	1.56		3.13		ns
	$t_{d(FLAG-DAT)}$	Delay time, hsi_caflag transition to hsi_cadata transition	1.56		3.13		ns
HSI3	$t_{d(DAT)}$	Duration time, hsi_cadata low level or high level duration	2.56		5.13		ns
	$t_{d(FLAG)}$	Duration time, hsi_caflag low level or high level duration	2.56		5.13		ns
HSI4	t_R	Rise time, hsi_cadata and hsi_caflag	1.0	1.30	1.0	1.30	ns
HSI5	t_F	Fall time, hsi_cadata and hsi_caflag	1.0	1.20	1.0	1.20	ns

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(1) See DM Operating Condition Addendum for CORE OPP voltages.

Table 6-109. HSI1 Switching Characteristics—Transmit Mode—1.2 V(1)(2)(3)

NO.	PARAMETER		OPP100		OPP50		UNIT
			MIN	MAX	MIN	MAX	
	$1 / t_{c(data,flag)}$	Frequency, hsi_acdata, hsi_acflag		96		48	MHz
HSI1	$1 / t_{c(NomBit)}$	Frequency, nominal bit time	192		96		MHz
HSI6	$t_{d(DAT-FLAG)}$	Delay time, hsi_acdata transition to his_acflag transition	2.08	P + 0.98	4.17	P + 2.21	ns
	$t_{d(FLAG-DAT)}$	Delay time, hsi_acflag transition to hsi_acdata transition	2.08	P + 0.98	4.17	P + 2.21	ns
HSI7	$t_{d(DAT)}$	Duration time, hsi_acdata low level or high level duration	2.32	P + 1.18	4.42	P + 2.41	ns
	$t_{d(FLAG)}$	Duration time, hsi_acflag low level or high level duration	2.32	P + 1.18	4.42	P + 2.41	ns
HSI8	t_R	Rise time, hsi_acdata and hsi_acflag	0.20	1.60	0.40	1.60	ns
HSI9	t_F	Fall time, hsi_acdata and hsi_acflag	0.20	1.40	0.30	1.40	ns

(1) Considered capacitive load is equal to 5 pF.

(2) P = $t_{c(NomBit)}$ time in ns

(3) See DM Operating Condition Addendum for CORE OPP voltages.

6.6.7.1.2 HSI1 Transmit and Receive Modes—1.8 V

Table 6-111 and Table 6-112 assume testing over the recommended operating conditions and electrical characteristic conditions below (see Figure 6-78 and Figure 6-79).

Table 6-110. HSI1 Timing Conditions—Transmit and Receive Modes—1.8 V(1)(2)(4)

SYSTEM CONDITION PARAMETER		VALUE		UNIT
		MIN	MAX	
Input Conditions				
t_R	Input signal rise time	1000	1500	ps
t_F	Input signal fall time	1000	1300	ps
PCB Conditions(3)				
	Number of external peripherals		1	
	Far end load		5	pF
	Trace length		4	cm
	Characteristics impedance	35	55	Ω

(1) IO settings: MB[1:0] = 11 and LB0 = 0, mode 3.
For more information, see Control Module / Control Module Functional Description/ Functional Register Description / Signal Integrity Parameter Control Registers with Pad Group Assignment / I/Os with Combined Mode and Load Settings section of the OMAP4430 TRM.

(2) In this table the rise and fall times are calculated for 20% to 80% of VDDS. For more information on the corresponding OMAP4 VDDS power supply name, see Table 2-1, POWER [9] column with the ball name.

(3) Minimize the number of vias by layer transitions.

(4) To have an idea of the output OMAP4 ball load supported for this application, you can consider the following:
Output OMAP4 ball load = Far End load + 1.34 pF/cm typical x trace length (cm).
Output load C_{LOAD} or Far end load equals to the total capacitance seen at the Far end of the transmission line.

Table 6-111. HSI1 Timing Requirements—Receive Mode—1.8 V(1)

NO.	PARAMETER		OPP100		OPP50		UNIT
			MIN	MAX	MIN	MAX	
	$1 / t_{c(data,flag)}$	Frequency, hsi_cadata, hsi_caflag		112		56	MHz
HSI1	$1 / t_{c(NomBit)}$	Frequency, nominal bit time	225		112		MHz

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Table 6-111. HSI1 Timing Requirements—Receive Mode—1.8 V(1) (continued)

NO.	PARAMETER		OPP100		OPP50		UNIT
			MIN	MAX	MIN	MAX	
HSI2	$t_{d(DAT\text{-}FLAG)}$	Delay time, hsi_cadata transition to hsi_caflag transition	1.56		3.13		ns
	$t_{d(FLAG\text{-}DAT)}$	Delay time, hsi_caflag transition to hsi_cadata transition	1.56		3.13		ns
HSI3	$t_{d(DAT)}$	Duration time, hsi_cadata low level or high level duration	2.56		5.13		ns
	$t_{d(FLAG)}$	Duration time, hsi_caflag low level or high level duration	2.56		5.13		ns
HSI4	t_R	Rise time, hsi_cadata and hsi_caflag	1.0	1.5	1.0	1.5	ns
HSI5	t_F	Fall time, hsi_cadata and hsi_caflag	1.0	1.3	1.0	1.3	ns

(1) See DM Operating Condition Addendum for CORE OPP voltages.

Table 6-112. HSI1 Switching Characteristics—Transmit Mode—1.8 V(1)(2)(3)

NO.	PARAMETER		OPP100		OPP50		UNIT
			MIN	MAX	MIN	MAX	
	$1 / t_{c(data,flag)}$	Frequency, hsi_acdata, hsi_acflag		96		48	MHz
HSI1	$1 / t_{c(NomBit)}$	Frequency, nominal bit time	192		96		MHz
HSI6	$t_{d(DAT\text{-}FLAG)}$	Delay time, hsi_acdata transition to his_acflag transition	2.08	P + 0.78	4.17	P + 1.91	ns
	$t_{d(FLAG\text{-}DAT)}$	Delay time, hsi_acflag transition to hsi_acdata transition	2.08	P + 0.78	4.17	P + 1.91	ns
HSI7	$t_{d(DAT)}$	Duration time, hsi_acdata low level or high level duration	2.57	P + 1.18	4.69	P + 2.41	ns
	$t_{d(FLAG)}$	Duration time, hsi_acflag low level or high level duration	2.57	P + 1.18	4.69	P + 2.41	ns
HSI8	t_R	Rise time, hsi_acdata and hsi_acflag	0.40	1.70	0.60	1.70	ns
HSI9	t_F	Fall time, hsi_acdata and hsi_acflag	0.50	1.50	0.60	1.50	ns

(1) Considered capacitive load is equal to 5 pF.

(2) P = $t_{c(NomBit)}$ time in ns

(3) See DM Operating Condition Addendum for CORE OPP voltages.

6.6.7.2 High-Speed Synchronous Interface 2

6.6.7.2.1 HSI2 Transmit and Receive Modes—1.2 V

Table 6-114 and Table 6-115 assume testing over the recommended operating conditions and electrical characteristic conditions below (see Figure 6-78 and Figure 6-79).

Table 6-113. HSI2 Timing Conditions—Transmit and Receive Modes—1.2 V(1)(2)(4)

SYSTEM CONDITION PARAMETER		VALUE		UNIT
		MIN	MAX	
Input Conditions				
t_R	Input signal rise time	1000	1100	ps
t_F	Input signal fall time	1000	1100	ps
PCB Conditions(3)				
	Number of external peripherals		1	
	Far end load		5	pF
	Trace length		4	cm
	Characteristics impedance	35	50	Ω

(1) IO settings: DS0 = 1.
For more information, see Control Module / Control Module Functional Description/ Functional Register Description / Signal Integrity Parameter Control Registers with Pad Group Assignment / I/O cells with Configurable Output Driver Impedance section of the OMAP4430 TRM.

(2) In this table the rise and fall times are calculated for 20% to 80% of VDDS. For more information on the corresponding OMAP4 VDDS power supply name, see Table 2-1, POWER [9] column with the ball name.

(3) Minimize the number of vias by layer transitions.

(4) To have an idea of the output OMAP4 ball load supported for this application, you can consider the following:
Output OMAP4 ball load = Far End load + 1.34 pF/cm typical x trace length (cm).
Output load C_{LOAD} or Far end load equals to the total capacitance seen at the Far end of the transmission line.

Table 6-114. HSI2 Timing Requirements—Receive Mode—1.2 V(1)

NO.	PARAMETER		OPP100		OPP50		UNIT
			MIN	MAX	MIN	MAX	
	$1 / t_{c(data,flag)}$	Frequency, hsi_cadata, hsi_caflag		112		56	MHz
HSI1	$1 / t_{c(NomBit)}$	Frequency, nominal bit time	225		112		MHz
HSI2	$t_{d(DAT-FLAG)}$	Delay time, hsi_cadata transition to hsi_caflag transition	1.56		3.13		ns
	$t_{d(FLAG-DAT)}$	Delay time, hsi_caflag transition to hsi_cadata transition	1.56		3.13		ns
HSI3	$t_{d(DAT)}$	Duration time, hsi_cadata low level or high level duration	2.56		5.13		ns
	$t_{d(FLAG)}$	Duration time, hsi_caflag low level or high level duration	2.56		5.13		ns
HSI4	t_R	Rise time, hsi_cadata and hsi_caflag	1	1.10	1	1.10	ns
HSI5	t_F	Fall time, hsi_cadata and hsi_caflag	1	1.10	1	1.10	ns

(1) See DM Operating Condition Addendum for CORE OPP voltages.

Table 6-115. HSI2 Switching Characteristics—Transmit Mode—1.2 V(1)(2)(3)

NO.	PARAMETER		OPP100		OPP50		UNIT
			MIN	MAX	MIN	MAX	
	$1 / t_{c(data,flag)}$	Frequency, hsi_acdata, hsi_acflag		96		48	MHz
HSI1	$1 / t_{c(NomBit)}$	Frequency, nominal bit time	192		96		MHz
HSI6	$t_{d(DAT-FLAG)}$	Delay time, hsi_acdata transition to his_acflag transition	2.08	P + 0.98	4.17	P + 2.21	ns
	$t_{d(FLAG-DAT)}$	Delay time, hsi_acflag transition to hsi_acdata transition	2.08	P + 0.98	4.17	P + 2.21	ns
HSI7	$t_{d(DAT)}$	Duration time, hsi_acdata low level or high level duration	2.31	P + 1.18	4.39	P + 2.41	ns
	$t_{d(FLAG)}$	Duration time, hsi_acflag low level or high level duration	2.31	P + 1.18	4.39	P + 2.41	ns
HSI8	t_R	Rise time, hsi_acdata and hsi_acflag	0.20	1.50	0.30	1.50	ns
HSI9	t_F	Fall time, hsi_acdata and hsi_acflag	0.20	1.40	0.30	1.40	ns

(1) Considered capacitive load is equal to 5 pF.
(2) P = $t_{c(NomBit)}$ time in ns
(3) See DM Operating Condition Addendum for CORE OPP voltages.

6.6.7.2.2 HSI2 Transmit and Receive Modes—1.8 V

Table 6-117 and Table 6-118 assume testing over the recommended operating conditions and electrical characteristic conditions below (see Figure 6-78 and Figure 6-79).

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Table 6-116. HSI2 Timing Conditions—Transmit and Receive Modes—1.8 V(1)(2)(4)

SYSTEM CONDITION PARAMETER		VALUE		UNIT
		MIN	MAX	
Input Conditions				
t_R	Input signal rise time	1000	1300	ps
t_F	Input signal fall time	1000	1200	ps
PCB Conditions(3)				
	Number of external peripherals		1	
	Far end load		5	pF
	Trace length		4	cm
	Characteristics impedance	35	50	Ω

(1) IO settings: DS0 = 1.
For more information, see Control Module / Control Module Functional Description/ Functional Register Description / Signal Integrity Parameter Control Registers with Pad Group Assignment / I/O cells with Configurable Output Driver Impedance section of the OMAP4430 TRM.

(2) In this table the rise and fall times are calculated for 20% to 80% of VDDS. For more information on the corresponding OMAP4 VDDS power supply name, see Table 2-1, POWER [9] column with the ball name.

(3) Minimize the number of vias by layer transitions.
The use of 15-Ω external serial resistance is recommended for transmit mode on hsi2_acdata (HSI2 APE to cellular modem data signal) and hsi2_acflag (HSI2 APE to cellular modem flag signal).
In case the application needs both transmit and receive modes, the serial resistance is also recommended for receive mode on hsi2_cadata (HSI2 cellular modem to APE data signal) and hsi2_caflag (HSI2 cellular modem to APE flag signal).

(4) To have an idea of the output OMAP4 ball load supported for this application, you can consider the following:
Output OMAP4 ball load = Far End load + 1.34 pF/cm typical x trace length (cm).
Output load C_{LOAD} or Far end load equals to the total capacitance seen at the Far end of the transmission line.

Table 6-117. HSI2 Timing Requirements—Receive Mode—1.8 V(1)

NO.	PARAMETER		OPP100		OPP50		UNIT
			MIN	MAX	MIN	MAX	
	$1 / t_{c(data,flag)}$	Frequency, hsi_cadata, hsi_caflag		112		56	MHz
HSI1	$1 / t_{c(NomBit)}$	Frequency, nominal bit time	225		112		MHz
HSI2	$t_{d(DAT-FLAG)}$	Delay time, hsi_cadata transition to hsi_caflag transition	1.56		3.13		ns
	$t_{d(FLAG-DAT)}$	Delay time, hsi_caflag transition to hsi_cadata transition	1.56		3.13		ns
HSI3	$t_{d(DAT)}$	Duration time, hsi_cadata low level or high level duration	2.56		5.13		ns
	$t_{d(FLAG)}$	Duration time, hsi_caflag low level or high level duration	2.56		5.13		ns
HSI4	t_R	Rise time, hsi_cadata and hsi_caflag	1.0	1.30	1.0	1.30	ns
HSI5	t_F	Fall time, hsi_cadata and hsi_caflag	1.0	1.20	1.0	1.20	ns

(1) See DM Operating Condition Addendum for CORE OPP voltages.

Table 6-118. HSI2 Switching Characteristics—Transmit Mode—1.8 V(1)(2)(3)

NO.	PARAMETER		OPP100		OPP50		UNIT
			MIN	MAX	MIN	MAX	
	$1 / t_{c(data,flag)}$	Frequency, hsi_acdata, hsi_acflag		96		48	MHz
HSI1	$1 / t_{c(NomBit)}$	Frequency, nominal bit time	192		96		MHz
HSI6	$t_{d(DAT-FLAG)}$	Delay time, hsi_acdata transition to his_acflag transition	2.08	P + 0.98	4.17	P + 2.21	ns
	$t_{d(FLAG-DAT)}$	Delay time, hsi_acflag transition to hsi_acdata transition	2.08	P + 0.98	4.17	P + 2.21	ns
HSI7	$t_{d(DAT)}$	Duration time, hsi_acdata low level or high level duration	2.35	P + 1.18	4.43	P + 2.41	ns
	$t_{d(FLAG)}$	Duration time, hsi_acflag low level or high level duration	2.35	P + 1.18	4.43	P + 2.41	ns
HSI8	t_R	Rise time, hsi_acdata and hsi_acflag	0.20	1.60	0.30	1.60	ns
HSI9	t_F	Fall time, hsi_acdata and hsi_acflag	0.20	1.40	0.30	1.40	ns

(1) Considered capacitive load is equal to 5 pF.

(2) P = $t_{c(NomBit)}$ time in ns

(3) See DM Operating Condition Addendum for CORE OPP voltages.

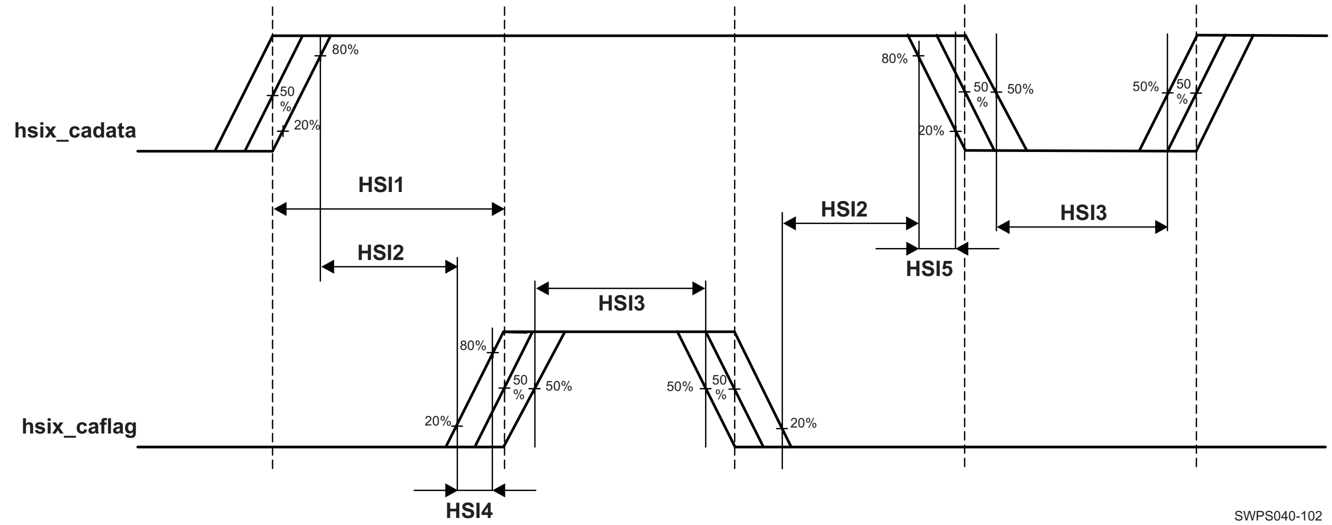

Figure 6-78. HSI1, 2 Interfaces—1.2 V and 1.8 V—Receive Mode(1)(2)

(1) In hsix, x is equal to 1 or 2.

(2) The hsix_cadata signal always reflects the value being transmitted and the hsix_caflag signal only toggles when the bit value transmitted remains constant. Transmission of one bit is indicated by a transition on exactly one, and only one, of the two signals.

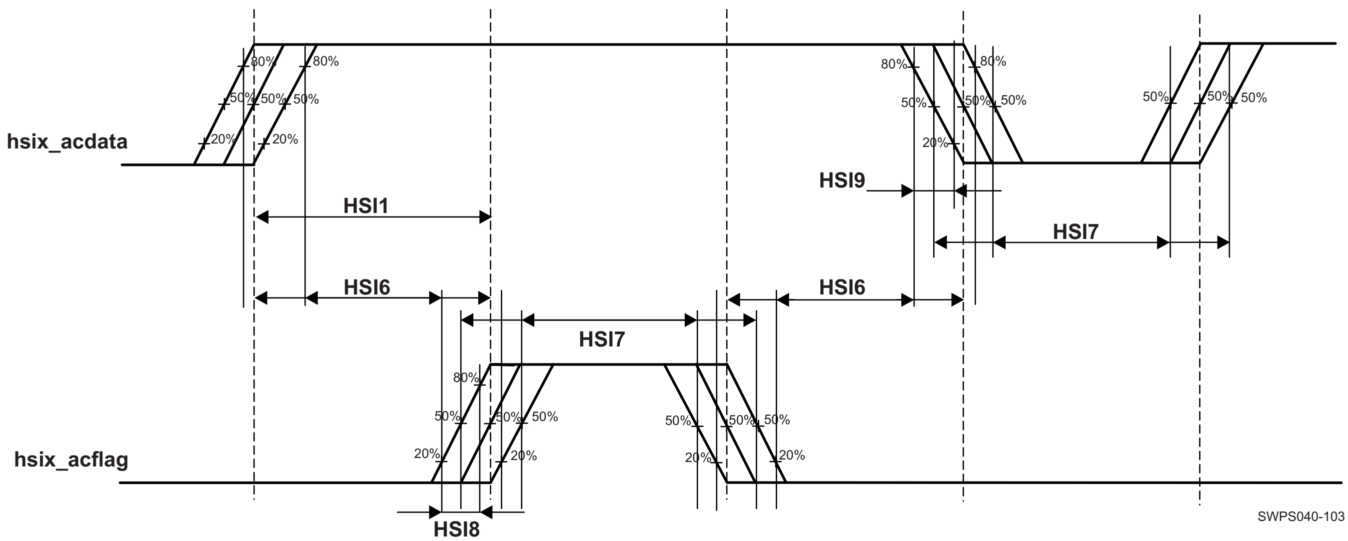

Figure 6-79. HSI1, 2 Interfaces—1.2 V and 1.8 V—Transmit Mode(1)(2)

(1) In hsix, x is equal to 1 or 2.

(2) The hsix_acdata signal always reflects the value being transmitted and the hsix_acflag signal only toggles when the bit value transmitted remains constant. Transmission of one bit is indicated by a transition on exactly one, and only one, of the two signals.

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6.6.8 Universal Serial Bus (USB)

6.6.8.1 Universal Serial Bus (USB)—USBA0

NOTE

For more information, see the Serial Communication Interface / High-Speed USB OTG Controller section of the OMAP4430 TRM.

6.6.8.1.1 High-Speed USBA0 (HSUSB)—USB HS OTG PHY

The USB HS OTG PHY module fits the High-speed Signaling Eye Patterns and Rise and Fall Time of the USB specification Revision 2.0, provided the PCB guidelines are followed (for more information on the PCB guidelines, see Section A, *OMAP4430 Processor Multimedia Device PCB Guideline*). For more information on the High-speed Signaling Eye Patterns and Rise and Fall Time, see the Electrical / Signaling / Data Signal Rise and Fall, Eye Patterns / High-speed Signaling Eye Patterns and Rise and Fall Time section of the USB specification Revision 2.0:

- For USB HS transmit waveform requirements, see Figure 7-13 (Template 1).
- For USB HS receiver sensitivity waveform requirements, see Figure 7-16 (Template 4).

6.6.8.1.2 High-Speed USBA0 (HSUSB)—ULPI SDR—Slave Mode

Table 6-120 and Table 6-121 assume testing over the recommended operating conditions and electrical characteristic conditions below (see Figure 6-80).

Table 6-119. High-Speed USB USBA0 Timing Conditions—ULPI SDR—Slave Mode—1.8 V(1)(2)(3)

SYSTEM CONDITION PARAMETER		VALUE		UNIT
		MIN	MAX	
Input Conditions				
t_R	Input signal rise time	1.00	3.00	ns
t_F	Input signal fall time	1.00	3.00	ns
PCB Conditions				
	Number of external peripherals		1	
	Far end load		5	pF
	Trace length		5	cm
	Characteristics impedance	30	60	Ω

(1) IO settings configuration: DS0 = 0
Corresponding voltage: 1.8 V
For more information, see Control Module / Control Module Functional Description/ Functional Register Description / Signal Integrity Parameter Control Registers with Pad Group Assignment / I/O cells with Configurable Output Driver Impedance section of the OMAP4430 TRM.

(2) In this table the rise and fall times are calculated for 20% to 80% of VDDS. For more information on the corresponding OMAP4 VDDS power supply name, see Table 2-1, POWER [9] column with the ball name.

(3) To have an idea of the output OMAP4 ball load supported for this application, you can consider the following:
Output OMAP4 ball load = Far End load + 1.34 pF/cm typical x trace length (cm).

Table 6-120. High-Speed USB USBA0 Timing Requirements—ULPI SDR—Slave Mode—1.8 V(4)

NO.	PARAMETER		OPP100		UNIT
			MIN	MAX	
US1	$1 / t_{c(clk)}$	Frequency(1), usba0_ulpiphy_clk		60	MHz
US2	$t_{w(clkH)}$	Typical pulse duration, usba0_ulpiphy_clk high	0.5*P(2)		ns
US3	$t_{w(clkL)}$	Typical pulse duration, usba0_ulpiphy_clk low	0.5*P(2)		ns
	$t_{dc(clk)}$	Duty cycle error, usba0_ulpiphy_clk	–833	833	ps
	$t_{j(clk)}$	Jitter standard deviation(3), usba0_ulpiphy_clk		500	ps

Table 6-120. High-Speed USB USBA0 Timing Requirements—ULPI SDR—Slave Mode—1.8 V[(4)] (continued)

NO.	PARAMETER		OPP100		UNIT
			MIN	MAX	
US5	$t_{su(ctrlV-clkH)}$	Setup time, usba0_ulpiphy_dir and usba0_ulpiphy_nxt valid before usba0_ulpiphy_clk rising edge	6.73		ns
US6	$t_{h(clkH-ctrlV)}$	Hold time, usba0_ulpiphy_dir and usba0_ulpiphy_nxt valid after usba0_ulpiphy_clk rising edge	0.00		ns
US7	$t_{su(dV-clkH)}$	Setup time, input usba0_ulpiphy_dat[7:0] valid before usba0_ulpiphy_clk rising edge	6.73		ns
US8	$t_{h(clkH-dV)}$	Hold time, input usba0_ulpiphy_dat[7:0] valid after usba0_ulpiphy_clk rising edge	0.00		ns

(1) Related to the input maximum frequency supported by the USB module.
(2) P = clk period in ns
(3) Maximum cycle jitter supported by clock input clock.
(4) See DM Operating Condition Addendum for CORE OPP voltages.

Table 6-121. High-Speed HSUSB USBA0 Switching Characteristics—ULPI SDR—Slave Mode—1.8 V[(1)]

NO.	PARAMETER		OPP100		UNIT
			MIN	MAX	
US4	$t_{d(clkL-ctrlV)}$	Delay time, usba0_ulpiphy_clk rising edge high to output usba0_ulpiphy_stp valid	0.40	8.34	ns
	$t_{R(ctrl)}$	Rise time, output usba0_ulpiphy_stp		3.0	ps
	$t_{F(dtrl)}$	Fall time, output usba0_ulpiphy_stp		3.0	ps
US9	$t_{d(clkL-doV)}$	Delay time, usba0_ulpiphy_clk rising edge to output usba0_ulpiphy_dat[7:0] valid	0.40	8.34	ns
	$t_{R(do)}$	Rise time, output usba0_ulpiphy_dat[7:0]		3.0	ps
	$t_{F(do)}$	Fall time, output usba0_ulpiphy_dat[7:0]		3.0	ps

(1) See DM Operating Condition Addendum for CORE OPP voltages.

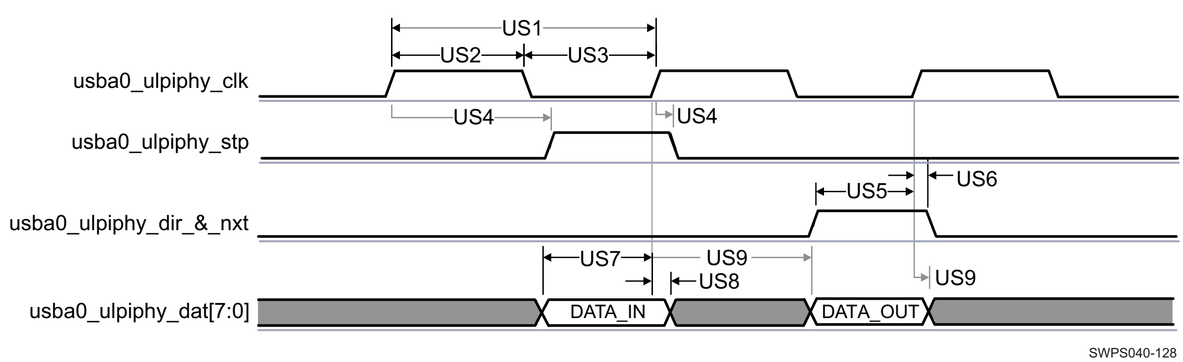

Figure 6-80. High-Speed USB USBA0—ULPI SDR—Slave Mode—1.8 V

6.6.8.2 Universal Serial Bus (USB)—USBC1

NOTE

For more information, see the Serial Communication Interface / Full-Speed USB Host Controller section of the OMAP4430 TRM.

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6.6.8.2.1 Low- / Full-Speed USBC1 (FSUSB)—Bidirectional Standard 4-pin Mode

Table 6-123 and Table 6-124 assume testing over the recommended operating conditions and electrical characteristic conditions below (see Figure 6-81).

Table 6-122. Low- / Full-Speed USBC1 Timing Conditions—Bidirectional Standard 4-pin Mode—1.8 V(1)(2)(3)

TIMING CONDITION PARAMETER		VALUE		UNIT
		MIN	MAX	
Input Conditions				
t_R	Input signal rise time	2		ns
t_F	Input signal fall time	2		ns
PCB Conditions				
	Number of external peripherals		1	
	Far end load		10	pF
	Trace length		10	cm
	Characteristics impedance	30	60	Ω

(1) IO settings:
- usbc1_icusb_txen (ball D23): LB0 = 0
  For more information, see the Control Module / Control Module Functional Description/ Functional Register Description / Signal Integrity Parameter Control Registers with Pad Group Assignment section of the OMAP4430 TRM.
- usbc1_icusb_dp, usbc1_icusb_dm, usbc1_icusb_txen, usbc1_icusb_rcv (balls AE5, AF5, AF4, AE4): MB[1:0] = 10, LB0 = 1
  For more information, see Control Module / Control Module Functional Description/ Functional Register Description / Signal Integrity Parameter Control Registers with Pad Group Assignment / 50-Ω Output Buffer I/Os with Combined Mode and Load Settings section of the OMAP4430 TRM.
- Corresponding voltage: 1.8 V

(2) In this table the rise and fall times are calculated for 10% to 90% of VDDS. For more information on the corresponding OMAP4 VDDS power supply name, see Table 2-1, POWER [9] column with the ball name.

(3) To have an idea of the output OMAP4 ball load supported for this application, you can consider the following:
Output OMAP4 ball load = Far End load + 1.34 pF/cm typical x trace length (cm).

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Table 6-123. Low- / Full-Speed USBC1 Timing Requirements—Bidirectional Standard 4-pin Mode—1.8 V(1)(2)

NO.	PARAMETER		OPP100		OPP50		UNIT
			MIN	MAX	MIN	MAX	
FSU10	$t_{d(DAT,SE0)}$	Time duration, usbc1_icusb_dp (TXDAT, ball AE5) and usbc1_icusb_dm (TSE0, ball AF5) low together during transition		14.0		14.0	ns
FSU11	$t_{d(DAT,SE0)}$	Time duration, usbc1_icusb_dp (TXDAT, ball AE5) and usbc1_icusb_dm (TSE0, ball AF5) high together during transition		8.0		8.0	ns
FSU12	$t_{d(RCVU0)}$	Time duration, usbc1_icusb_rcv undefined during a Single End 0 (usbc1_icusb_dp (TXDAT, ball AE5) and usbc1_icusb_dm (TSE0, ball AF5) low together)		14.0		14.0	ns
FSU13	$t_{d(RCVU1)}$	Time duration, usbc1_icusb_rcv undefined during a Single End 1 (usbc1_icusb_dp (TXDAT, ball AE5) and usbc1_icusb_dm (TSE0, ball AF5) high together)		8.0		8.0	ns

(1) See DM Operating Condition Addendum for CORE OPP voltages.

(2) Low-Speed mode is a subset of the Full-Speed mode and it is expected to work at low bandwidth (1.5Mb/s).

Table 6-124. Low- / Full-Speed USBC1 Switching Characteristics—Bidirectional Standard 4-pin Mode—1.8 V(1)(2)

NO.	PARAMETER		OPP100		OPP50		UNIT
			MIN	MAX	MIN	MAX	
FSU14	$t_{d(TXENL-DATV)}$	Delay time usbc1_icusb_txen low to usbc1_icusb_dp (TXDAT, ball AE5) valid	81.8	84.8	81.8	84.8	ns
FSU15	$t_{d(TXENL-SE0V)}$	Delay time usbc1_icusb_txen low to usbc1_icusb_dm (TSE0, ball AF5) valid	81.8	84.8	81.8	84.8	ns
FSU16	$t_{sk(DAT-SE0)}$	Skew between usbc1_icusb_dp (TXDAT, ball AE5) and usbc1_icusb_dm (TSE0, ball AF5) transition		1.5		1.5	ns
FSU17	$t_{d(DATV-TXENH)}$	Delay time, usbc1_icusb_dp (TXDAT, ball AE5) invalid before usbc1_icusb_txen high	81.8		81.8		ns
FSU18	$t_{d(SE0V-TXENH)}$	Delay time, usbc1_icusb_dm (TSE0, ball AF5) invalid before usbc1_icusb_txen high	81.8		81.8		ns

(1) See DM Operating Condition Addendum for CORE OPP voltages.

(2) Low-Speed mode is a subset of the Full-Speed mode and it is expected to work at low bandwidth (1.5Mb/s).

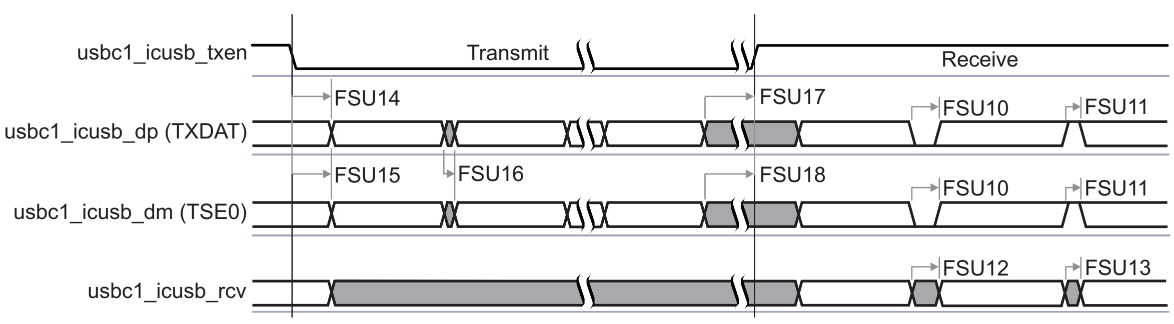

Figure 6-81. Low- / Full-Speed USBC1—Bidirectional Standard 4-pin Mode—1.8 V(1)

(1) To have usbc1_icusb_dm as TXDAT signal, use ball AF5.
To have usbc1_icusb_dp as TXSE0 signal, use ball AE5.

6.6.8.2.2 Low- / Full-Speed USBC1 (FSUSB)—Bidirectional Standard 4-pin TLL Mode

Table 6-126 and Table 6-127 assume testing over the recommended operating conditions and electrical characteristic conditions below (see Figure 6-82).

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Table 6-125. Low- / Full-Speed USBC1 Timing Conditions—Bidirectional Standard 4-pin TLL Mode—1.8 V(1)(2)(3)

TIMING CONDITION PARAMETER		VALUE		UNIT
		MIN	MAX	
Input Conditions				
t_R	Input signal rise time	2		ns
t_F	Input signal fall time	2		ns
PCB Conditions				
	Number of external peripherals		1	
	Far end load		10	pF
	Trace length		10	cm
	Characteristics impedance	30	60	Ω

(1) IO settings:
- usbc1_icusb_txen (ball D23): LB0 = 0
  For more information, see the Control Module / Control Module Functional Description/ Functional Register Description / Signal Integrity Parameter Control Registers with Pad Group Assignment section of the OMAP4430 TRM.
- usbc1_icusb_dp, usbc1_icusb_dm, usbc1_icusb_txen, usbc1_icusb_rcv (balls AE5, AF5, AF4, AE4): MB[1:0] = 10, LB0 = 1
  For more information, see Control Module / Control Module Functional Description/ Functional Register Description / Signal Integrity Parameter Control Registers with Pad Group Assignment / 50-Ω Output Buffer I/Os with Combined Mode and Load Settings section of the OMAP4430 TRM.
- Corresponding voltage: 1.8 V

(2) In this table the rise and fall times are calculated for 10% to 90% of VDDS. For more information on the corresponding OMAP4 VDDS power supply name, see Table 2-1, POWER [9] column with the ball name.

(3) To have an idea of the output OMAP4 ball load supported for this application, you can consider the following:
Output OMAP4 ball load = Far End load + 1.34 pF/cm typical x trace length (cm).

Table 6-126. Low- / Full-Speed USBC1 Timing Requirements—Bidirectional Standard 4-pin TLL Mode—1.8 V(1)(2)

NO.	PARAMETER		OPP100		OPP50		UNIT
			MIN	MAX	MIN	MAX	
FSUT9	$t_{d(DAT,SE0)}$	Time duration, usbc1_icusb_dp (TXDAT, ball AE5) and usbc1_icusb_dm (TSE0, ball AF5) low together during transition		14.0		14.0	ns
FSUT10	$t_{d(DAT,SE0)}$	Time duration, usbc1_icusb_dp (TXDAT, ball AE5) and usbc1_icusb_dm (TSE0, ball AF5) high together during transition		8.0		8.0	ns

(1) See DM Operating Condition Addendum for CORE OPP voltages.

(2) Low-Speed mode is a subset of the Full-Speed mode and it is expected to work at low bandwidth (1.5Mb/s).

Table 6-127. Low- / Full-Speed USBC1 Switching Characteristics—Bidirectional Standard 4-pin TLL Mode—1.8 V(1)(2)

NO.	PARAMETER		OPP100		OPP50		UNIT
			MIN	MAX	MIN	MAX	
FSUT11	$t_{d(TXENL-DATV)}$	Delay time usbc1_icusb_txen active to usbc1_icusb_dp (TXDAT, ball AE5) valid	81.8	84.8	81.8	84.8	ns
FSUT12	$t_{d(TXENL-SE0V)}$	Delay time usbc1_icusb_txen active to usbc1_icusb_dm (TSE0, ball AF5) valid	81.8	84.8	81.8	84.8	ns
FSUT13	$t_{sk(DAT-SE0)}$	Skew between usbc1_icusb_dp (TXDAT, ball AE5) and usbc1_icusb_dm (TSE0, ball AF5) transition		1.5		1.5	ns
FSUT14	$t_{sk(DP,DM-RCV)}$	Skew between usbc1_icusb_dp (TXDAT, ball AE5), usbc1_icusb_dm (TSE0, ball AF5) and usbc1_icusb_rcv transition		1.5		1.5	ns
FSUT15	$t_{d(DATI-TXENL)}$	Delay time usbc1_icusb_dm (TSE0, ball AF5) invalid to usbc1_icusb_txen Low	81.8		81.8		ns

Table 6-127. Low- / Full-Speed USBC1 Switching Characteristics—Bidirectional Standard 4-pin TLL Mode—1.8 V(1)(2) (continued)

NO.	PARAMETER		OPP100		OPP50		UNIT
			MIN	MAX	MIN	MAX	
FSUT16	$t_{d(SE0I-TXENL)}$	Delay time usbc1_icusb_dp (TXDAT, ball AE5) invalid to usbc1_icusb_txen Low	81.8		81.8		ns

(1) See DM Operating Condition Addendum for CORE OPP voltages.

(2) Low-Speed mode is a subset of the Full-Speed mode and it is expected to work at low bandwidth (1.5Mb/s).

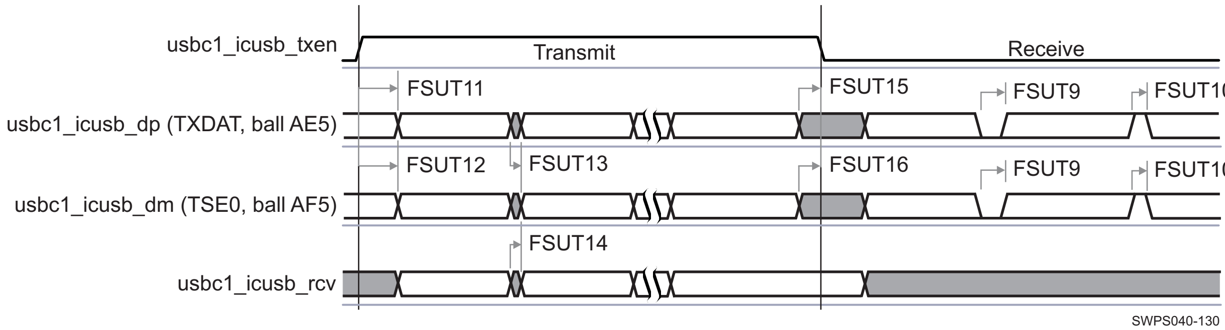

Figure 6-82. Low- / Full-Speed USBC1—Bidirectional Standard 4-pin TLL Mode—1.8 V(1)

(1) To have usbc1_icusb_dm as TXDAT signal, use ball AF5.
To have usbc1_icusb_dp as TXSE0 signal, use ball AE5.

6.6.8.2.3 Low- / Full-Speed USBC1 (FSUSB)—Bidirectional 2-pin Mode

Table 6-129 assumes testing over the recommended operating conditions and electrical characteristic conditions below (see Figure 6-83).

Table 6-128. Low- / Full-Speed USBC1 Timing Conditions—Bidirectional 2-pin Mode—1.8 V, 3.3 V(1)(2)(3)

TIMING CONDITION PARAMETER		VALUE		UNIT
		MIN	MAX	
Input Conditions				
t_R	Input signal rise time	2		ns
t_F	Input signal fall time	2		ns
PCB Conditions				
	Number of external peripherals		1	
	Far end load		10	pF
	Trace length		10	cm
	Characteristics impedance	30	60	Ω

(1) IO settings:
- usbc1_icusb_dp, usbc1_icusb_dm (balls H2, H3): SPEECTRL = 0
  For more information see, USBC1_DR0_SPEEDCTRL register in Control Module / Control Module Functional Description/ Functional Register Description / Signal Integrity Parameter Control Registers with Pad Group Assignment / Device Interfaces Signal Group Controls Mapping section of OMAP4430 TRM.
- Corresponding voltages: 1.8 V, 3.3 V

(2) In this table the rise and fall times are calculated for 10% to 90% of VDDS. For more information on the corresponding OMAP4 VDDS power supply name, see Table 2-1, POWER [9] column with the ball name.

(3) To have an idea of the output OMAP4 ball load supported for this application, you can consider the following:
Output OMAP4 ball load = Far End load + 1.34 pF/cm typical x trace length (cm).

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Table 6-129. Low- / Full-Speed USBC1 Timing Requirements—Bidirectional 2-pin Mode—1.8 V, 3.3 V(1)(2)

NO.	PARAMETER		OPP100		OPP50		UNIT
			MIN	MAX	MIN	MAX	
FSU1	$t_{d(DAT,SE0)}$	Time duration, usbc1_icusb_dp (TXDAT, ball H2) and usbc1_icusb_dm (TSE0, ball H3) low together during transition		14.0		14.0	ns
FSU2	$t_{d(DAT,SE0)}$	Time duration, usbc1_icusb_dp (TXDAT, ball H2) and usbc1_icusb_dm (TSE0, ball H3) high together during transition		8.0		8.0	ns

(1) See DM Operating Condition Addendum for CORE OPP voltages.

(2) Low-Speed mode is a subset of the Full-Speed mode and it is expected to work at low bandwidth (1.5Mb/s).

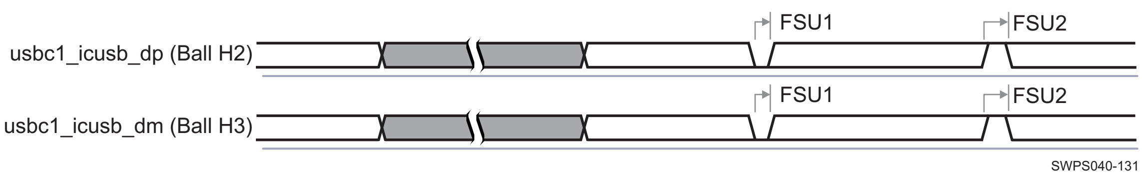

Figure 6-83. Low- / Full-Speed USBC1—Bidirectional 2-pin Mode—1.8 V, 3.3 V(1)

(1) To use usbc1_icusb_dm as TXDAT signal, use ball H3.
To use usbc1_icusb_dp as TXSE0 signal, use ball H2.

6.6.8.3 Universal Serial Bus (USB)—USBB1

NOTE

For more information, see the Serial Communication Interface / High-Speed Multiport USB Host Subsystem section of the OMAP4430 TRM.

6.6.8.3.1 Low- / Full-Speed USBB1 (FSUSB)—Bidirectional Standard 4-pin Mode

Table 6-131 and Table 6-132 assume testing over the recommended operating conditions and electrical characteristic conditions below (see Figure 6-84).

Table 6-130. Low- / Full-Speed USBB1 Timing Conditions—Bidirectional Standard 4-pin Mode—1.8 V(1)(2)(3)

TIMING CONDITION PARAMETER		VALUE		UNIT
		MIN	MAX	
Input Conditions				
t_R	Input signal rise time	2		ns
t_F	Input signal fall time	2		ns
PCB Conditions				
	Number of external peripherals		1	
	Far end load		10	pF
	Trace length		10	cm
	Characteristics impedance	30	60	Ω

(1) IO settings:
- usbb1_mm_txen (ball AF18): MB[1:0] = 10, LB0 = 1
- usbb1_mm_txdat (ball AG18): MB[1:0] = 10, LB0 = 1
- usbb1_mm_txse0 (ball AE17): MB[1:0] = 10, LB0 = 1
- usbb1_mm_rxrcv (ball AF17): MB[1:0] = 10, LB0 = 1
  For more information, see Control Module / Control Module Functional Description/ Functional Register Description / Signal Integrity Parameter Control Registers with Pad Group Assignment / Low Speed I/Os Combined Slew Rate vs TL Length and Load Settings section of the OMAP4430 TRM.
- Corresponding voltage: 1.8 V

(2) In this table the rise and fall times are calculated for 10% to 90% of VDDS. For more information on the corresponding OMAP4 VDDS power supply name, see Table 2-1, POWER [9] column with the ball name.

(3) To have an idea of the output OMAP4 ball load supported for this application, you can consider the following:
Output OMAP4 ball load = Far End load + 1.34 pF/cm typical x trace length (cm).

Table 6-131. Low- / Full-Speed USBB1 Timing Requirements—Bidirectional Standard 4-pin Mode—1.8 V(1)(2)

NO.	PARAMETER		OPP100		OPP50		UNIT
			MIN	MAX	MIN	MAX	
FSU10	$t_{d(DAT,SE0)}$	Time duration, usbb1_mm_txdat and usbb1_mm_txse0 low together during transition		14.0		14.0	ns
FSU11	$t_{d(DAT,SE0)}$	Time duration, usbb1_mm_txdat and usbb1_mm_txse0 high together during transition		8.0		8.0	ns
FSU12	$t_{d(RCVU0)}$	Time duration, usbb1_mm_rxrcv undefined during a Single End 0 (usbb1_mm_txdat and usbb1_mm_txse0 low together)		14.0		14.0	ns
FSU13	$t_{d(RCVU1)}$	Time duration, usbb1_mm_rxrcv undefined during a Single End 1 (usbb1_mm_txdat and usbb1_mm_txse0 high together)		8.0		8.0	ns

(1) See DM Operating Condition Addendum for CORE OPP voltages.

(2) Low-Speed mode is a subset of the Full-Speed mode and it is expected to work at low bandwidth (1.5Mb/s).

Table 6-132. Low- / Full-Speed USBB1 Switching Characteristics—Bidirectional Standard 4-pin Mode—1.8 V(1)(2)

NO.	PARAMETER		OPP100		OPP50		UNIT
			MIN	MAX	MIN	MAX	
FSU14	$t_{d(TXENL-DATV)}$	Delay time usbb1_mm_txen low to usbb1_mm_txdat valid	81.8	84.8	81.8	84.8	ns
FSU15	$t_{d(TXENL-SE0V)}$	Delay time usbb1_mm_txen low to usbb1_mm_txse0 valid	81.8	84.8	81.8	84.8	ns
FSU16	$t_{sk(DAT-SE0)}$	Skew between usbb1_mm_txdat and usbb1_mm_txse0 transition		1.5		1.5	ns
FSU17	$t_{d(DATV-TXENH)}$	Delay time, usbb1_mm_txdat invalid before usbb1_mm_txen high	81.8		81.8		ns
FSU18	$t_{d(SE0V-TXENH)}$	Delay time, usbb1_mm_txse0 invalid before usbb1_mm_txen high	81.8		81.8		ns

(1) See DM Operating Condition Addendum for CORE OPP voltages.

(2) Low-Speed mode is a subset of the Full-Speed mode and it is expected to work at low bandwidth (1.5Mb/s).

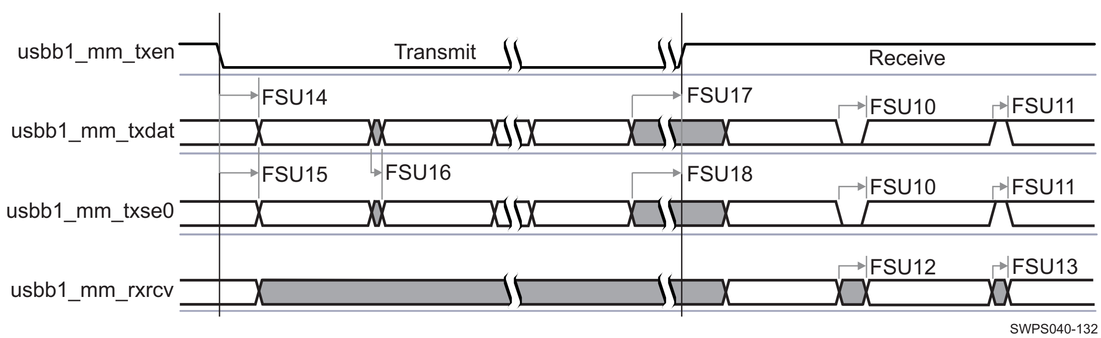

Figure 6-84. Low- / Full-Speed USBB1—Bidirectional Standard 4-pin Mode—1.8 V

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6.6.8.3.2 Low- / Full-Speed USBB1 (FSUSB)—Bidirectional Standard 4-pin TLL Mode

Table 6-134 and Table 6-135 assume testing over the recommended operating conditions and electrical characteristic conditions below (see Figure 6-85).

Table 6-133. Low- / Full-Speed USBB1 Timing Conditions—Bidirectional TLL 4-pin Mode—1.8 V(1)(2)(3)

TIMING CONDITION PARAMETER		VALUE		UNIT
		MIN	MAX	
Input Conditions				
t_R	Input signal rise time	2		ns
t_F	Input signal fall time	2		ns
PCB Conditions				
	Number of external peripherals		1	
	Far end load		10	pF
	Trace length		10	cm
	Characteristics impedance	30	60	Ω

(1) IO settings:
- usbb1_mm_txen (ball AF18): MB[1:0] = 10, LB0 = 1
- usbb1_mm_txdat (ball AG18): MB[1:0] = 10, LB0 = 1
- usbb1_mm_txse0 (ball AE17): MB[1:0] = 10, LB0 = 1
- usbb1_mm_rxrcv (ball AF17): MB[1:0] = 10, LB0 = 1
  For more information, see Control Module / Control Module Functional Description/ Functional Register Description / Signal Integrity Parameter Control Registers with Pad Group Assignment / Low Speed I/Os Combined Slew Rate vs TL Length and Load Settings section of the OMAP4430 TRM.
- Corresponding voltage: 1.8 V

(2) In this table the rise and fall times are calculated for 10% to 90% of VDDS. For more information on the corresponding OMAP4 VDDS power supply name, see Table 2-1, POWER [9] column with the ball name.

(3) To have an idea of the output OMAP4 ball load supported for this application, you can consider the following:
Output OMAP4 ball load = Far End load + 1.34 pF/cm typical x trace length (cm).

Table 6-134. Low- / Full-Speed USBB1 Timing Requirements—Bidirectional TLL 4-pin Mode—1.8 V(1)(2)

NO.	PARAMETER		OPP100		OPP50		UNIT
			MIN	MAX	MIN	MAX	
FSU9	$t_{d(DAT,SE0)}$	Time duration, usbb1_mm_txdat and usbb1_mm_txse0 low together during transition		14.0		14.0	ns
FSU10	$t_{d(DAT,SE0)}$	Time duration, usbb1_mm_txdat and usbb1_mm_txse0 high together during transition		8.0		8.0	ns

(1) See DM Operating Condition Addendum for CORE OPP voltages.

(2) Low-Speed mode is a subset of the Full-Speed mode and it is expected to work at low bandwidth (1.5Mb/s).

Table 6-135. Low- / Full-Speed USBB1 Switching Characteristics—Bidirectional TLL 4-pin Mode—1.8 V(1)(2)

NO.	PARAMETER		OPP100		OPP50		UNIT
			MIN	MAX	MIN	MAX	
FSU11	$t_{d(TXENL-DATV)}$	Delay time usbb1_mm_txen low to usbb1_mm_txdat valid	81.8	84.8	81.8	84.8	ns
FSU12	$t_{d(TXENL-SE0V)}$	Delay time usbb1_mm_txen low to usbb1_mm_txse0 valid	81.8	84.8	81.8	84.8	ns
FSU13	$t_{sk(DAT-SE0)}$	Skew between usbb1_mm_txdat and usbb1_mm_txse0 transition		1.5		1.5	ns
FSU14	$t_{sk(DAT-SE0)}$	Skew between usbb1_mm_txdat, usbb1_txse0 and usbb1_mm_rxrcv transition		1.5		1.5	ns

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Table 6-135. Low- / Full-Speed USBB1 Switching Characteristics—Bidirectional TLL 4-pin Mode—1.8 V(1)(2) (continued)

NO.	PARAMETER		OPP100		OPP50		UNIT
			MIN	MAX	MIN	MAX	
FSU15	$t_{d(DATV-TXENH)}$	Delay time, usbb1_mm_txdat invalid before usbb1_mm_txen high	81.8		81.8		ns
FSU16	$t_{d(SE0V-TXENH)}$	Delay time, usbb1_mm_txse0 invalid before usbb1_mm_txen high	81.8		81.8		ns

(1) See DM Operating Condition Addendum for CORE OPP voltages.

(2) Low-Speed mode is a subset of the Full-Speed mode and it is expected to work at low bandwidth (1.5Mb/s).

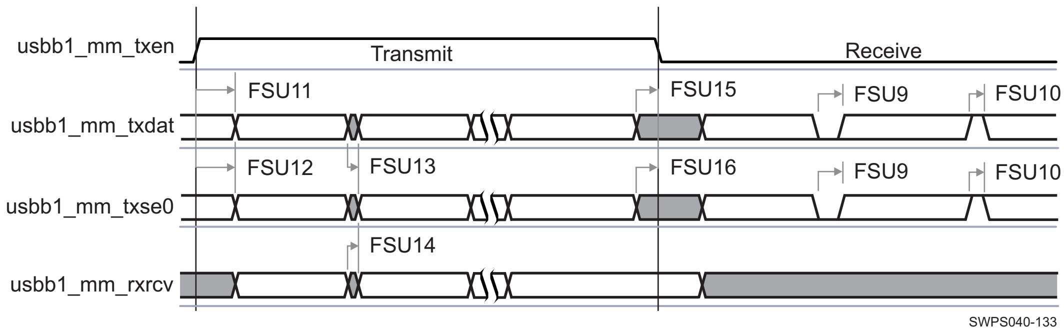

Figure 6-85. Low- / Full-Speed USBB1—Bidirectional TLL 4-pin Mode—1.8 V

6.6.8.3.3 Low- / Full-Speed USBB1 (FSUSB)—Bidirectional Standard 3-pin Mode

Table 6-137 and Table 6-138 assume testing over the recommended operating conditions and electrical characteristic conditions below (see Figure 6-86).

Table 6-136. Low- / Full-Speed USBB1 Timing Conditions—Bidirectional Standard 3-pin Mode—1.8 V(1)(2)(3)

TIMING CONDITION PARAMETER		VALUE		UNIT
		MIN	MAX	
Input Conditions				
t_R	Input signal rise time	2		ns
t_F	Input signal fall time	2		ns
PCB Conditions				
	Number of external peripherals		1	
	Far end load		10	pF
	Trace length		10	cm
	Characteristics impedance	30	60	Ω

(1) IO settings:
- usbb1_mm_txen (ball AF18): MB[1:0] = 10, LB0 = 1
- usbb1_mm_txdat (ball AG18): MB[1:0] = 10, LB0 = 1
- usbb1_mm_txse0 (ball AE17): MB[1:0] = 10, LB0 = 1
  For more information, see Control Module / Control Module Functional Description/ Functional Register Description / Signal Integrity Parameter Control Registers with Pad Group Assignment / Low Speed I/Os Combined Slew Rate vs TL Length and Load Settings section of the OMAP4430 TRM.
- Corresponding voltage: 1.8 V

(2) In this table the rise and fall times are calculated for 10% to 90% of VDDS. For more information on the corresponding OMAP4 VDDS power supply name, see Table 2-1, POWER [9] column with the ball name.

(3) To have an idea of the output OMAP4 ball load supported for this application, you can consider the following:
Output OMAP4 ball load = Far End load + 1.34 pF/cm typical x trace length (cm).

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Table 6-137. Low- / Full-Speed USBB1 Timing Requirements—Bidirectional Standard 3-pin Mode—1.8 V(1)(2)

NO.	PARAMETER		OPP100		OPP50		UNIT
			MIN	MAX	MIN	MAX	
FSU19	$t_{d(DAT,SE0)}$	Time duration, usbb1_mm_txdat and usbb1_mm_txse0 low together during transition		14.0		14.0	ns
FSU20	$t_{d(DAT,SE0)}$	Time duration, usbb1_mm_txdat and usbb1_mm_txse0 high together during transition		8.0		8.0	ns

(1) See DM Operating Condition Addendum for CORE OPP voltages.

(2) Low-Speed mode is a subset of the Full-Speed mode and it is expected to work at low bandwidth (1.5Mb/s).

Table 6-138. Low- / Full-Speed USBB1 Switching Characteristics—Bidirectional Standard 3-pin Mode—1.8 V(1)(2)

NO.	PARAMETER		OPP100		OPP50		UNIT
			MIN	MAX	MIN	MAX	
FSU21	$t_{d(TXENL-DATV)}$	Delay time usbb1_mm_txen low to usbb1_mm_txdat valid	81.8	84.8	81.8	84.8	ns
FSU22	$t_{d(TXENL-SE0V)}$	Delay time usbb1_mm_txen low to usbb1_mm_txse0 valid	81.8	84.8	81.8	84.8	ns
FSU23	$t_{sk(DAT-SE0)}$	Skew between usbb1_mm_txdat and usbb1_mm_txse0 transition		1.5		1.5	ns
FSU24	$t_{d(DATV-TXENH)}$	Delay time, usbb1_mm_txdat invalid before usbb1_mm_txen high	81.8		81.8		ns
FSU25	$t_{d(SE0V-TXENH)}$	Delay time, usbb1_mm_txse0 invalid before usbb1_mm_txen high	81.8		81.8		ns

(1) See DM Operating Condition Addendum for CORE OPP voltages.

(2) Low-Speed mode is a subset of the Full-Speed mode and it is expected to work at low bandwidth (1.5Mb/s).

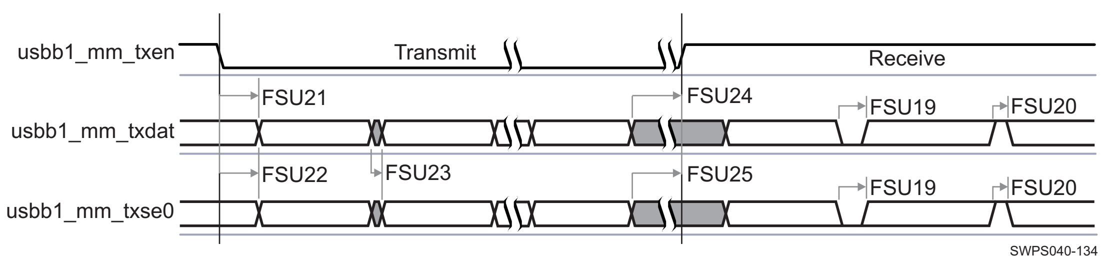

Figure 6-86. Low- / Full-Speed USBB1—Bidirectional Standard 3-pin Mode—1.8 V

6.6.8.3.4 Low- / Full-Speed USBB1 (FSUSB)—Bidirectional Standard 3-pin TLL Mode

Table 6-140 and Table 6-141 assume testing over the recommended operating conditions and electrical characteristic conditions below (see Figure 6-87).

Table 6-139. Low- / Full-Speed USBB1 Timing Conditions—Bidirectional TLL 3-pin Mode—1.8 V(1)(2)(3)

TIMING CONDITION PARAMETER		VALUE		UNIT
		MIN	MAX	
Input Conditions				
t_R	Input signal rise time	2		ns
t_F	Input signal fall time	2		ns
PCB Conditions				
	Number of external peripherals		1	

Table 6-139. Low- / Full-Speed USBB1 Timing Conditions—Bidirectional TLL 3-pin Mode—1.8 V(1)(2)(3) (continued)

TIMING CONDITION PARAMETER		VALUE		UNIT
		MIN	MAX	
	Far end load		10	pF
	Trace length		10	cm
	Characteristics impedance	30	60	Ω

(1) IO settings:
- usbb1_mm_txen (ball AF18): MB[1:0] = 10, LB0 = 1
- usbb1_mm_txdat (ball AG18): MB[1:0] = 10, LB0 = 1
- usbb1_mm_txse0 (ball AE17): MB[1:0] = 10, LB0 = 1
  For more information, see Control Module / Control Module Functional Description/ Functional Register Description / Signal Integrity Parameter Control Registers with Pad Group Assignment / Low Speed I/Os Combined Slew Rate vs TL Length and Load Settings section of the OMAP4430 TRM.
- Corresponding voltage: 1.8 V

(2) In this table the rise and fall times are calculated for 10% to 90% of VDDS. For more information on the corresponding OMAP4 VDDS power supply name, see Table 2-1, POWER [9] column with the ball name.

(3) To have an idea of the output OMAP4 ball load supported for this application, you can consider the following:
Output OMAP4 ball load = Far End load + 1.34 pF/cm typical x trace length (cm).

Table 6-140. Low- / Full-Speed USBB1 Timing Requirements—Bidirectional TLL 3-pin Mode—1.8 V(1)(2)

NO.	PARAMETER		OPP100		OPP50		UNIT
			MIN	MAX	MIN	MAX	
FSU17	$t_{d(DAT,SE0)}$	Time duration, usbb1_mm_txdat and usbb1_mm_txse0 low together during transition		14.0		14.0	ns
FSU18	$t_{d(DAT,SE0)}$	Time duration, usbb1_mm_txdat and usbb1_mm_txse0 high together during transition		8.0		8.0	ns

(1) See DM Operating Condition Addendum for CORE OPP voltages.

(2) Low-Speed mode is a subset of the Full-Speed mode and it is expected to work at low bandwidth (1.5Mb/s).

Table 6-141. Low- / Full-Speed USBB1 Switching Characteristics—Bidirectional TLL 3-pin Mode—1.8 V(1)(2)

NO.	PARAMETER		OPP100		OPP50		UNIT
			MIN	MAX	MIN	MAX	
FSU19	$t_{d(TXENL-DATV)}$	Delay time usbb1_mm_txen low to usbb1_mm_txdat valid	81.8	84.8	81.8	84.8	ns
FSU20	$t_{d(TXENL-SE0V)}$	Delay time usbb1_mm_txen low to usbb1_mm_txse0 valid	81.8	84.8	81.8	84.8	ns
FSU21	$t_{sk(DAT-SE0)}$	Skew between usbb1_mm_txdat and usbb1_mm_txse0 transition		1.5		1.5	ns
FSU22	$t_{d(DATV-TXENH)}$	Delay time, usbb1_mm_txdat invalid before usbb1_mm_txen high	81.8		81.8		ns
FSU23	$t_{d(SE0V-TXENH)}$	Delay time, usbb1_mm_txse0 invalid before usbb1_mm_txen high	81.8		81.8		ns

(1) See DM Operating Condition Addendum for CORE OPP voltages.

(2) Low-Speed mode is a subset of the Full-Speed mode and it is expected to work at low bandwidth (1.5Mb/s).

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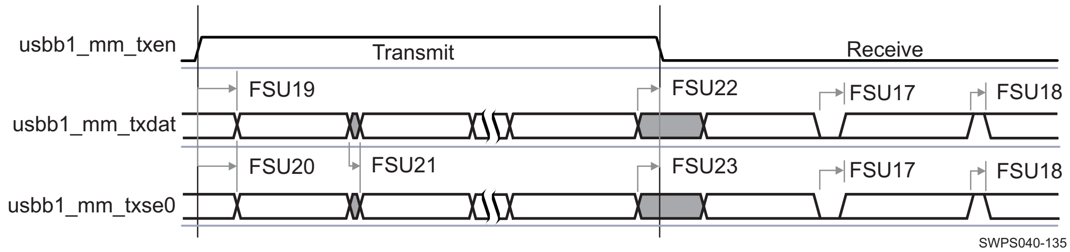

Figure 6-87. Low- / Full-Speed USBB1—Bidirectional TLL 3-pin Mode—1.8 V

6.6.8.3.5 High-Speed USBB1 (HSUSB)—ULPI SDR Mode—Slave Mode

Table 6-143 and Table 6-144 assume testing over the recommended operating conditions and electrical characteristic conditions below (see Figure 6-88).

Table 6-142. High-Speed USBB1 Timing Conditions—ULPI SDR Mode—1.8 V(1)(2)(3)

SYSTEM CONDITION PARAMETER		VALUE		UNIT
		MIN	MAX	
Input Conditions				
t_R	Input signal rise time	1.00	3.00	ns
t_F	Input signal fall time	1.00	3.00	ns
PCB Conditions				
	Number of external peripherals		1	
	Far end load		5	pF
	Trace length		5	cm
	Characteristics impedance	30	60	Ω

(1) IO settings:
- usbb1_ulpiphy_clk (ball AE18): DS0 = 0
  For more information, see Control Module / Control Module Functional Description/ Functional Register Description / Signal Integrity Parameter Control Registers with Pad Group Assignment / I/O cells with Configurable Output Driver Impedance section of the OMAP4430 TRM.
- usbb1_ulpiphy_stp (ball AG19): MB[1:0] = 11 and LB0 = 1
- usbb1_ulpiphy_dir (ball AF19): MB[1:0] = 11 and LB0 = 1
- usbb1_ulpiphy_nxt (ball AE19): MB[1:0] = 11 and LB0 = 1
- usbb1_ulpiphy_dat[7:0] (balls AG16 / AF16 / AE16 / AH17 / AF17 / AE17 / AG18 / AF18): MB[1:0] = 11 and LB0 = 1
  For more information, see Control Module / Control Module Functional Description/ Functional Register Description / Signal Integrity Parameter Control Registers with Pad Group Assignment / Low Speed I/Os Combined Slew Rate vs TL Length and Load Settings section of the OMAP4430 TRM.
- Corresponding voltage: 1.8 V

(2) In this table the rise and fall times are calculated for 10% to 90% of VDDS. For more information on the corresponding OMAP4 VDDS power supply name, see Table 2-1, POWER [9] column with the ball name.

(3) To have an idea of the output OMAP4 ball load supported for this application, you can consider the following:
Output OMAP4 ball load = Far End load + 1.34 pF/cm typical x trace length (cm).

Table 6-143. High-Speed USBB1 Timing Requirements—ULPI SDR Mode—Slave Mode—1.8 V(4)

NO.	PARAMETER		OPP100		UNIT
			MIN	MAX	
US1	$1 / t_{c(clk)}$	Frequency(1), usbb1_ulpiphy_clk		60	MHz
US2	$t_{w(clkH)}$	Typical pulse duration, usbb1_ulpiphy_clk high	0.5*P(2)		ns
US3	$t_{w(clkL)}$	Typical pulse duration, usbb1_ulpiphy_clk low	0.5*P(2)		ns
	$t_{dc(clk)}$	Duty cycle error, usbb1_ulpiphy_clk	–833	833	ps
	$t_{j(clk)}$	Jitter standard deviation(3), usbb1_ulpiphy_clk		500	ps
US5	$t_{su(ctrlV-clkH)}$	Setup time, usbb1_ulpiphy_dir and usbb1_ulpiphy_nxt valid before usbb1_ulpiphy_clk rising edge	6.73		ns

Table 6-143. High-Speed USBB1 Timing Requirements—ULPI SDR Mode—Slave Mode—1.8 V[(4)] (continued)

NO.	PARAMETER		OPP100		UNIT
			MIN	MAX	
US6	$t_{h(clkH-ctrlV)}$	Hold time, usbb1_ulpiphy_dir and usbb1_ulpiphy_nxt valid after usbb1_ulpiphy_clk rising edge	0.00		ns
US7	$t_{su(dV-clkH)}$	Setup time, input usbb1_ulpiphy_dat[7:0] valid before usbb1_ulpiphy_clk rising edge	6.73		ns
US8	$t_{h(clkH-dV)}$	Hold time, input usbb1_ulpiphy_dat[7:0] valid after usbb1_ulpiphy_clk rising edge	0.00		ns

(1) Related to the input maximum frequency supported by the USB module.
(2) P = clk period in ns
(3) Maximum cycle jitter supported by clk input clock.
(4) See DM Operating Condition Addendum for CORE OPP voltages.

Table 6-144. High-Speed USBB1 Switching Characteristics—ULPI SDR Mode—Slave Mode—1.8 V[(1)]

NO.	PARAMETER		OPP100		UNIT
			MIN	MAX	
Ball: AE18 (usbb1_ulpiphy_clk)					
US4	$t_{d(clkL-ctrlV)}$	Delay time, usbb1_ulpiphy_clk rising edge high to output usbb1_ulpiphy_stp valid	0.40	8.34	ns
US9	$t_{d(clkL-doV)}$	Delay time, usbb1_ulpiphy_clk rising edge to output usbb1_ulpiphy_dat[7:0] valid	0.40	8.34	ns
Balls: AG19 / AF19 / AE19 / AF18 / AG18 / AE17 / AF17 / AH17 / AE16 / AF16 / AG16 (usbb1_ulpiphy_stp, usbb1_ulpiphy_dir, usbb1_ulpiphy_nxt, usbb1_ulpiphy_dat[7:0])					
US4	$t_{d(clkL-ctrlV)}$	Delay time, usbb1_ulpiphy_clk rising edge high to output usbb1_ulpiphy_stp valid	0.22	8.60	ns
	$t_{R(ctrl)}$	Rise time, output usbb1_ulpiphy_stp		3.0	ps
	$t_{F(dtrl)}$	Fall time, output usbb1_ulpiphy_stp		3.0	ps
US9	$t_{d(clkL-doV)}$	Delay time, usbb1_ulpiphy_clk rising edge to output usbb1_ulpiphy_dat[7:0] valid	0.22	8.60	ns
	$t_{R(do)}$	Rise time, output usbb1_ulpiphy_dat[7:0]		3.0	ps
	$t_{F(do)}$	Fall time, output usbb1_ulpiphy_dat[7:0]		3.0	ps

(1) See DM Operating Condition Addendum for CORE OPP voltages.

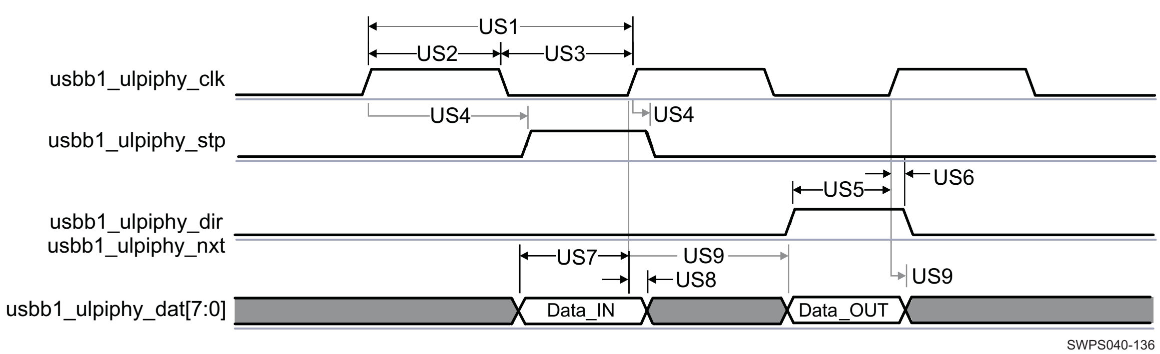

Figure 6-88. High-Speed USBB1—ULPI SDR Mode—Slave Mode—1.8 V

6.6.8.3.6 High-Speed USBB1 (HSUSB)—ULPI TLL Mode—Master Mode

Table 6-146 and Table 6-147 assume testing over the recommended operating conditions and electrical characteristic conditions below (see Figure 6-89).

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Table 6-145. High-Speed USBB1 Timing Conditions—ULPI TLL Mode—Master Mode—1.8 V(1)(2)(3)

SYSTEM CONDITION PARAMETER		VALUE		UNIT
		MIN	MAX	
Input Conditions				
t_R	Input signal rise time	1.00	3.00	ns
t_F	Input signal fall time	1.00	3.00	ns
PCB Conditions				
	Number of external peripherals		1	
	Far end load		5	pF
	Trace length		5	cm
	Characteristics impedance	30	60	Ω

(1) IO settings:
- usbb1_ulpitll_clk (ball AE18): DS0 = 0
  For more information, see Control Module / Control Module Functional Description/ Functional Register Description / Signal Integrity Parameter Control Registers with Pad Group Assignment / I/O cells with Configurable Output Driver Impedance section of the OMAP4430 TRM.
- usbb1_ulpitll_stp (ball AG19): MB[1:0] = 11 and LB0 = 1
- usbb1_ulpitll_dir (ball AF19): MB[1:0] = 11 and LB0 = 1
- usbb1_ulpitll_nxt (ball AE19): MB[1:0] = 11 and LB0 = 1
- usbb1_ulpitll_dat[7:0] (balls AG16 / AF16 / AE16 / AH17 / AF17 / AE17 / AG18 / AF18): MB[1:0] = 11 and LB0 = 1
  For more information, see Control Module / Control Module Functional Description/ Functional Register Description / Signal Integrity Parameter Control Registers with Pad Group Assignment / Low Speed I/Os Combined Slew Rate vs TL Length and Load Settings section of the OMAP4430 TRM.
- Corresponding voltage: 1.8 V

(2) In this table the rise and fall times are calculated for 10% to 90% of VDDS. For more information on the corresponding OMAP4 VDDS power supply name, see Table 2-1, POWER [9] column with the ball name.

(3) To have an idea of the output OMAP4 ball load supported for this application, you can consider the following:
Output OMAP4 ball load = Far End load + 1.34 pF/cm typical x trace length (cm).

Table 6-146. High-Speed USBB1 Timing Requirements—ULPI TLL Mode—Master Mode—1.8 V(1)

NO.	PARAMETER		OPP100		OPP50		UNIT
			MIN	MAX	MIN	MAX	
For ball: AE18 (usbb1_ulpitll_clk)							
UT4	$t_{su(ctrlV-clkH)}$	Setup time, usbb1_ulpitll_stp valid before usbb1_ulpitll_clk rising edge	5.78		5.78		ns
UT5	$t_{h(clkH-ctrlV)}$	Hold time, usbb1_ulpitll_stp valid after usbb1_ulpitll_clk rising edge	0.09		0.09		ns
UT6	$t_{su(dV-clkH)}$	Setup time, usbb1_ulpitll_dat[7:0] valid before usbb1_ulpitll_clk rising edge	5.78		5.78		ns
UT7	$t_{h(clkH-dV)}$	Hold time, usbb1_ulpitll_dat[7:0] valid after usbb1_ulpitll_clk rising edge	0.09		0.09		ns
For balls: AG19 / AF19 / AE19 / AF18 / AG18 / AE17 / AF17 / AH17 / AE16 / AF16 / AG16 (usbb1_ulpitll_stp, usbb1_ulpitll_dir, usbb1_ulpitll_nxt, usbb1_ulpitll_dat[7:0])							
UT4	$t_{su(ctrlV-clkH)}$	Setup time, usbb1_ulpitll_stp valid before usbb1_ulpitll_clk rising edge	5.86		5.86		ns
UT5	$t_{h(clkH-ctrlV)}$	Hold time, usbb1_ulpitll_stp valid after usbb1_ulpitll_clk rising edge	0.13		0.13		ns
UT6	$t_{su(dV-clkH)}$	Setup time, usbb1_ulpitll_dat[7:0] valid before usbb1_ulpitll_clk rising edge	5.86		5.86		ns
UT7	$t_{h(clkH-dV)}$	Hold time, usbb1_ulpitll_dat[7:0] valid after usbb1_ulpitll_clk rising edge	0.13		0.13		ns

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(1) See DM Operating Condition Addendum for CORE OPP voltages.

Table 6-147. High-Speed USBB1 Switching Characteristics—ULPI TLL Mode—Master Mode—1.8 V[(4)]

NO.	PARAMETER		OPP100		OPP50		UNIT
			MIN	MAX	MIN	MAX	
UT1	$1 / t_{c(clk)}$	Frequency[(1)], output usbb1_ulpitll_clk		60		60	MHz
UT2	$t_{w(clkH)}$	Typical pulse duration, output usbb1_ulpitll_clk high	0.5*P[(2)]		0.5*P[(2)]		ns
UT3	$t_{w(clkL)}$	Typical pulse duration, output usbb1_ulpitll_clk low	0.5*P[(2)]		0.5*P[(2)]		ns
	$t_{dc(clk)}$	Duty cycle error, output usbb1_ulpitll_clk	–833	833	–833	833	ps
	$t_{j(clk)}$	Jitter standard deviation[(3)], output usbb1_ulpitll_clk		400		400	ps
	$t_{R(clk)}$	Rising time, output usbb1_ulpitll_clk		3.0		3.0	ps
	$t_{F(clk)}$	Falling time, output usbb1_ulpitll_clk		3.0		3.0	ps
UT8	$t_{d(clkL-ctrlV)}$	Delay time, output usbb1_ulpitll_clk rising edge to output usbb1_ulpitll_dir and usbb1_ulpitll_nxt	0.04	8.96	0.04	8.96	ns
	$t_{R(ctrl)}$	Rising time, output usbb1_ulpitll_dir and usbb1_ulpitll_nxt		3.0		3.0	ps
	$t_{F(dtrl)}$	Falling time, output usbb1_ulpitll_dir and usbb1_ulpitll_nxt		3.0		3.0	ps
UT9	$t_{d(clkL-doV)}$	Delay time, output usbb1_ulpitll_clk rising edge to output usbb1_ulpitll_dat[7:0] valid	0.04	8.96	0.04	8.96	ns
	$t_{R(do)}$	Rising time, output usbb1_ulpitll_dat[7:0]		3.0		3.0	ps
	$t_{F(do)}$	Falling time, output usbb1_ulpitll_dat[7:0]		3.0		3.0	ps

(1) Related to the input maximum frequency supported by the USB module.
(2) P = output clk period in ns
(3) The jitter probability density can be approximated by a Gaussian function.
(4) See DM Operating Condition Addendum for CORE OPP voltages.

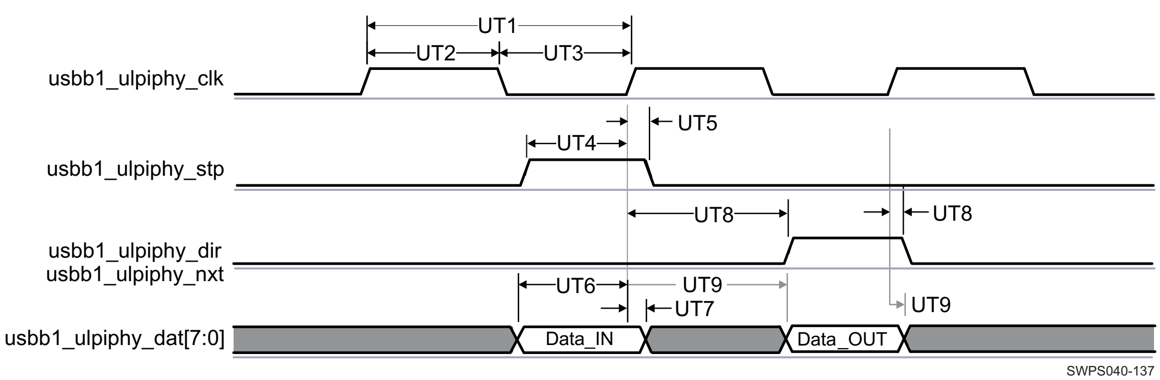

Figure 6-89. High-Speed USBB1—ULPI TLL Mode—Master Mode—1.8 V

6.6.8.3.7 *High-Speed USBB1 (HSUSB)—High-Speed InterChip Interface 1 (HSIC1)*

High-Speed InterChip (HSIC) is an alternative to the standard USB physical layer targeted at fixed, inter-chip communications. This implies short distances between devices, and allows for simpler, smaller, more power-efficient PHYs over a single-ended, 2-wire interface running at a fixed HS speed. HSIC must be identical to standard USB from a high-level application standpoint.

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6.6.8.3.7.1 High-Speed USBB1—HSIC DDR Receive And Transmit Modes—1.2 V

Table 6-149 and Table 6-150 assume testing over the recommended operating conditions and electrical characteristic conditions below (see Figure 6-90).

Table 6-148. High-Speed USBB1—HSIC DDR Timing Conditions—1.2 V(1)(2)(3)

SYSTEM CONDITION PARAMETER		VALUE		UNIT
		MIN	MAX	
Input Conditions				
t_R	Input signal rise time	0.29	0.58	ns
t_F	Input signal fall time	0.29	0.58	ns
PCB Conditions				
	Number of external peripherals		1	
	Far end load		5	pF
	Trace length		4	cm
	Characteristics impedance	45	55	Ω

(1) IO settings:
- usbb1_hsic_data, usbb1_hsic_strobe (Balls AF14 / AE14): sr[2:0] = 010 and i[2:0] = 110
  For more information, see Control Module / Control Module Functional Description / Functional Register Description / Signal Integrity Parameter Control Registers with Pad Group Assignment / High-speed I/O Buffers with Impedance, Slew Rate and Weak Driver Settings section of OMAP4430 TRM.
- Corresponding voltage: 1.2 V

(2) In this table the rise and fall times are calculated for 30% to 70% of VDDS. For more information on the corresponding OMAP4 VDDS power supply name, see Table 2-1, POWER [9] column with the ball name.

(3) To have an idea of the output OMAP4 ball load supported for this application, you can consider the following:
Output OMAP4 ball load = Far End load + 1.34 pF/cm typical x trace length (cm).

Table 6-149. High-Speed USBB1 Timing Requirements—HSIC DDR Receive Mode—1.2 V(3)

NO.	PARAMETER		OPP100		UNIT
			MIN	MAX	
HSIC1	$1 / t_{c(clk)}$	Frequency(1), usbb1_hsic_strobe period		240	MHz
HSIC2	$t_{w(clkH)}$	Typical pulse duration, usbb1_hsic_strobe high	0.5*P(2)		ns
HSIC3	$t_{w(clkL)}$	Typical pulse duration, usbb1_hsic_strobe low	0.5*P(2)		ns
HSIC5	$t_{su(strobe-dataV)}$	Setup time, usbb1_hsic_data valid before usbb1_hsic_strobe low/high	0.271		ns
HSIC6	$t_{h(strobe-dataV)}$	Hold time, usbb1_hsic_data valid after usbb1_hsic_strobe low/high	0.271		ns

(1) Related to the maximum USB HSIC frequency.

(2) P = input clock period in ns

(3) See DM Operating Condition Addendum for CORE OPP voltages.

Table 6-150. High-Speed USBB1 Switching Characteristics—HSIC DDR Transmit Mode—1.2 V(3)

NO.	PARAMETER		OPP100		UNIT
			MIN	MAX	
HSIC1	$1 / t_{c(clk)}$	Frequency(1), usbb1_hsic_strobe period		240	MHz
HSIC2	$t_{w(clkH)}$	Typical pulse duration, usbb1_hsic_strobe high	0.5*P(2)		ns
HSIC3	$t_{w(clkL)}$	Typical pulse duration, usbb1_hsic_strobe low	0.5*P(2)		ns
	$t_{dc(clk)}$	Duty cycle error, usbb1_hsic_strobe	–83	83	ps
	$t_{R(clk)}$	Rise time, usbb1_hsic_strobe	0.39	0.56	ns
	$t_{F(clk)}$	Fall time, usbb1_hsic_strobe	0.39	0.56	ns
HSIC4	$t_{d(clk-dataV)}$	Delay time, usbb1_hsic_strobe low/high to usbb1_hsic_data valid	–0.325	0.325	ns
	$t_{R(do)}$	Rise time, output data usbb1_hsic_data	0.39	0.56	ns
	$t_{F(do)}$	Falli ime, output data usbb1_hsic_data	0.39	0.56	ns

(1) Related to the maximum USB HSIC frequency.

(2) P = output clock period in ns

(3) See DM Operating Condition Addendum for CORE OPP voltages.

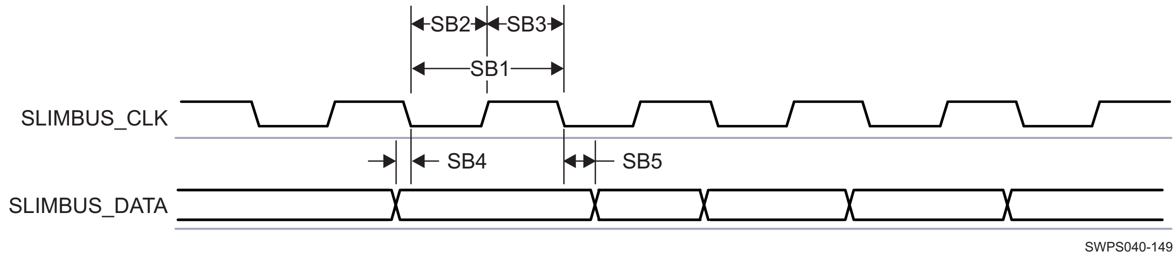

Figure 6-90. High-Speed USBB1—HSIC DDR Receive And Transmit Modes—1.2 V

6.6.8.4 Universal Serial Bus (USB)—USBB2

NOTE

For more information, see the Serial Communication Interface / High-Speed Multiport USB Host Subsystem section of the OMAP4430 TRM.

6.6.8.4.1 Low- / Full-Speed USBB2 (FSUSB)—Bidirectional Standard 4-pin Mode

Table 6-152 and Table 6-153 assume testing over the recommended operating conditions and electrical characteristic conditions below (see Figure 6-91).

Table 6-151. Low- / Full-Speed USBB2 Timing Conditions—Bidirectional Standard 4-pin Mode—1.8 V(1)(2)(3)

TIMING CONDITION PARAMETER		VALUE		UNIT
		MIN	MAX	
Input Conditions				
t_R	Input signal rise time	2		ns
t_F	Input signal fall time	2		ns
PCB Conditions				
	Number of external peripherals		1	
	Far end load		10	pF
	Trace length		10	cm
	Characteristics impedance	30	60	Ω

(1) IO settings:

- usbb2_mm_txen (ball AC28): MB[1:0] = 10, LB0 = 1
- usbb2_mm_txdat (ball AF24): MB[1:0] = 10, LB0 = 1
- usbb2_mm_txse0 (ball AE24): MB[1:0] = 10, LB0 = 1
- usbb2_mm_rxrcv (ball AD25): MB[1:0] = 10, LB0 = 1
  For more information, see Control Module / Control Module Functional Description/ Functional Register Description / Signal Integrity Parameter Control Registers with Pad Group Assignment / 50-Ω Output Buffer I/Os with Combined Mode and Load Settings section of the OMAP4430 TRM.
- Corresponding voltage: 1.8 V

(2) In this table the rise and fall times are calculated for 10% to 90% of VDDS. For more information on the corresponding OMAP4 VDDS power supply name, see Table 2-1, POWER [9] column with the ball name.

(3) To have an idea of the output OMAP4 ball load supported for this application, you can consider the following:
Output OMAP4 ball load = Far End load + 1.34 pF/cm typical x trace length (cm).

Table 6-152. Low- / Full-Speed USBB2 Timing Requirements—Bidirectional Standard 4-pin Mode—1.8 V(1)(2)

NO.	PARAMETER		OPP100		OPP50		UNIT
			MIN	MAX	MIN	MAX	
FSU10	$t_{d(DAT,SE0)}$	Time duration, usbb2_mm_txdat and usbb2_mm_txse0 low together during transition		14.0		14.0	ns
FSU11	$t_{d(DAT,SE0)}$	Time duration, usbb2_mm_txdat and usbb2_mm_txse0 high together during transition		8.0		8.0	ns
FSU12	$t_{d(RCVU0)}$	Time duration, usbb2_mm_rxrcv undefined during a Single End 0 (usbb2_mm_txdat and usbb2_mm_txse0 low together)		14.0		14.0	ns
FSU13	$t_{d(RCVU1)}$	Time duration, usbb2_mm_rxrcv undefined during a Single End 1 (usbb2_mm_txdat and usbb2_mm_txse0 high together)		8.0		8.0	ns

(1) See DM Operating Condition Addendum for CORE OPP voltages.

(2) Low-Speed mode is a subset of the Full-Speed mode and it is expected to work at low bandwidth (1.5Mb/s).

Table 6-153. Low- / Full-Speed USBB2 Switching Characteristics—Bidirectional Standard 4-pin Mode—1.8 V(1)(2)

NO.	PARAMETER		OPP100		OPP50		UNIT
			MIN	MAX	MIN	MAX	
FSU14	$t_{d(TXENL-DATV)}$	Delay time usbb2_mm_txen low to usbb2_mm_txdat valid	81.8	84.8	81.8	84.8	ns
FSU15	$t_{d(TXENL-SE0V)}$	Delay time usbb2_mm_txen low to usbb2_mm_txse0 valid	81.8	84.8	81.8	84.8	ns
FSU16	$t_{sk(DAT-SE0)}$	Skew between usbb2_mm_txdat and usbb2_mm_txse0 transition		1.5		1.5	ns
FSU17	$t_{d(DATV-TXENH)}$	Delay time, usbb2_mm_txdat invalid before usbb2_mm_txen high	81.8		81.8		ns
FSU18	$t_{d(SE0V-TXENH)}$	Delay time, usbb2_mm_txse0 invalid before usbb2_mm_txen high	81.8		81.8		ns

(1) See DM Operating Condition Addendum for CORE OPP voltages.

(2) Low-Speed mode is a subset of the Full-Speed mode and it is expected to work at low bandwidth (1.5Mb/s).

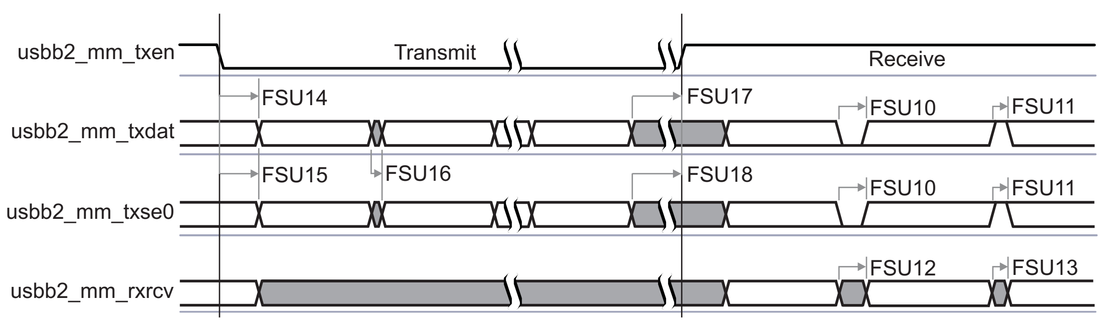

Figure 6-91. Low- / Full-Speed USBB2—Bidirectional Standard 4-pin Mode—1.8 V

6.6.8.4.2 Low- / Full-Speed USBB2 (FSUSB)—Bidirectional Standard 4-pin TLL Mode

Table 6-155 and Table 6-156 assume testing over the recommended operating conditions and electrical characteristic conditions below (see Figure 6-92).

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Table 6-154. Low- / Full-Speed USBB2 Timing Conditions—Bidirectional TLL 4-pin Mode—1.8 V(1)(2)(3)

TIMING CONDITION PARAMETER		VALUE		UNIT
		MIN	MAX	
Input Conditions				
t_R	Input signal rise time	2		ns
t_F	Input signal fall time	2		ns
PCB Conditions				
	Number of external peripherals		1	
	Far end load		10	pF
	Trace length		10	cm
	Characteristics impedance	30	60	Ω

(1) IO settings:
- usbb2_mm_txen (ball AC28): MB[1:0] = 10, LB0 = 1
- usbb2_mm_txdat (ball AF24): MB[1:0] = 10, LB0 = 1
- usbb2_mm_txse0 (ball AE24): MB[1:0] = 10, LB0 = 1
- usbb2_mm_rxrcv (ball AD25): MB[1:0] = 10, LB0 = 1
  For more information, see Control Module / Control Module Functional Description/ Functional Register Description / Signal Integrity Parameter Control Registers with Pad Group Assignment / 50-Ω Output Buffer I/Os with Combined Mode and Load Settings section of the OMAP4430 TRM.
- Corresponding voltage: 1.8 V

(2) In this table the rise and fall times are calculated for 10% to 90% of VDDS. For more information on the corresponding OMAP4 VDDS power supply name, see Table 2-1, POWER [9] column with the ball name.

(3) To have an idea of the output OMAP4 ball load supported for this application, you can consider the following:
Output OMAP4 ball load = Far End load + 1.34 pF/cm typical x trace length (cm).

Table 6-155. Low- / Full-Speed USBB2 Timing Requirements—Bidirectional TLL 4-pin Mode—1.8 V(1)(2)

NO.	PARAMETER		OPP100		OPP50		UNIT
			MIN	MAX	MIN	MAX	
FSU9	$t_{d(DAT,SE0)}$	Time duration, usbb2_mm_txdat and usbb2_mm_txse0 low together during transition		14.0		14.0	ns
FSU10	$t_{d(DAT,SE0)}$	Time duration, usbb2_mm_txdat and usbb2_mm_txse0 high together during transition		8.0		8.0	ns

(1) See DM Operating Condition Addendum for CORE OPP voltages.

(2) Low-Speed mode is a subset of the Full-Speed mode and it is expected to work at low bandwidth (1.5Mb/s).

Table 6-156. Low- / Full-Speed USBB2 Switching Characteristics—Bidirectional TLL 4-pin Mode—1.8 V(1)(2)

NO.	PARAMETER		OPP100		OPP50		UNIT
			MIN	MAX	MIN	MAX	
FSU11	$t_{d(TXENL-DATV)}$	Delay time usbb2_mm_txen low to usbb2_mm_txdat valid	81.8	84.8	81.8	84.8	ns
FSU12	$t_{d(TXENL-SE0V)}$	Delay time usbb2_mm_txen low to usbb2_mm_txse0 valid	81.8	84.8	81.8	84.8	ns
FSU13	$t_{sk(DAT-SE0)}$	Skew between usbb2_mm_txdat and usbb2_mm_txse0 transition		1.5		1.5	ns
FSU14	$t_{sk(DAT-SE0)}$	Skew between usbb2_mm_txdat, usbb2_mm_txse0 and usbb2_mm_rxrcv transition		1.5		1.5	ns
FSU15	$t_{d(DATV-TXENH)}$	Delay time, usbb2_mm_txdat invalid before usbb2_mm_txen high	81.8		81.8		ns
FSU16	$t_{d(SE0V-TXENH)}$	Delay time, usbb2_mm_txse0 invalid before usbb2_mm_txen high	81.8		81.8		ns

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(1) See DM Operating Condition Addendum for CORE OPP voltages.
(2) Low-Speed mode is a subset of the Full-Speed mode and it is expected to work at low bandwidth (1.5Mb/s).

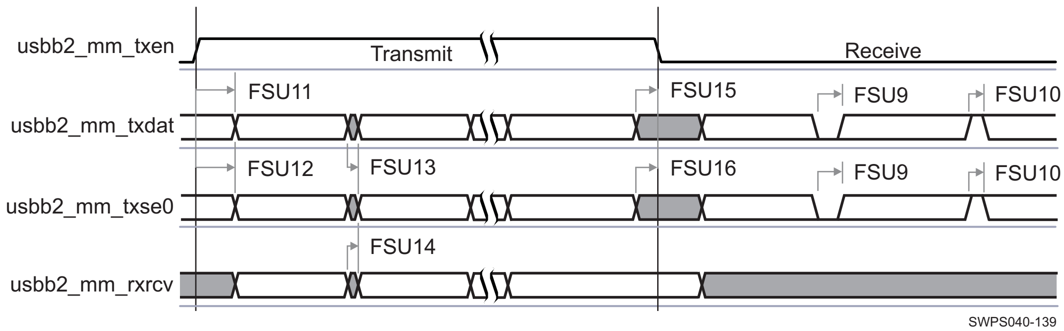

Figure 6-92. Low- / Full-Speed USBB2—Bidirectional TLL 4-pin Mode—1.8 V

6.6.8.4.3 Low- / Full-Speed USBB2 (FSUSB)—Bidirectional Standard 3-pin Mode

Table 6-158 and Table 6-159 assume testing over the recommended operating conditions and electrical characteristic conditions below (see Figure 6-93).

Table 6-157. Low- / Full-Speed USBB2 Timing Conditions—Bidirectional Standard 3-pin Mode—1.8 V(1)(2)(3)

TIMING CONDITION PARAMETER		VALUE		UNIT
		MIN	MAX	
Input Conditions				
t_R	Input signal rise time	2		ns
t_F	Input signal fall time	2		ns
PCB Conditions				
	Number of external peripherals		1	
	Far end load		10	pF
	Trace length		10	cm
	Characteristics impedance	30	60	Ω

(1) IO settings:
– usbb2_mm_txen (ball AE11): DS0 = 0
– usbb2_mm_txdat (ball AF11): DS0 = 0
– usbb2_mm_txse0 (ball AG11): DS0 = 0
For more information, see Control Module / Control Module Functional Description/ Functional Register Description / Signal Integrity Parameter Control Registers with Pad Group Assignment / I/O cells with Configurable Output Driver Impedance section of the OMAP4430 TRM.
– Corresponding voltage: 1.8 V

(2) In this table the rise and fall times are calculated for 10% to 90% of VDDS. For more information on the corresponding OMAP4 VDDS power supply name, see Table 2-1, POWER [9] column with the ball name.

(3) To have an idea of the output OMAP4 ball load supported for this application, you can consider the following:
Output OMAP4 ball load = Far End load + 1.34 pF/cm typical x trace length (cm).

Table 6-158. Low- / Full-Speed USBB2 Timing Requirements—Bidirectional Standard 3-pin Mode—1.8 V(1)(2)

NO.	PARAMETER		OPP100		OPP50		UNIT
			MIN	MAX	MIN	MAX	
FSU19	$t_{d(DAT,SE0)}$	Time duration, usbb2_mm_txdat and usbb2_mm_txse0 low together during transition		14.0		14.0	ns
FSU20	$t_{d(DAT,SE0)}$	Time duration, usbb2_mm_txdat and usbb2_mm_txse0 high together during transition		8.0		8.0	ns

PRODUCT PREVIEW

(1) See DM Operating Condition Addendum for CORE OPP voltages.

(2) Low-Speed mode is a subset of the Full-Speed mode and it is expected to work at low bandwidth (1.5Mb/s).

Table 6-159. Low- / Full-Speed USBB2 Switching Characteristics—Bidirectional Standard 3-pin Mode—1.8 V(1)(2)

NO.	PARAMETER		OPP100		OPP50		UNIT
			MIN	MAX	MIN	MAX	
FSU21	$t_{d(TXENL-DATV)}$	Delay time usbb2_mm_txen low to usbb2_mm_txdat valid	81.8	84.8	81.8	84.8	ns
FSU22	$t_{d(TXENL-SE0V)}$	Delay time usbb2_mm_txen low to usbb2_mm_txse0 valid	81.8	84.8	81.8	84.8	ns
FSU23	$t_{sk(DAT-SE0)}$	Skew between usbb2_mm_txdat and usbb2_mm_txse0 transition		1.5		1.5	ns
FSU24	$t_{d(DATV-TXENH)}$	Delay time, usbb2_mm_txdat invalid before usbb2_mm_txen high	81.8		81.8		ns
FSU25	$t_{d(SE0V-TXENH)}$	Delay time, usbb2_mm_txse0 invalid before usbb2_mm_txen high	81.8		81.8		ns

(1) See DM Operating Condition Addendum for CORE OPP voltages.

(2) Low-Speed mode is a subset of the Full-Speed mode and it is expected to work at low bandwidth (1.5Mb/s).

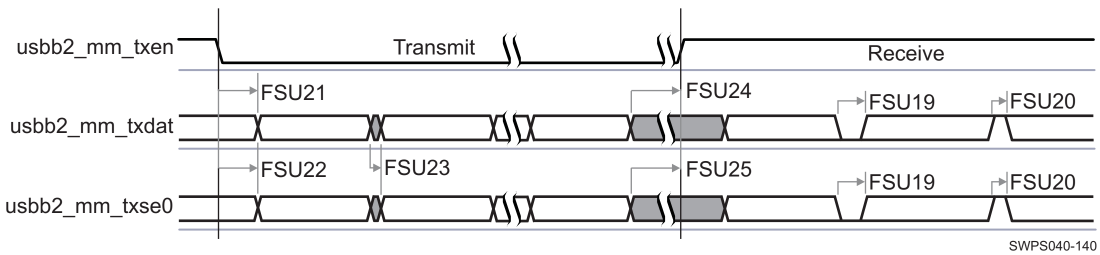

Figure 6-93. Low- / Full-Speed USBB2—Bidirectional Standard 3-pin Mode—1.8 V

6.6.8.4.4 Low- / Full-Speed USBB2 (FSUSB)—Bidirectional Standard 3-pin TLL Mode

Table 6-161 and Table 6-162 assume testing over the recommended operating conditions and electrical characteristic conditions below (see Figure 6-94).

Table 6-160. Low- / Full-Speed USBB2 Timing Conditions—Bidirectional TLL 3-pin Mode—1.8 V(1)(2)(3)

TIMING CONDITION PARAMETER		VALUE		UNIT
		MIN	MAX	
Input Conditions				
t_R	Input signal rise time	2		ns
t_F	Input signal fall time	2		ns
PCB Conditions				
	Number of external peripherals		1	
	Far end load		10	pF
	Trace length		10	cm
	Characteristics impedance	30	60	Ω

(1) IO settings:
- usbb2_mm_txen (ball AE11): DS0 = 0
- usbb2_mm_txdat (ball AF11): DS0 = 0
- usbb2_mm_txse0 (ball AG11): DS0 = 0
  For more information, see Control Module / Control Module Functional Description/ Functional Register Description / Signal Integrity Parameter Control Registers with Pad Group Assignment / I/O cells with Configurable Output Driver Impedance section of the OMAP4430 TRM.
- Corresponding voltage: 1.8 V

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(2) In this table the rise and fall times are calculated for 10% to 90% of VDDS. For more information on the corresponding OMAP4 VDDS power supply name, see Table 2-1, POWER [9] column with the ball name.

(3) To have an idea of the output OMAP4 ball load supported for this application, you can consider the following: Output OMAP4 ball load = Far End load + 1.34 pF/cm typical x trace length (cm).

Table 6-161. Low- / Full-Speed USBB2 Timing Requirements—Bidirectional TLL 3-pin Mode—1.8 V(1)(2)

NO.	PARAMETER		OPP100		OPP50		UNIT
			MIN	MAX	MIN	MAX	
FSU17	$t_{d(DAT,SE0)}$	Time duration, usbb2_mm_txdat and usbb2_mm_txse0 low together during transition		14.0		14.0	ns
FSU18	$t_{d(DAT,SE0)}$	Time duration, usbb2_mm_txdat and usbb2_mm_txse0 high together during transition		8.0		8.0	ns

(1) See DM Operating Condition Addendum for CORE OPP voltages.

(2) Low-Speed mode is a subset of the Full-Speed mode and it is expected to work at low bandwidth (1.5Mb/s).

Table 6-162. Low- / Full-Speed USBB2 Switching Characteristics—Bidirectional TLL 3-pin Mode—1.8 V(1)(2)

NO.	PARAMETER		OPP100		OPP50		UNIT
			MIN	MAX	MIN	MAX	
FSU19	$t_{d(TXENL-DATV)}$	Delay time usbb2_mm_txen low to usbb2_mm_txdat valid	81.8	84.8	81.8	84.8	ns
FSU20	$t_{d(TXENL-SE0V)}$	Delay time usbb2_mm_txen low to usbb2_mm_txse0 valid	81.8	84.8	81.8	84.8	ns
FSU21	$t_{sk(DAT-SE0)}$	Skew between usbb2_mm_txdat and usbb2_mm_txse0 transition		1.5		1.5	ns
FSU22	$t_{d(DATV-TXENH)}$	Delay time, usbb2_mm_txdat invalid before usbb2_mm_txen high	81.8		81.8		ns
FSU23	$t_{d(SE0V-TXENH)}$	Delay time, usbb2_mm_txse0 invalid before usbb2_mm_txen high	81.8		81.8		ns

(1) See DM Operating Condition Addendum for CORE OPP voltages.

(2) Low-Speed mode is a subset of the Full-Speed mode and it is expected to work at low bandwidth (1.5Mb/s).

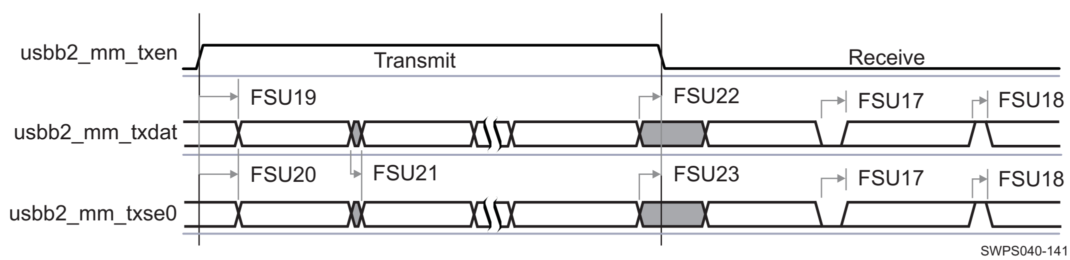

Figure 6-94. Low- / Full-Speed USBB2—Bidirectional TLL 3-pin Mode—1.8 V

6.6.8.4.5 Low- / Full-Speed USBB2 (FSUSB)—Bidirectional Standard 2-pin Mode

Table 6-164 assumes testing over the recommended operating conditions and electrical characteristic conditions below (see Figure 6-95).

Table 6-163. Low- / Full-Speed USBB2 Timing Conditions—Bidirectional 2-pin Mode—1.8 V(1)(2)(3)

TIMING CONDITION PARAMETER		VALUE		UNIT
		MIN	MAX	
Input Conditions				
t_R	Input signal rise time	2		ns
t_F	Input signal fall time	2		ns
PCB Conditions				
	Number of external peripherals		1	
	Far end load		10	pF
	Trace length		10	cm
	Characteristics impedance	30	60	Ω

(1) IO settings:
- Balls AD26, AD27 (usbb2_mm_rxdp, usbb2_mm_rxdm): MB[1:0] = 10 and LB0 = 1
  For more information, see Control Module / Control Module Functional Description/ Functional Register Description / Signal Integrity Parameter Control Registers with Pad Group Assignment / 50-Ω Output Buffer I/Os with Combined Mode and Load Settings section of the OMAP4430 TRM.
- Corresponding voltage: 1.8 V

(2) In this table the rise and fall times are calculated for 10% to 90% of VDDS. For more information on the corresponding OMAP4 VDDS power supply name, see Table 2-1, POWER [9] column with the ball name.

(3) To have an idea of the output OMAP4 ball load supported for this application, you can consider the following:
Output OMAP4 ball load = Far End load + 1.34 pF/cm typical x trace length (cm).

Table 6-164. Low- / Full-Speed USBB2 Timing Requirements—Bidirectional 2-pin Mode—1.8 V(1)(2)

NO.	PARAMETER		OPP100		OPP50		UNIT
			MIN	MAX	MIN	MAX	
FSU1	$t_{d(DAT,SE0)}$	Time duration, usbb2_mm_rxdp and usbb2_mm_rxdm low together during transition		14.0		14.0	ns
FSU2	$t_{d(DAT,SE0)}$	Time duration, usbb2_mm_rxdp and usbb2_mm_rxdm high together during transition		8.0		8.0	ns

(1) See DM Operating Condition Addendum for CORE OPP voltages.

(2) Low-Speed mode is a subset of the Full-Speed mode and it is expected to work at low bandwidth (1.5Mb/s).

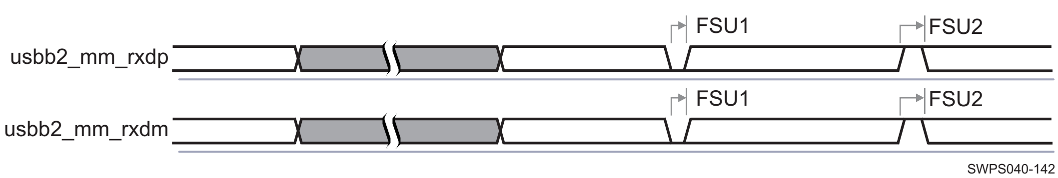

Figure 6-95. Low- / Full-Speed USBB2—Bidirectional 2-pin Mode—1.8 V

6.6.8.4.6 High-Speed USBB2 (HSUSB)—ULPI SDR Mode—Slave Mode

Table 6-166 and Table 6-167 assume testing over the recommended operating conditions and electrical characteristic conditions below (see Figure 6-96).

Table 6-165. High-Speed USBB2 Timing Conditions—ULPI SDR Mode(1)(2)(3)

SYSTEM CONDITION PARAMETER		VALUE		UNIT
		MIN	MAX	
Input Conditions				
t_R	Input signal rise time	1.00	3.00	ns
t_F	Input signal fall time	1.00	3.00	ns

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Table 6-165. High-Speed USBB2 Timing Conditions—ULPI SDR Mode[(1)(2)(3)] (continued)

SYSTEM CONDITION PARAMETER		VALUE		UNIT
		MIN	MAX	
PCB Conditions				
	Number of external peripherals		1	
	Far end load		5	pF
	Trace length		5	cm
	Characteristics impedance	30	60	Ω

(1) IO settings:

- usbb2_ulpiphy_clk (ball AG12): DS0 = 0
- usbb2_ulpiphy_stp (ball AF12): DS0 = 0
- usbb2_ulpiphy_dir (ball AE12): DS0 = 0
- usbb2_ulpiphy_nxt (ball AG13): DS0 = 0
- usbb2_ulpiphy_dat[7:0] (balls AE9 / AG10 / AF10 / AE10 / AH11 / AG11 / AF11 / AE11): DS0 = 0
  For more information, see Control Module / Control Module Functional Description/ Functional Register Description / Signal Integrity Parameter Control Registers with Pad Group Assignment / I/O cells with Configurable Output Driver Impedance section of the OMAP4430 TRM.
- Corresponding voltage: 1.8 V

(2) In this table the rise and fall times are calculated for 10% to 90% of VDDS. For more information on the corresponding OMAP4 VDDS power supply name, see Table 2-1, POWER [9] column with the ball name.

(3) To have an idea of the output OMAP4 ball load supported for this application, you can consider the following:
Output OMAP4 ball load = Far End load + 1.34 pF/cm typical x trace length (cm).

Table 6-166. High-Speed USBB2 Timing Requirements—ULPI SDR Mode—Slave Mode[(4)]

NO.	PARAMETER		OPP100		UNIT
			MIN	MAX	
US1	$1 / t_{c(clk)}$	Frequency[(1)], usbb2_ulpiphy_clk		60	MHz
US2	$t_{w(clkH)}$	Typical pulse duration, usbb2_ulpiphy_clk high	0.5*P[(2)]		ns
US3	$t_{w(clkL)}$	Typical pulse duration, usbb2_ulpiphy_clk low	0.5*P[(2)]		ns
	$t_{dc(clk)}$	Duty cycle error, usbb2_ulpiphy_clk	–833	833	ps
	$t_{j(clk)}$	Jitter standard deviation[(3)], usbb2_ulpiphy_clk		500	ps
US5	$t_{su(ctrlV-clkH)}$	Setup time, usbb2_ulpiphy_dir and usbb2_ulpiphy_nxt valid before usbb2_ulpiphy_clk rising edge	6.73		ns
US6	$t_{h(clkH-ctrlV)}$	Hold time, usbb2_ulpiphy_dir and usbb2_ulpiphy_nxt valid after usbb2_ulpiphy_clk rising edge	0.00		ns
US7	$t_{su(dV-clkH)}$	Setup time, input usbb2_ulpiphy_dat[7:0] valid before usbb2_ulpiphy_clk rising edge	6.73		ns
US8	$t_{h(clkH-dV)}$	Hold time, input usbb2_ulpiphy_dat[7:0] valid after usbb2_ulpiphy_clk rising edge	0.00		ns

(1) Related to the input maximum frequency supported by the USB module.

(2) P = clk period in ns

(3) Maximum cycle jitter supported by clk input clock.

(4) See DM Operating Condition Addendum for CORE OPP voltages.

Table 6-167. High-Speed USBB2 Switching Characteristics—ULPI SDR Mode—Slave Mode[(1)]

NO.	PARAMETER		OPP100		UNIT
			MIN	MAX	
US4	$t_{d(clkL-ctrlV)}$	Delay time, usbb2_ulpiphy_clk rising edge high to output usbb2_ulpiphy_stp valid	0.40	8.34	ns
	$t_{R(ctrl)}$	Rise time, output usbb2_ulpiphy_stp		3.0	ps
	$t_{F(dtrl)}$	Fall time, output usbb2_ulpiphy_stp		3.0	ps
US9	$t_{d(clkL-doV)}$	Delay time, usbb2_ulpiphy_clk rising edge to output usbb2_ulpiphy_dat[7:0] valid	0.40	8.34	ns
	$t_{R(do)}$	Rise time, output usbb2_ulpiphy_dat[7:0]		3.0	ps

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Table 6-167. High-Speed USBB2 Switching Characteristics—ULPI SDR Mode—Slave Mode[(1)] (continued)

NO.	PARAMETER		OPP100		UNIT
			MIN	MAX	
	$t_{F(do)}$	Fall time, output usbb2_ulpiphy_dat[7:0]		3.0	ps

(1) See DM Operating Condition Addendum for CORE OPP voltages.

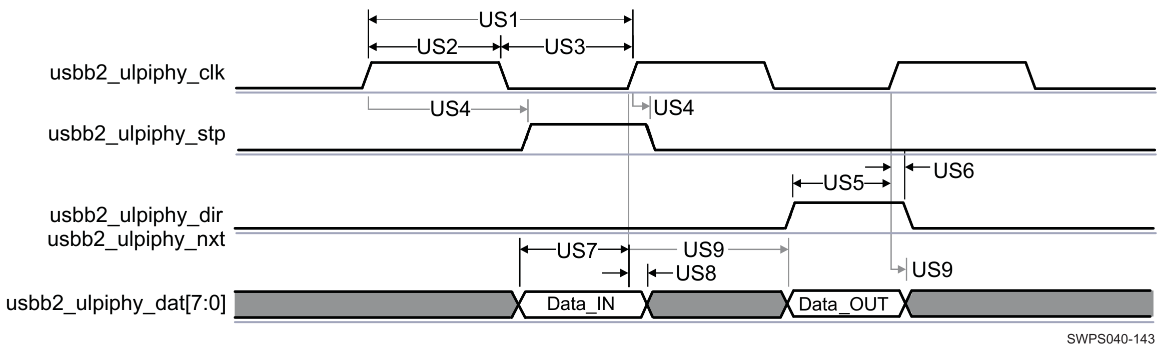

Figure 6-96. High-Speed USBB2—ULPI SDR Mode—Slave Mode

6.6.8.4.7 High-Speed USBB2 (HSUSB)—ULPI TLL Mode—Master Mode

Table 6-169 and Table 6-170 assume testing over the recommended operating conditions and electrical characteristic conditions below (see Figure 6-97).

Table 6-168. High-Speed USBB2 Timing Conditions—ULPI TLL Mode—Master Mode[(2)(3)]

SYSTEM CONDITION PARAMETER		VALUE		UNIT
		MIN	MAX	
Input Conditions				
t_R	Input signal rise time	1.00	3.00	ns
t_F	Input signal fall time	1.00	3.00	ns
PCB Conditions				
	Number of external peripherals		1	
	Far end load		5	pF
	Trace length		5	cm
	Characteristics impedance	30	60	Ω

(1) IO settings:
- usbb2_ulpitll_clk (ball AG12): DS0 = 0
- usbb2_ulpitll_stp (ball AF12): DS0 = 0
- usbb2_ulpitll_dir (ball AE12): DS0 = 0
- usbb2_ulpitll_nxt (ball AG13): DS0 = 0
- usbb2_ulpitll_dat[7:0] (balls AE9 / AG10 / AF10 / AE10 / AH11 / AG11 / AF11 / AE11): DS0 = 0
  For more information, see Control Module / Control Module Functional Description/ Functional Register Description / Signal Integrity Parameter Control Registers with Pad Group Assignment / I/O cells with Configurable Output Driver Impedance section of the OMAP4430 TRM.
- Corresponding voltage: 1.8 V

(2) In this table the rise and fall times are calculated for 10% to 90% of VDDS. For more information on the corresponding OMAP4 VDDS power supply name, see Table 2-1, POWER [9] column with the ball name.

(3) To have an idea of the output OMAP4 ball load supported for this application, you can consider the following:
Output OMAP4 ball load = Far End load + 1.34 pF/cm typical x trace length (cm).

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Table 6-169. High-Speed USBB2 Timing Requirements—ULPI TLL Mode—Master Mode[1]

NO.	PARAMETER		OPP100		OPP50		UNIT
			MIN	MAX	MIN	MAX	
UT4	$t_{su(ctrlV-clkH)}$	Setup time, usbb2_ulpitll_stp valid before usbb2_ulpitll_clk rising edge	5.78		5.78		ns
UT5	$t_{h(clkH-ctrlV)}$	Hold time, usbb2_ulpitll_stp valid after usbb2_ulpitll_clk rising edge	0.09		0.09		ns
UT6	$t_{su(dV-clkH)}$	Setup time, usbb2_ulpitll_dat[7:0] valid before usbb2_ulpitll_clk rising edge	5.78		5.78		ns
UT7	$t_{h(clkH-dV)}$	Hold time, usbb2_ulpitll_dat[7:0] valid after usbb2_ulpitll_clk rising edge	0.09		0.09		ns

(1) See DM Operating Condition Addendum for CORE OPP voltages.

Table 6-170. High-Speed USBB2 Switching Characteristics—ULPI TLL Mode—Master Mode[4]

NO.	PARAMETER		OPP100		OPP50		UNIT
			MIN	MAX	MIN	MAX	
UT1	$1 / t_{c(clk)}$	Frequency[1], output usbb2_ulpitll_clk		60		60	MHz
UT2	$t_{w(clkH)}$	Typical pulse duration, output usbb2_ulpitll_clk high	0.5*P[2]		0.5*P[2]		ns
UT3	$t_{w(clkL)}$	Typical pulse duration, output usbb2_ulpitll_clk low	0.5*P[2]		0.5*P[2]		ns
	$t_{dc(clk)}$	Duty cycle error, output usbb2_ulpitll_clk	–833	833	–833	833	ps
	$t_{j(clk)}$	Jitter standard deviation[3], output usbb2_ulpitll_clk		400		400	ps
	$t_{R(clk)}$	Rising time, output usbb2_ulpitll_clk		3.0		3.0	ps
	$t_{F(clk)}$	Falling time, output usbb2_ulpitll_clk		3.0		3.0	ps
UT8	$t_{d(clkL-ctrlV)}$	Delay time, output usbb2_ulpitll_clk rising edge to output usbb2_ulpitll_dir and usbb2_ulpitll_nxt	0.04	8.96	0.04	8.96	ns
	$t_{R(ctrl)}$	Rising time, output usbb2_ulpitll_dir and usbb2_ulpitll_nxt		3.0		3.0	ps
	$t_{F(dtrl)}$	Falling time, output usbb2_ulpitll_dir and usbb2_ulpitll_nxt		3.0		3.0	ps
UT9	$t_{d(clkL-doV)}$	Delay time, output usbb2_ulpitll_clk rising edge to output usbb2_ulpitll_dat[7:0] valid	0.04	8.96	0.04	8.96	ns
	$t_{R(do)}$	Rising time, output usbb2_ulpitll_dat[7:0]		3.0		3.0	ps
	$t_{F(do)}$	Falling time, output usbb2_ulpitll_dat[7:0]		3.0		3.0	ps

(1) Related to the input maximum frequency supported by the USB module.
(2) P = output clk period in ns
(3) The jitter probability density can be approximated by a Gaussian function.
(4) See DM Operating Condition Addendum for CORE OPP voltages.

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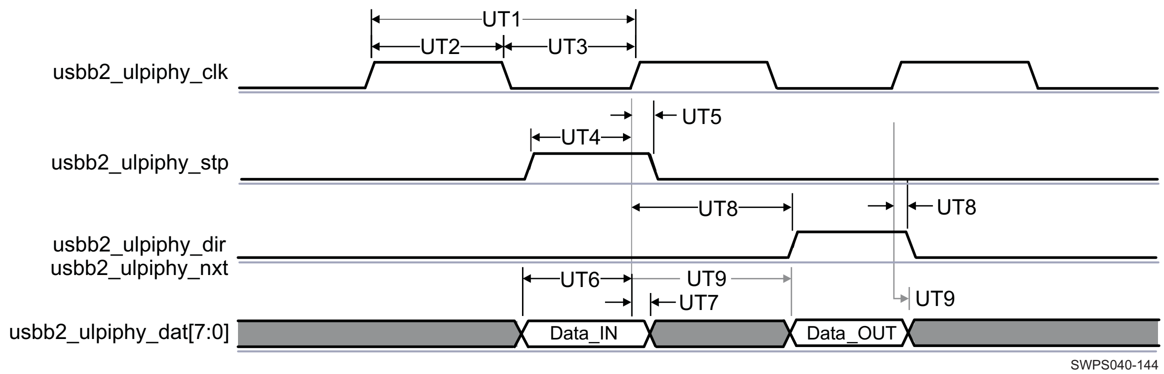

Figure 6-97. High-Speed USBB2—ULPI TLL Mode—Master Mode

6.6.8.4.8 High-Speed USBB2 (HSUSB)—High-Speed InterChip Interface 2 (HSIC2)

High-Speed InterChip (HSIC) is an alternative to the standard USB physical layer targeted at fixed, inter-chip communications. This implies short distances between devices, and allows for simpler, smaller, more power-efficient PHYs over a single-ended, 2-wire interface running at a fixed HS speed. HSIC should be identical to standard USB from a high-level application standpoint.

6.6.8.4.8.1 High-Speed USBB2—HSIC DDR Receive And Transmit Modes—1.2 V

Table 6-172 and Table 6-173 assume testing over the recommended operating conditions and electrical characteristic conditions below (see Figure 6-98).

Table 6-171. High-Speed USBB2—HSIC DDR Timing Conditions—1.2 V(1)(2)(3)

SYSTEM CONDITION PARAMETER		VALUE		UNIT
		MIN	MAX	
Input Conditions				
t_R	Input signal rise time	0.29	0.58	ns
t_F	Input signal fall time	0.29	0.58	ns
PCB Conditions				
	Number of external peripherals		1	
	Far end load		5	pF
	Trace length		4	cm
	Characteristics impedance	45	55	Ω

(1) IO settings:
- usbb2_hsic_data, usbb2_hsic_strobe (balls: AF13, AE13): sr[2:0] = 010 and i[2:0] = 110
  For more information, see Control Module / Control Module Functional Description / Functional Register Description / Signal Integrity Parameter Control Registers with Pad Group Assignment / High-speed I/O Buffers with Impedance, Slew Rate and Weak Driver Settings section of OMAP4430 TRM.
- Corresponding voltage: 1.2 V

(2) In this table the rise and fall times are calculated for 30% to 70% of VDDS. For more information on the corresponding OMAP4 VDDS power supply name, see Table 2-1, POWER [9] column with the ball name.

(3) To have an idea of the output OMAP4 ball load supported for this application, you can consider the following:
Output OMAP4 ball load = Far End load + 1.34 pF/cm typical x trace length (cm).

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Table 6-172. High-Speed USBB2 Timing Requirements—HSIC DDR Receive Mode—1.2 V(3)

NO.	PARAMETER		OPP100		UNIT
			MIN	MAX	
HSIC1	1 / $t_{c(clk)}$	Frequency(1), usbb2_hsic_strobe period		240	MHz
HSIC2	$t_{w(clkH)}$	Typical pulse duration, usbb2_hsic_strobe high	0.5*P(2)		ns
HSIC3	$t_{w(clkL)}$	Typical pulse duration, usbb2_hsic_strobe low	0.5*P(2)		ns
HSIC5	$t_{su(strobe-dataV)}$	Setup time, usbb2_hsic_data valid before usbb2_hsic_strobe low/high	0.271		ns
HSIC6	$t_{h(strobe-dataV)}$	Hold time, usbb2_hsic_data valid after usbb2_hsic_strobe low/high	0.271		ns

(1) Related to the maximum USB HSIC frequency.
(2) P = input clock period in ns
(3) See DM Operating Condition Addendum for CORE OPP voltages.

Table 6-173. High-Speed USBB2 Switching Characteristics—HSIC DDR Transmit Mode—1.2 V(3)

NO.	PARAMETER		OPP100		UNIT
			MIN	MAX	
HSIC1	1 / $t_{c(clk)}$	Frequency(1), usbb2_hsic_strobe period		240	MHz
HSIC2	$t_{w(clkH)}$	Typical pulse duration, usbb2_hsic_strobe high	0.5*P(2)		ns
HSIC3	$t_{w(clkL)}$	Typical pulse duration, usbb2_hsic_strobe low	0.5*P(2)		ns
	$t_{dc(clk)}$	Duty cycle error, usbb2_hsic_strobe	–83	83	ps
	$t_{R(clk)}$	Rise time, usbb2_hsic_strobe	0.39	0.56	ns
	$t_{F(clk)}$	Fall time, usbb2_hsic_strobe	0.39	0.56	ns
HSIC4	$t_{d(clk-dataV)}$	Delay time, usbb2_hsic_strobe low/high to usbb2_hsic_data valid	–0.325	0.325	ns
	$t_{R(do)}$	Rise time, output data usbb2_hsic_data	0.39	0.56	ns
	$t_{F(do)}$	Falli ime, output data usbb2_hsic_data	0.39	0.56	ns

(1) Related to the maximum USB HSIC frequency.
(2) P = output clock period in ns
(3) See DM Operating Condition Addendum for CORE OPP voltages.

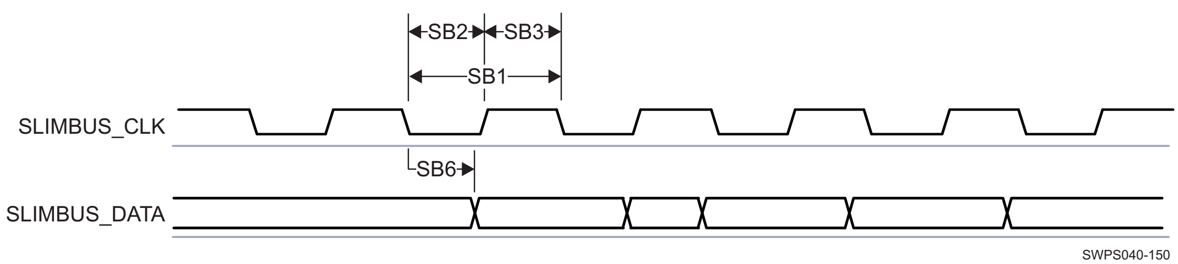

Figure 6-98. High-Speed USBB2—HSIC DDR Receive And Transmit Modes—1.2 V

6.6.9 *Inter-Integrated Circuit Interface (I^2C)*

NOTE

For more information, see the Serial Communication Interface / Multimaster High-Speed I^2C Controller / HS I^2C Functional Description section of the OMAP4430 TRM.

The multi-master I^2C peripheral provides an interface between two or more devices via an I^2C serial bus. The I^2C controller supports the multi-master mode which allows more than one device capable of controlling the bus to be connected to it. Each I^2C device is recognized by a unique address and can operates as either transmitter or receiver, according to the function of the device. In addition to being a transmitter or receiver, a device connected to the I^2C bus can also be considered as master or slave when performing data transfers. This data transfer is carried out via two serial bidirectional wires:

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- An SDA data line
- An SCL clock line

In Figure 6-99 and Figure 6-100 the data transfer is in master or slave configuration with 7-bit addressing format.

The I^2C and SmartReflex interfaces are compliant with Philips I^2C specification version 2.1. It supports standard mode (up to 100K bits/s), fast mode (up to 400K bits/s), and high-speed mode (up to 3.4Mb/s).

6.6.9.1 I^2C and SmartReflex—Standard and Fast Modes

NOTE

PCB conditions:

- Far End Load is less than 30 pF: for more information regarding LB1, LB0 Far End Load IO settings, see Control Module / Control Module Functional Description/ Functional Register Description / I2Cx I/Os Group Pullupresx Controls and Load Range Settings section of OMAP4430 TRM.
- Maximum trace length is less than 20 cm.
- Characteristic impedance is between 20 Ω to 70 Ω.

Table 6-174. I^2C and SmartReflex—Standard and Fast Modes[(6)]

NO.	PARAMETER		STANDARD MODE		FAST MODE		UNIT
			MIN	MAX	MIN	MAX	
	f_{scl}	Frequency, clock i2cx_scl[(4)]		100		400	kHz
I1	$t_{w(sclH)}$	Pulse duration, clock i2cx_scl[(4)] high	4.0		0.6		µs
I2	$t_{w(sclL)}$	Pulse duration, clock i2cx_scl[(4)] low	4.7		1.3		µs
I3	$t_{su(sdaV-sclH)}$	Setup time, data i2cx_sda[(4)] valid before clock i2cx_scl[(4)] active level	250		100[(1)]		ns
I4	$t_{h(sclH-sdaV)}$	Hold time, data i2cx_sda[(4)] valid after clock i2cx_scl[(4)] active level	0[(2)]	3.45[(3)]	0[(2)]	0.9[(3)]	µs
I5	$t_{su(sclH-sdaL)}$	Setup time, clock i2cx_scl[(4)] high before data i2cx_sda[(4)] low (for a START[(5)] condition or a repeated START condition)	4.7		0.6		µs
I6	$t_{h(sdaL-sclH)}$	Hold time, clock i2cx_scl[(4)] high after data i2cx_sda[(4)] low (for a START[(5)] condition or a repeated START condition)	4.0		0.6		µs
I7	$t_{su(sclH-sdaH)}$	Setup time, clock i2cx_scl[(4)] high before data i2cx_sda[(4)] high (for a STOP condition)	4.0		0.6		µs
I8	$t_{w(sdaH)}$	Pulse duration, data i2cx_sda[(4)] high between STOP and START conditions	4.7		1.3		µs
	$t_{R(scl)}$	Rise time, clock i2cx_scl[(4)]		1000	20 + $0.1C_B$	300	ns
	$t_{F(scl)}$	Fall time, clock i2cx_scl[(4)]		300	20 + $0.1C_B$	300	ns
	$t_{R(sda)}$	Rise time, data i2cx_sda[(4)]		1000	20 + $0.1C_B$	300	ns
	$t_{F(sda)}$	Fall time, data i2cx_sda[(4)]		300	20 + $0.1C_B$	300	ns
	C_B	Capacitive load for each bus line		400		400	pF

(1) A fast-mode I^2C-bus device can be used in a standard-mode I^2C-bus system, but the requirement $t_{su(SDAV-SCLH)} \geq 250$ ns must then be met. This is automatically the case if the device does not stretch the low period of the i2cx_scl[(4)]. If such a device does stretch the low period of the i2cx_scl[(4)], it must output the next data bit to the i2cx_sda[(4)] line $t_{R(SDA)}$ MAX + $t_{su(SDAV-SCLH)}$ = 1000 + 250 = 1250 ns (according to the standard-mode I^2C-bus specification) before the i2cx_scl[(4)] line is released.

(2) The device provides (via the I^2C bus) a minimum hold time (= I2C_FCLK period x (PSC+1) x 4) for the i2cx_sda[(4)] signal (refer to the fall and rise times of i2cx_scl[(4)]) to bridge the undefined region of the falling edge of i2cx_scl[(4)].
For more information, see the Serial Communication Interface / Multimaster High-Speed I^2C Controller / HS I^2C Functional Description /

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HS I²C Clocks section of the OMAP4430 TRM.

(3) The maximum $t_{h(SCLH\text{-}SDA)}$ has only to be met if the device does not stretch the low period of the i2cx_scl[(4)] signal.

(4) In i2cx, x is equal to 1, 2, 3, or 4 or sr for SmartReflex. Note that sr (SmartReflex) is master transmitter only.

(5) After this time, the first clock is generated.

(6) In this table the rise and fall times are calculated for 30% to 70% of VDDS. For more information on the corresponding OMAP4 VDDS power supply name, see Table 2-1, POWER [9] column with the ball name.

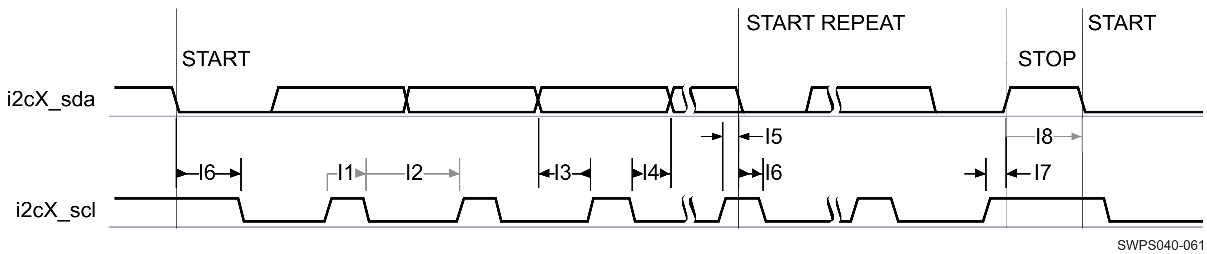

Figure 6-99. I²C and SmartReflex—Standard and Fast Modes[(1)]

(1) In i2cX, X is equal to 1, 2, 3 or 4, or sr for SmartReflex.

6.6.9.2 I²C and SmartReflex—High-Speed Mode

NOTE

PCB conditions:

- Far End Load is less than 30 pF: for more information regarding LB1, LB0 Far End Load IO settings, see Control Module / Control Module Functional Description/ Functional Register Description / I2Cx I/Os Group Pullupresx Controls and Load Range Settings section of OMAP4430 TRM.
- Maximum trace length is less than 20 cm.
- Characteristic impedance is between 20 Ω to 70 Ω.

Table 6-175. I²C and SmartReflex—High-Speed Mode[(6)]

NO.	PARAMETER		MIN	MAX	UNIT
	f_{scl}	Frequency, clock i2cx_scl[(3)]		3.4[(5)]	MHz
IH1	$t_{w(sclH)}$	Pulse duration, clock i2cx_scl[(3)] high	60[(1)]		ns
IH2	$t_{w(sclL)}$	Pulse duration, clock i2cx_scl[(3)] low	160[(1)]		ns
IH3	$t_{su(sdaV–sclH)}$	Setup time, data i2cx_sda[(3)] valid before clock i2cx_scl[(3)] active level	10		ns
IH4	$t_{h(sclH–sdaV)}$	Hold time, data i2cx_sda[(3)] valid after clock i2cx_scl[(3)] active level	0[(4)]	70	ns
IH5	$t_{su(sclH–sdaL)}$	Setup time, clock i2cx_scl[(3)] high before data i2cx_sda[(3)] low (for a START[(2)] condition or a repeated START condition)	160		ns
IH6	$t_{h(sdaL–sclH)}$	Hold time, clock i2cx_scl[(3)] high after data i2cx_sda[(3)] low (for a START[(2)] condition or a repeated START condition)	160		ns
IH7	$t_{su(sclH–sdaH)}$	Setup time, clock i2cx_scl[(3)] high before data i2cx_sda[(3)] high (for a STOP condition)	160		ns
	$t_{R(scl)}$	Rise time, clock i2cx_scl[(3)]	10	40	ns
	$t_{R(scl)}$	Rise time, clock i2cx_scl[(3)] after a repeated START condition and after a bit acknowledge	10	80	ns
	$t_{F(scl)}$	Fall time, clock i2cx_scl[(3)]	10	40	ns
	$t_{R(sda)}$	Rise time, data i2cx_sda[(3)]	10	80	ns
	$t_{F(sda)}$	Fall time, data i2cx_sda[(3)]	10	80	ns
	C_B	Capacitive load for each bus line		100	pF

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(1) HS-mode master devices generate a serial clock signal with a high to low ratio of 1 to 2. $t_{w(sclL)} > 2 * t_{w(sclH)}$.

(2) After this time, the first clock is generated.

(3) In i2cx, x is equal to 1, 2, 3, or 4 or sr for SmartReflex. Note that sr (SmartReflex) is master transmitter only.

(4) The device provides (via the I²C bus) a minimum hold time (= I2C_FCLK period x 4) for the i2cx_sda[(3)] signal (refer to the fall and rise times of i2cx_scl[(3)]) to bridge the undefined region of the falling edge of i2cx_scl[(3)].
For more information, see the Serial Communication Interface / Multimaster High-Speed I²C Controller / HS I²C Functional Description / HS I²C Clocks section of the OMAP4430 TRM.

(5) The maximum I2C5 (or SmartReflex) clock frequency in high-speed mode is equal to the SYS_CLK clock frequency (38.4 MHz maximum) divided by 18, with LB[1:0] = 01 setting on sr_scl, ball AG9 (load range = 12 pF to 25 pF and internal pullup resistance = 920 Ω). Therefore, the maximum I2C5 (or SmartReflex) clock frequency in high-speed mode is 2.13 MHz.
For more information about the I2C5 (or SmartReflex) timings constraints calculation and the corresponding I2C5 registers settings, see the Serial Communication Interface / Multimaster High-Speed I²C Controller / HS I²C Functional Description / HS I²C Clocks section of the OMAP4430 TRM.
For more information on the LB0[1:0] IO cell configuration, see the Control Module / Control Module Functional Description / Functional Register Description / Signal Integrity Parameter Control Registers With Pad Group Assignment section of the OMAP4430 TRM.

(6) In this table the rise and fall times are calculated for 30% to 70% of VDDS. For more information on the corresponding OMAP4 VDDS power supply name, see Table 2-1, POWER [9] column with the ball name.

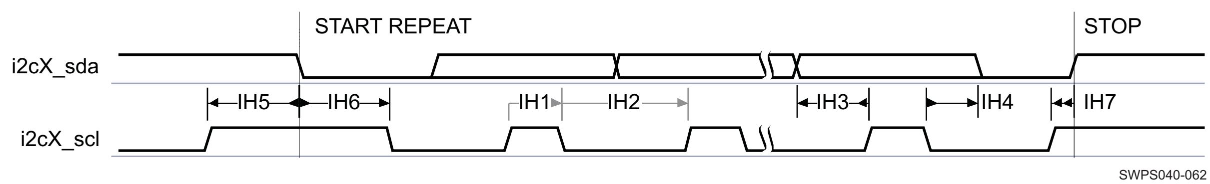

Figure 6-100. I²C and SmartReflex—High-Speed Mode[(1)]

(1) In i2cX, X is equal to 1, 2, 3 or 4, or sr for SmartReflex.

Table 6-176. I²C and SmartReflex Correspondence Standard vs Data Manual Timing References

TI-OMAP		STANDARD-I²C	
		Standard/Fast Modes	High-Speed Mode
	f_{scl}	F_{SCL}	F_{SCLH}
I1	$t_{w(sclH)}$	T_{HIGH}	T_{HIGH}
I2	$t_{w(sclL)}$	T_{LOW}	T_{LOW}
I3	$t_{su(sdaV-sclH)}$	$T_{SU;DAT}$	$T_{SU;DAT}$
I4	$t_{h(sclH-sdaV)}$	$T_{SU;DAT}$	$T_{SU;DAT}$
I5	$t_{su(sdaL-sclH)}$	$T_{SU;STA}$	$T_{SU;STA}$
I6	$t_{h(sclH-sdaH)}$	$T_{HD;STA}$	$T_{HD;STA}$
I7	$t_{h(sclH-RSTART)}$	$T_{SU;STO}$	$T_{SU;STO}$
I8	$t_{w(sdaH)}$	T_{BUF}	

6.6.10 HDQ / 1-Wire Interface (HDQ/1-Wire)

NOTE

For more information, see the Serial Communication Interface section of the OMAP4430 TRM.

The module is intended to work with both HDQ and 1-Wire protocols. The protocols use a single wire to communicate between the master and the slave. The protocols employ an asynchronous return to one mechanism where, after any command, the line is pulled high.

6.6.10.1 HDQ / 1-Wire—HDQ Mode

Table 6-177 through Table 6-179 assume testing over the recommended operating conditions and electrical characteristic conditions below (see Figure 6-101 through Figure 6-105).

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Table 6-177. HDQ/1-Wire Timing Requirements—HDQ Mode

PARAMETER	DESCRIPTION	MIN	TYP	MAX	UNIT
t_{CYCH}	Read bit window timing	190		250	µs
t_{HW1}	Read one data valid after HDQ low	32(2)		66(2)	
t_{HW0}	Read zero data hold after HDQ low	70(2)		145(2)	
t_{RSPS}	Response time from HDQ slave device(1)	190		320	

(1) Defined by software.

(2) If HDQ slave device drives a logic-low state after t_{HW0} maximum, it can be interpreted as a break pulse. For more information see Table 6-179 and the HDQ/1-Wire chapter of the OMAP4430 TRM.

Table 6-178. HDQ Sampling Cases(1)

CASES	FIRST SAMPLING (at 68 µs)	SECOND SAMPLING (at 180 µs)
1	L (logic-low state)	L (logic-low state)
2	L (logic-low state)	H (logic-high state)
3	H (logic-high state)	L (logic-low state)
4	H (logic-high state)	H (logic-high state)

(1) The different cases can be interpreted as follows:
- Case 1: If a logic-low state is present at the first sampling time and also at the second sampling time, the receive data can be interpreted as a break pulse.
- Case 2: If a logic-low state is present at the first sampling time and a logic-high state is present at the second sampling time, the receive data on the line is a zero (data).
- Case 3: Undefined.
- Case 4: If a logic-high state is present at the first sampling time and also at the second sampling time, the receive data on the line is a one (data).

Table 6-179. HDQ/1-Wire Switching Characteristics—HDQ Mode

PARAMETER	DESCRIPTION	MIN	TYP	MAX	UNIT
t_B	Break timing	190			µs
t_{BR}	Break recovery time	40			
t_{CYCD}	Write bit windows timing	190			
t_{DW1}	Write one data valid after HDQ low	0.5		50	
t_{DW0}	Write zero data hold after HDQ low	86		145	

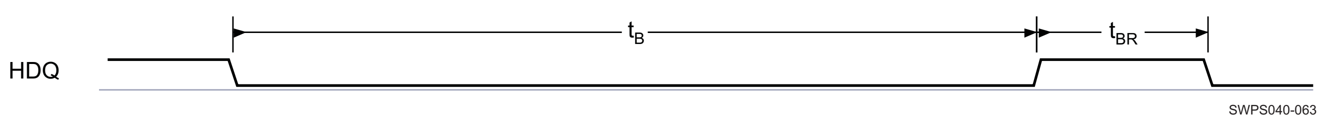

Figure 6-101. HDQ Break and Break Recovery Timing—OMAP HDQ Interface Writing to Slave

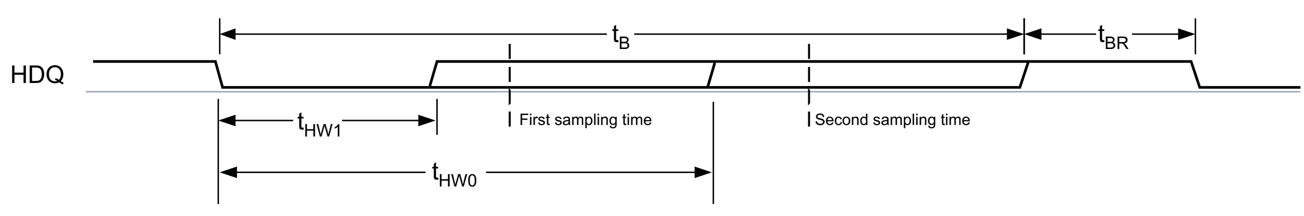

Figure 6-102. HDQ Break Detection—OMAP HDQ Interface Reading to Slave

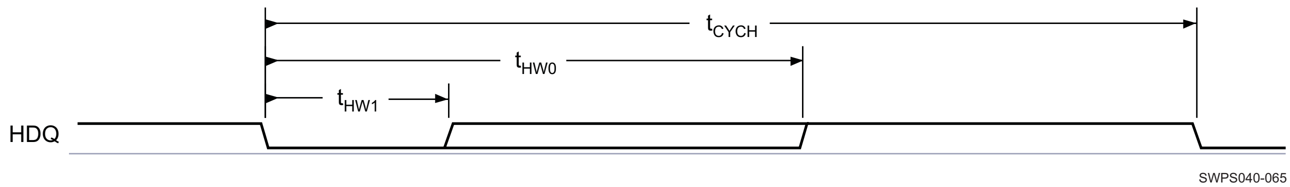

Figure 6-103. OMAP HDQ Interface Bit Read Timing (Data)

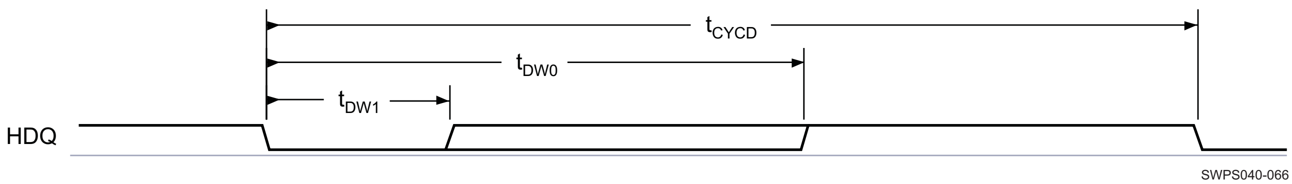

Figure 6-104. OMAP HDQ Interface Bit Write Timing (Command / Address or Data)

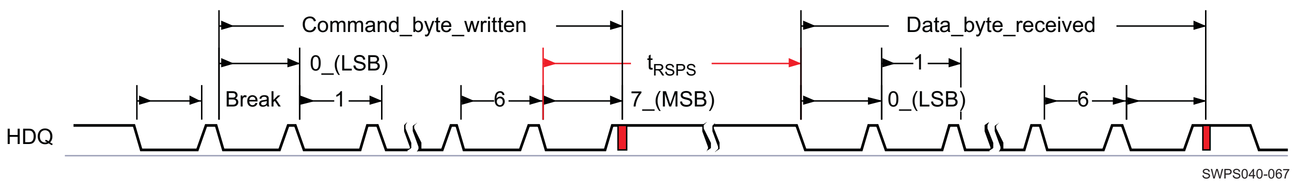

Figure 6-105. HDQ Communication Timing

6.6.10.2 HDQ/1-Wire—1-Wire Mode

Table 6-180 and Table 6-181 assume testing over the recommended operating conditions and electrical characteristic conditions below (see Figure 6-106 through Figure 6-109).

Table 6-180. HDQ/1-Wire Timing Requirements—1-Wire Mode

PARAMETER	DESCRIPTION	MIN	TYP	MAX	UNIT
t_{PDH}	Presence pulse delay high	15		60	µs
t_{PDL}	Presence pulse delay low	60		240	
t_{RDV}	Read data valid time	t_{LOWR}		15	
t_{REL}	Read data release time	0		45	

Table 6-181. HDQ/1-Wire Switching Characteristics—1-Wire Mode

PARAMETER	DESCRIPTION	MIN	TYP	MAX	UNIT
t_{RSTL}	Reset time low	480		960	µs
t_{RSTH}	Reset time high	480			µs
t_{SLOT}	Bit cycle time	60		120	µs
t_{LOW1}	Write bit-one time	1		15	µs
t_{LOW0}	Write bit-zero time(2)	60		120	µs
t_{REC}	Recovery time	1			µs
t_{LOWR}	Read bit strobe time(1)	1		15	µs

(1) t_{LOWR} (low pulse sent by the master) must be short as possible to maximize the master sampling window.

(2) t_{LOW0} must be less than t_{SLOT}.

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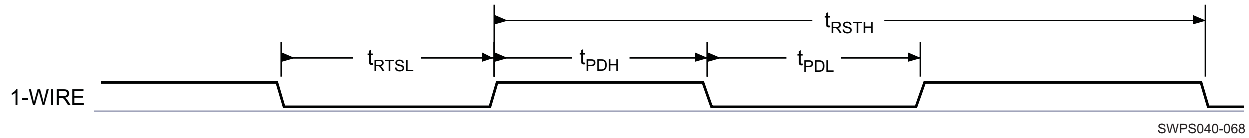

Figure 6-106. 1-Wire—Break (Reset)

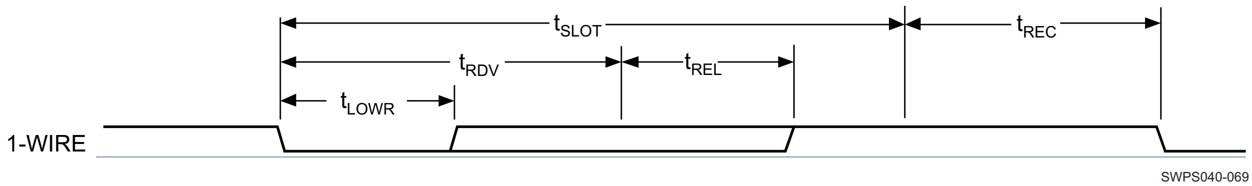

Figure 6-107. 1-Wire—Read Bit (Data)

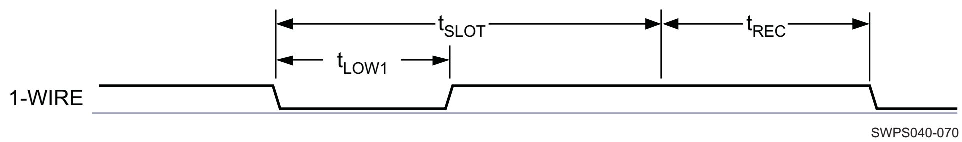

Figure 6-108. 1-Wire—Write Bit-One Timing (Command / Address or Data)

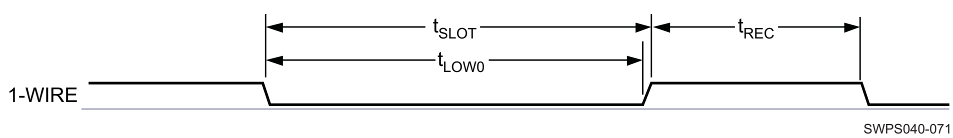

Figure 6-109. 1-Wire—Write Bit-Zero Timing (Command / Address or Data)

6.6.11 Universal Asynchronous Receiver Transmitter (UART)

NOTE

PCB conditions:

- Far End Load is less than 5 pF: for more information on the UART IO Settings, see Table 6-182.
- Maximum trace length is less than 10 cm.
- Characteristic impedance is between 20 Ω to 70 Ω.

Table 6-182. UART IO Settings References

MULTIPLEXING MODES	IO SETTINGS REFERENCES					
	IO SET 1	IO SET 2	IO SET 3	IO SET 4	IO SET 5	IO SET 6
UART1						
Mode1	Balls: C26 / D26 Signals: uart2_rx, uart1_tx For more information regarding LB[1:0] Far End Load IO settings, see Control Module / Control Module Functional Description/ Functional Register Description / I2Cx I/Os Group Pullupresx Controls and Load Range Settings section of OMAP4430 TRM.	Balls: AF23 / F27 Signals: uart1_rx, uart1_tx For more information regarding LB[1:0] and SC[1:0] Far End Load IO settings, see Control Module / Control Module Functional Description/ Functional Register Description / Low-Speed I/Os Combined Slew Rate Versus TL Length and Load Settings section of OMAP4430 TRM.	Balls: AG23 / AH23 Signals: uart1_cts, uart1_rts For more information regarding MB[1:0] and LB0 Far End Load IO settings, see Control Module / Control Module Functional Description/ Functional Register Description / 50-Ω Output Buffer I/Os With Combined Mode and Load Settings section of OMAP4430 TRM.			
Mode2				Ball: E3 Signal: uart1_rx For more information on SDMMC1_DR[2:0] _SPEEDCTRL registers see: Control Module / Control Module Functional Description / Functional Register Description / Signal Integrity Parameter Control Registers With Pad Group Assignment / Device Interfaces Signal Group Controls Mapping section or, Control Module / Control Module Register Manual / SYSCTRL_PADC ONF_CORE Register Description section of the OMAP4430 TRM.	Ball: AA3 Signal: uart1_rx For more information regarding DS0 Far End Load IO settings, see Control Module / Control Module Functional Description/ Functional Register Description / I/O Cells With Configurable Output Driver Impedance section of OMAP4430 TRM.	
UART2						

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Table 6-182. UART IO Settings References (continued)

MULTIPLEXING MODES	IO SETTINGS REFERENCES					
	IO SET 1	IO SET 2	IO SET 3	IO SET 4	IO SET 5	IO SET 6
Mode 0			Balls: AB26 / AB27 / AA25 / AA26 Signals: uart2_cts, uart2_rts, uart2_rx, uart2_tx For more information regarding MB[1:0] and LB0 Far End Load IO settings, see Control Module / Control Module Functional Description/ Functional Register Description / 50-Ω Output Buffer I/Os With Combined Mode and Load Settings section of OMAP4430 TRM.			
Mode 2						Balls: B5 / B4 Signals: uart2_rx, uart2_tx No IO settings needed.
UART3						
Mode 0		Balls: F27 / F28 / G27 / G28 Signals: uart3_cts_rctx, uart3_rts_sd, uart3_rx_irrx, uart3_tx_irtx For more information regarding LB[1:0] and SC[1:0] Far End Load IO settings, see Control Module / Control Module Functional Description/ Functional Register Description / Low-Speed I/Os Combined Slew Rate Versus TL Length and Load Settings section of OMAP4430 TRM.				
Mode 1						Balls: B5 / B4 Signals: uart3_rx_irrx, uart3_tx_irtx No IO settings needed.

Table 6-182. UART IO Settings References (continued)

MULTIPLEXING MODES	IO SETTINGS REFERENCES					
	IO SET 1	IO SET 2	IO SET 3	IO SET 4	IO SET 5	IO SET 6
Mode 2					Balls: W2 / W3 / W4 / Y2 uart3_tx_irtx, uart3_rx_irrx, uart3_rts_sd, uart3_cts_rctx For more information regarding DS0 Far End Load IO settings, see Control Module / Control Module Functional Description/ Functional Register Description / I/O Cells With Configurable Output Driver Impedance section of OMAP4430 TRM.	
UART4						
Mode 0			Balls: AG20 / AH19 uart4_rx, uart4_tx For more information regarding MB[1:0] and LB0 Far End Load IO settings, see Control Module / Control Module Functional Description/ Functional Register Description / 50-Ω Output Buffer I/Os With Combined Mode and Load Settings section of OMAP4430 TRM.			
Mode 5			Balls: AE24 / AF24 Signals: uart4_cts, uart4_rts For more information regarding MB[1:0] and LB0 Far End Load IO settings, see Control Module / Control Module Functional Description/ Functional Register Description / 50-Ω Output Buffer I/Os With Combined Mode and Load Settings section of OMAP4430 TRM.			

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Table 6-183. UART Switching Characteristics

SIGNAL NAME	MUX MODE	DESCRIPTION		MIN	MAX	UNIT
Universal Asynchronous Receiver/Transmitter (UART1)						
UART1 (uart1_tx): D26	1	t_{OT}[1]			10	ns
		C_L, Output load			40	pF
UART1 (uart1_tx): F27	1	t_{OT}[1]	SC[1:0] = 00	1	15	ns
		C_L, Output load		4	60	pF
		t_{OT}[1]	SC[1:0] = 01	0.4	5	ns
		C_L, Output load		2	21	pF
		t_{OT}[1]	SC[1:0] = 10	0.6	7	ns
		C_L, Output load		7	33	pF
UART1 (uart1_rts): AH23	1	t_{OT}[1][2]	MB[1:0] = 11 LB0 = 1 (Mode1) maximum frequency = 24 MHz transmission line delay = 670 ps		10	ns
		C_L, Output load[2]		20	25	pF
		t_{OT}[1][2]	MB[1:0] = 11 LB0 = 1 (Mode1) maximum frequency = 60 MHz transmission line delay = 335 ps		4	ns
		C_L, Output load[2]		2	5	pF
		t_{OT}[2]	MB[1:0] = 01 LB0 = 0 (Mode2) maximum frequency = 25 MHz transmission line delay = 335 ps		5.6[4]	ns
		C_L, Output load[2]		14	17	pF
		t_{OT}[1][2]	MB[1:0] = 01 LB0 = 0 (Mode2) maximum frequency = 48 MHz transmission line delay = 536 ps		6.3	ns
		C_L, Output load[2]		2	5	pF
		t_{OT}[2]	MB[1:0] = 10 LB0 = 1 (Mode3) maximum frequency = 20 MHz transmission line delay = 838 ps		10.5[4]	ns
		C_L, Output load[2]		23	28	pF
		t_{OT}[1][2]	MB[1:0] = 10 LB0 = 1 (Mode3) maximum frequency = 24 MHz transmission line delay = 670 ps		12.5	ns
		C_L, Output load[2]		16	20	pF
		t_{OT}[2]	MB[1:0] = 10 LB0 = 0 (Mode4) maximum frequency = 4 MHz transmission line delay = 1675 ps		16.8[4]	ns
		C_L, Output load[2]		16	20	pF
		t_{OT}[1][2]	MB[1:0] = 10 LB0 = 0 (Mode4) maximum frequency = 25 MHz transmission line delay = 670 ps		10	ns
		C_L, Output load[2]		2	5	pF
		t_{OT}[1][2]	MB[1:0] = 10 LB0 = 0 (Mode4) maximum frequency = 25 MHz transmission line delay = 670 ps		12.2	ns
		C_L, Output load[2]		5	7	pF
		t_{OT}[2]	MB[1:0] = 10 LB0 = 0 (Mode4) maximum frequency = 25 MHz transmission line delay = 536 ps		8[4]	ns
		C_L, Output load[2]		2	11	pF
Universal Asynchronous Receiver/Transmitter (UART2)						

Table 6-183. UART Switching Characteristics (continued)

SIGNAL NAME	MUX MODE	DESCRIPTION		MIN	MAX	UNIT
UART2 (uart2_rts, uart2_tx): AB27 / AA26	0	t_{OT}(1)(2)	MB[1:0] = 11 LB0 = 1 (Mode1) maximum frequency = 24 MHz transmission line delay = 670 ps		10	ns
		C_L, Output load		20	25	pF
		t_{OT}(1)(2)	MB[1:0] = 11 LB0 = 1 (Mode1) maximum frequency = 60 MHz transmission line delay = 335 ps		4	ns
		C_L, Output load		2	5	pF
		t_{OT}(2)	MB[1:0] = 01 LB0 = 0 (Mode2) maximum frequency = 25 MHz transmission line delay = 335 ps		5.6(4)	ns
		C_L, Output load		14	17	pF
		t_{OT}(1)(2)	MB[1:0] = 01 LB0 = 0 (Mode2) maximum frequency = 48 MHz transmission line delay = 536 ps		6.3	ns
		C_L, Output load		2	5	pF
		t_{OT}(2)	MB[1:0] = 10 LB0 = 1 (Mode3) maximum frequency = 20 MHz transmission line delay = 838 ps		10.5(4)	ns
		C_L, Output load		23	28	pF
		t_{OT}(1)(2)	MB[1:0] = 10 LB0 = 1 (Mode3) maximum frequency = 24 MHz transmission line delay = 670 ps		12.5	ns
		C_L, Output load		16	20	pF
		t_{OT}(2)	MB[1:0] = 10 LB0 = 0 (Mode4) maximum frequency = 4 MHz transmission line delay = 1675 ps		16.8(4)	ns
		C_L, Output load		16	20	pF
		t_{OT}(1)(2)	MB[1:0] = 10 LB0 = 0 (Mode4) maximum frequency = 25 MHz transmission line delay = 670 ps		10	ns
		C_L, Output load		2	5	pF
		t_{OT}(1)(2)	MB[1:0] = 10 LB0 = 0 (Mode4) maximum frequency = 25 MHz transmission line delay = 670 ps		12.2	ns
		C_L, Output load		5	7	pF
		t_{OT}(2)	MB[1:0] = 10 LB0 = 0 (Mode4) maximum frequency = 25 MHz transmission line delay = 536 ps		8(4)	ns
		C_L, Output load		2	11	pF
UART2 (uart2_rx, uart2_tx): B5 / B4	2	t_{OT}(1)		4	30	ns
		C_L, Output load		0	50	pF
Universal Asynchronous Receiver/Transmitter (UART3)						
UART3 (uart3_cts_rctx, uart3_rts_sd, uart3_tx_irtx): F27 / F28 / G28	0	t_{OT}(1)	SC[1:0] = 00	1	15	ns
		C_L, Output load		4	60	pF
		t_{OT}(1)	SC[1:0] = 01	0.4	5	ns
		C_L, Output load		2	21	pF
		t_{OT}(1)	SC[1:0] = 10	0.6	7	ns
		C_L, Output load		7	33	pF
UART3 (uart3_rx_irrx, uart3_tx_irtx): B5 / B4	1	t_{OT}(1)		4	30	ns
		C_L, Output load		0	50	pF
UART3 (uart3_tx_irtx, uart3_rts_sd, uart3_cts_rctx): W2 / W4 / Y2	2	t_{OT}	DS0 = 0 (Mode2) maximum frequency = 20 MHz transmission line delay = 1340 ps		15(3)	ns
		C_L, Output load		5	35	pF
		t_{OT}	DS0 = 0 (Mode2) maximum frequency = 48 MHz transmission line delay = 670 ps		3(3)	ns
		C_L, Output load		2	5	pF
		t_{OT}	DS0 = 0 (Mode2) maximum frequency = 60 MHz transmission line delay = 335 ps		3(4)	ns
		C_L, Output load		2	5	pF
		t_{OT}	DS0 = 0 (Mode2) maximum frequency = 75 MHz transmission line delay = 402 ps		4(1)	ns
		C_L, Output load		2	5	pF
		t_{OT}	DS0 = 1 (Mode1) maximum frequency = 100 MHz transmission line delay = 203 ps		2(1)	ns
		C_L, Output load		2	5	pF
Universal Asynchronous Receiver/Transmitter (UART4)						

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Table 6-183. UART Switching Characteristics (continued)

SIGNAL NAME	MUX MODE	DESCRIPTION		MIN	MAX	UNIT
UART4 (uart4_tx): AH19	0	t_{OT} [1][2]	MB[1:0] = 11 LB0 = 1 (Mode1) maximum frequency = 24 MHz transmission line delay = 670 ps		10	ns
		C_L, Output load		20	25	pF
		t_{OT} [2]	MB[1:0] = 11 LB0 = 1 (Mode1) maximum frequency = 60 MHz transmission line delay = 335 ps		4	ns
		C_L, Output load		2	5	pF
		t_{OT} [2]	MB[1:0] = 01 LB0 = 0 (Mode2) maximum frequency = 25 MHz transmission line delay = 335 ps		5.6[4]	ns
		C_L, Output load		14	17	pF
		t_{OT} [2]	MB[1:0] = 01 LB0 = 0 (Mode2) maximum frequency = 48 MHz transmission line delay = 536 ps		6.3	ns
		C_L, Output load		2	5	pF
		t_{OT} [2]	MB[1:0] = 10 LB0 = 1 (Mode3) maximum frequency = 20 MHz transmission line delay = 838 ps		10.5[4]	ns
		C_L, Output load		23	28	pF
		t_{OT} [2]	MB[1:0] = 10 LB0 = 1 (Mode3) maximum frequency = 24 MHz transmission line delay = 670 ps		12.5	ns
		C_L, Output load		16	20	pF
		t_{OT} [2]	MB[1:0] = 10 LB0 = 0 (Mode4) maximum frequency = 4 MHz transmission line delay = 1675 ps		16.8[4]	ns
		C_L, Output load		16	20	pF
		t_{OT} [2]	MB[1:0] = 10 LB0 = 0 (Mode4) maximum frequency = 25 MHz transmission line delay = 670 ps		10	ns
		C_L, Output load		2	5	pF
		t_{OT} [2]	MB[1:0] = 10 LB0 = 0 (Mode4) maximum frequency = 25 MHz transmission line delay = 670 ps		12.2	ns
		C_L, Output load		5	7	pF
		t_{OT} [2]	MB[1:0] = 10 LB0 = 0 (Mode4) maximum frequency = 25 MHz transmission line delay = 536 ps		8[4]	ns
		C_L, Output load		2	11	pF
UART4 (uart4_cts, uart4_rts): AE24 / AF24	5	t_{OT} [1][2]	MB[1:0] = 11 LB0 = 1 (Mode1) maximum frequency = 24 MHz transmission line delay = 670 ps		10	ns
		C_L, Output load[2]		20	25	pF
		t_{OT} [1][2]	MB[1:0] = 11 LB0 = 1 (Mode1) maximum frequency = 60 MHz transmission line delay = 335 ps		4	ns
		C_L, Output load[2]		2	5	pF
		t_{OT} [2]	MB[1:0] = 01 LB0 = 0 (Mode2) maximum frequency = 25 MHz transmission line delay = 335 ps		5.6[4]	ns
		C_L, Output load[2]		14	17	pF
		t_{OT} [1][2]	MB[1:0] = 01 LB0 = 0 (Mode2) maximum frequency = 48 MHz transmission line delay = 536 ps		6.3	ns
		C_L, Output load[2]		2	5	pF
		t_{OT} [2]	MB[1:0] = 10 LB0 = 1 (Mode3) maximum frequency = 20 MHz transmission line delay = 838 ps		10.5[4]	ns
		C_L, Output load[2]		23	28	pF
		t_{OT} [1][2]	MB[1:0] = 10 LB0 = 1 (Mode3) maximum frequency = 24 MHz transmission line delay = 670 ps		12.5	ns
		C_L, Output load[2]		16	20	pF
		t_{OT} [2]	MB[1:0] = 10 LB0 = 0 (Mode4) maximum frequency = 4 MHz transmission line delay = 1675 ps		16.8[4]	ns
		C_L, Output load[2]		16	20	pF
		t_{OT} [1][2]	MB[1:0] = 10 LB0 = 0 (Mode4) maximum frequency = 25 MHz transmission line delay = 670 ps		10	ns
		C_L, Output load[2]		2	5	pF
		t_{OT} [1][2]	MB[1:0] = 10 LB0 = 0 (Mode4) maximum frequency = 25 MHz transmission line delay = 670 ps		12.2	ns
		C_L, Output load[2]		5	7	pF
		t_{OT} [2]	MB[1:0] = 10 LB0 = 0 (Mode4) maximum frequency = 25 MHz transmission line delay = 536 ps		8[4]	ns
		C_L, Output load[2]		2	11	pF

(1) Output transition time measured between 10% to 90% of PAD voltage
(2) Depending on the programming mode, different output load and transition time are available following the targeted maximum frequency, transmission line or output transition time.
(3) Output transition time measured between 20% to 70% of PAD voltage.
(4) Output transition time measured between 20% to 80% of PAD voltage.

6.6.11.1 UART3 IrDA

NOTE

For more information, see the Serial Communication Interface section of the OMAP4430 TRM.

The IrDA module can operate in three different modes:

- Slow infrared (SIR) (≤ 115.2 Kbits/s)
- Medium infrared (MIR) (0.576 Mbits/s and 1.152 Mbits/s)
- Fast infrared (FIR) (4 Mbits/s)

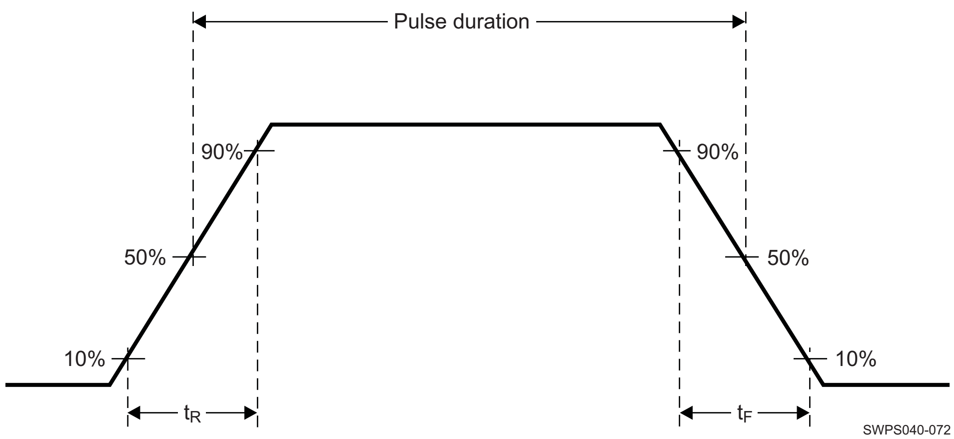

Figure 6-110. UART IrDA Pulse Parameters

6.6.11.1.1 UART3 IrDA—Receive Mode

Table 6-184. UART3 IrDA Signaling Rate and Pulse Duration with 3/16th Encoding—Receive Mode

SIGNALING RATE	ELECTRICAL PULSE DURATION			UNIT
	MIN	TYP	MAX	
SIR				
2.4 Kbit/s	52.17	78.13	208.33	μs
9.6 Kbit/s	13.10	19.53	52.08	μs
19.2 Kbit/s	6.59	9.77	26.04	μs
38.4 Kbit/s	3.34	4.88	13.02	μs
57.6 Kbit/s	2.25	3.26	8.68	μs
115.2 Kbit/s	1.17	1.63	4.34	μs
MIR				
0.576 Mbit/s	300.55	416.67	867.86	ns
1.152 Mbit/s	192.04	208.33	433.83	ns
FIR				
4.0 Mbit/s (Single pulse)	62.70	125.00	170.63	ns
4.0 Mbit/s (Double pulse)	208.53	250.00	291.47	ns

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NOTE

In SIR receive mode, both the 3/16th and the 1.6-µs pulse duration methods are supported. For more information, see the Serial Communication Interface / UART/IrDA/CIR section of the OMAP4430 TRM.

Table 6-185. UART3 IrDA Rise and Fall Times—Receive Mode

PARAMETER		MIN	TYP	MAX	UNIT
t_R	Rise time, input data uart3_rx_irrx			200	ns
t_F	Fall time, input data uart3_rx_irrx			200	ns

6.6.11.1.2 UART3 IrDA—Transmit Mode

Table 6-186. UART3 IrDA Signaling Rate and Pulse Duration with 3/16th Encoding—Transmit Mode

SIGNALING RATE	ELECTRICAL PULSE DURATION			UNIT
	MIN	TYP	MAX	
SIR				
2.4 Kbit/s	78.1	78.1	78.1	µs
9.6 Kbit/s	19.5	19.5	19.5	µs
19.2 Kbit/s	9.75	9.75	9.75	µs
38.4 Kbit/s	4.87	4.87	4.87	µs
57.6 Kbit/s	3.25	3.25	3.25	µs
115.2 Kbit/s	1.62	1.62	1.62	µs
MIR				
0.576 Mbit/s	414	416	419	ns
1.152 Mbit/s	206	208	211	ns
FIR				
4.0 Mbit/s (Single pulse)	123	125	128	ns
4.0 Mbit/s (Double pulse)	248	250	253	ns

NOTE

In SIR transmit mode, both the 3/16th and the 1.6-µs pulse duration methods are supported. For more information, see the Serial Communication Interface / UART/IrDA/CIR section of the OMAP4430 TRM.

6.7 Removable Media Interfaces

NOTE

For more information, see the MMC/SD/SDIO section of the OMAP4430 TRM.

The MMC/SD/SDIO host controller provides an interface to MMC, SD memory cards or SDIO cards. The MMC/SD/SDIO host controller deals with MMC/SD/SDIO protocol at transmission level, data packing, adding cyclic redundancy checks (CRC), start/end bit, and checking for syntactical correctness.

There are five MMC/SD/SDIO host controllers inside the device:

- MMC/SD/SDIO1:
  - 1.8-V / 3-V support
  - 1-bit, 4-bit, and 8-bit data transfers without external transceiver
- MMC/SD/SDIO2:
  - Only 1.8-V support
  - 1-bit, 4-bit, and 8-bit data transfers without external transceiver
  - 8-bit with external transceiver allowing supporting 3-V peripherals
- MMC/SD/SDIO3, MMC/SD/SDIO4, and MMC/SD/SDIO5:
  - Only 1.8-V support
  - 1-bit and 4-bit data transfers without external transceiver

6.7.1 Multimedia Memory Card and Secure Digital IO Card (SDMMC)

6.7.1.1 MMC/SD/SDIO 1 Interface

6.7.1.1.1 MMC/SD/SDIO 1 Interface—SD Identification and Standard SD Mode

Table 6-188 and Table 6-189 assume testing over the recommended operating conditions and electrical characteristic conditions below (see Figure 6-111 and Figure 6-112).

Table 6-187. MMC/SD/SDIO 1 Interface Timing Conditions—SD Identification and Standard SD Mode(1)(2)(3)(4)

TIMING CONDITION PARAMETER			VALUE		UNIT
			MIN	MAX	
Input Conditions					
t_R	Input signal rise time		10		ns
t_F	Input signal fall time		10		ns
PCB Conditions					
	Number of external peripherals			1	
	Far end load			40	pF
	Trace length for SD car types			10	cm
	Characteristics impedance	SanDisk Extreme III cards	45	55	Ω
		Other card types	20	70	

(1) IO settings: SPEEDCTRL = 0
For more information, see
– The Control Module Functional Description / Extended-Drain I/O and PBIAS Cell / Extended-Drain I/O section or
– The Control Module / Control Module Functional Description / Functional Register Description / Signal Integrity Parameter Control Registers with Pad Group Assignment / Device Interfaces Signal Group Controls Mapping section
of the OMAP4430 TRM.

(2) In this table the rise and fall times are calculated for the V_{IL} / V_{IH} described in Section 3.3.11, *MMC/SDIO DC Electrical Characteristics*.

(3) For more information on SDMMC ESD guideline examples, see Section A.3.2.2.1, *ESD Implementation—MMC/SD/SDIO 1 Interface—SD Mode.*

(4) To have an idea of the output OMAP4 ball load supported for this application, you can consider the following:

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Output OMAP4 ball load = Far End load + 1.34 pF/cm typical x trace length (cm).

Table 6-188. MMC/SD/SDIO 1 Interface Timing Requirements—SD Identification and Standard SD Mode[(1)(2)]

NO.	PARAMETER		OPP100		OPP50		UNIT
			MIN	MAX	MIN	MAX	
SD Identification Mode							
SD3	$t_{su(CMDV-CLKH)}$	Setup time, sdmmc1_cmd valid before sdmmc1_clk rising clock edge	1198.2		1198.2		ns
SD4	$t_{h(clkH-CMDIV)}$	Hold time, sdmmc1_cmd valid after sdmmc1_clk rising clock edge	1249.0		1249.0		ns
MMC/SD/SDIO 1 Interface (1.8-V IO) Standard SD Mode							
SD3	$t_{su(CMDV-CLKH)}$	Setup time, sdmmc1_cmd valid before sdmmc1_clk rising clock edge	6.0		6.0		ns
SD4	$t_{h(clkH-CMDIV)}$	Hold time, sdmmc1_cmd valid after sdmmc1_clk rising clock edge	19.2		19.2		ns
SD7	$t_{su(datV-CLKH)}$	Setup time, sdmmc1_dat[n:0] valid before sdmmc1_clk rising clock edge	6.0		6.0		ns
SD8	$t_{h(clkH-datIV)}$	Hold time, sdmmc1_dat[n:0] valid after sdmmc1_clk rising clock edge	19.2		19.2		ns
MMC/SD/SDIO 1 Interface (3.3-V IO) Standard SD Mode							
SD3	$t_{su(CMDV-CLKH)}$	Setup time, sdmmc1_cmd valid before sdmmc1_clk rising clock edge	6.0		6.0		ns
SD4	$t_{h(clkH-CMDIV)}$	Hold time, sdmmc1_cmd valid after sdmmc1_clk rising clock edge	19.2		19.2		ns
SD7	$t_{su(datV-CLKH)}$	Setup time, sdmmc1_dat[n:0] valid before sdmmc1_clk rising clock edge	6.0		6.0		ns
SD8	$t_{h(clkH-datIV)}$	Hold time, sdmmc1_dat[n:0] valid after sdmmc1_clk rising clock edge	19.2		19.2		ns

(1) In sdmmc1_dat[n:0], n up to 7

(2) See DM Operating Condition Addendum for CORE OPP voltages.

Table 6-189. MMC/SD/SDIO 1 Interface Switching Characteristics—SD Identification and Standard SD Mode[(1)(3)(4)]

NO.	PARAMETER		OPP100		OPP50		UNIT
			MIN	MAX	MIN	MAX	
SD Identification Mode							
SD1	$1 / t_{clk}$	Frequency, sdmmc1_clk		0.4		0.4	MHz
SD2	$t_{w(clk)}$	Pulse duration, sdmmc1_clk high or low	0.45*P[(2)]	0.55*P[(2)]	0.45*P[(2)]	0.55*P[(2)]	ns
SD5	$t_{d(clkH-CMDT)}$	Delay time, sdmmc1_clk rising clock edge to sdmmc1_cmd transition	6.5	2492.5	6.5	2492.5	ns
MMC/SD/SDIO 1 Interface (1.8-V IO) Standard SD Mode							
SD1	$1 / t_{clk}$	Frequency, sdmmc1_clk		24		24	MHz
SD2	$t_{w(clk)}$	Pulse duration, sdmmc1_clk high or low	0.45*P[(2)]	0.55*P[(2)]	0.45*P[(2)]	0.55*P[(2)]	ns
SD5	$t_{d(clkH-CMD)}$	Delay time, sdmmc1_clk rising clock edge to sdmmc1_cmd transition	6.3	35.3	6.3	35.3	ns
SD6	$t_{d(clkH-dat)}$	Delay time, sdmmc1_clk rising clock edge to sdmmc1_dat[n:0] transition	6.3	35.3	6.3	35.3	ns
MMC/SD/SDIO 1 Interface (3.3-V IO) Standard SD Mode							
SD1	$1 / t_{clk}$	Frequency, sdmmc1_clk		24		24	MHz
SD2	$t_{w(clk)}$	Pulse duration, sdmmc1_clk high or low	0.45*P[(2)]	0.55*P[(2)]	0.45*P[(2)]	0.55*P[(2)]	ns
SD5	$t_{d(clkH-CMD)}$	Delay time, sdmmc1_clk rising clock edge to sdmmc1_cmd transition	6.3	35.3	6.3	35.3	ns

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Table 6-189. MMC/SD/SDIO 1 Interface Switching Characteristics—SD Identification and Standard SD Mode(1)(3)(4) (continued)

NO.	PARAMETER		OPP100		OPP50		UNIT
			MIN	MAX	MIN	MAX	
SD6	$t_{d(clkH-dat)}$	Delay time, sdmmc1_clk rising clock edge to sdmmc1_dat[n:0] transition	6.3	35.3	6.3	35.3	ns

(1) Related to the output sdmmc1_clk maximum and minimum frequency.

(2) P = output sdmmc1_clk period in ns

(3) In sdmmc1_dat[n:0], n up to 7

(4) See DM Operating Condition Addendum for CORE OPP voltages.

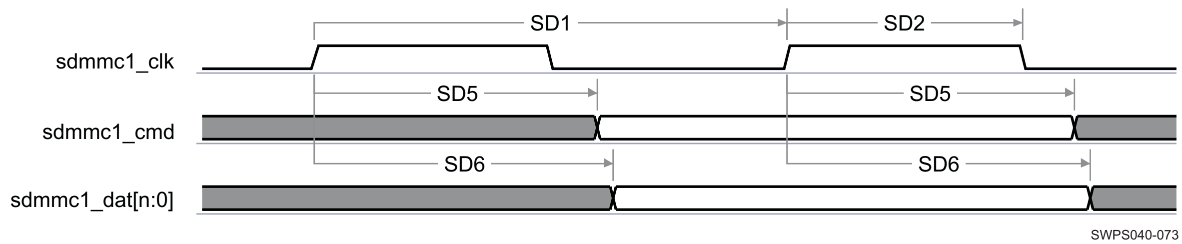

Figure 6-111. MMC/SD/SDIO 1 Interface—SD Identification and Standard SD—Transmitter Mode(1)

(1) In sdmmc1_dat[n:0], n up to 7

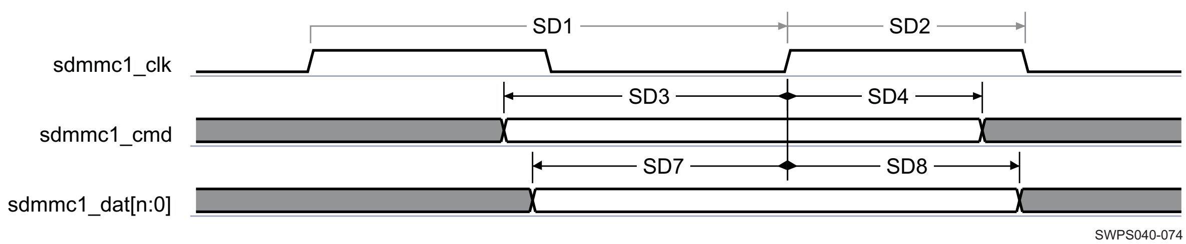

Figure 6-112. MMC/SD/SDIO 1 Interface—SD Identification and Standard SD—Receiver Mode(1)

(1) In sdmmc1_dat[n:0], n up to 7

6.7.1.1.2 MMC/SD/SDIO 1 Interface—High-Speed SD Mode

Table 6-191 and Table 6-192 assume testing over the recommended operating conditions and electrical characteristic conditions below (see Figure 6-113 and Figure 6-114).

Table 6-190. MMC/SD/SDIO 1 Interface Timing Conditions—High-Speed SD Mode(1)(2)(3)(4)

TIMING CONDITION PARAMETER		VALUE		UNIT
		MIN	MAX	
Input Conditions				
MMC/SD/SDIO 1 Interface (1.8-V IO) High-Speed SD Mode				
t_R	Input signal rise time	1091	4284	ps
t_F	Input signal fall time	1091	4284	ps
MMC/SD/SDIO 1 Interface (3.3-V IO) High-Speed SD Mode				
t_R	Input signal rise time	1345	5283	ps
t_F	Input signal fall time	1345	5283	ps
PCB Conditions				
	Number of external peripherals		1	
	Far end load		10	pF
	Trace length		10	cm

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Table 6-190. MMC/SD/SDIO 1 Interface Timing Conditions—High-Speed SD Mode[(1)(2)(3)(4)] (continued)

TIMING CONDITION PARAMETER			VALUE		UNIT
			MIN	MAX	
	Characteristics impedance	SanDisk Extreme III cards	45	55	Ω
		Other card types	20	70	

(1) IO settings: SPEEDCTRL = 1
For more information, see
- The Control Module Functional Description / Extended-Drain I/O and PBIAS Cell / Extended-Drain I/O section or
- The Control Module / Control Module Functional Description / Functional Register Description / Signal Integrity Parameter Control Registers with Pad Group Assignment / Device Interfaces Signal Group Controls Mapping section

of the OMAP4430 TRM.

(2) In this table the rise and fall times are calculated for the V_{IL} / V_{IH} described in Section 3.3.11, *MMC/SDIO DC Electrical Characteristics*.

(3) For more information on SDMMC ESD guideline examples, see Section A.3.2.2.1, *ESD Implementation—MMC/SD/SDIO 1 Interface—SD Mode.*

(4) To have an idea of the output OMAP4 ball load supported for this application, you can consider the following:
Output OMAP4 ball load = Far End load + 1.34 pF/cm typical x trace length (cm).

Table 6-191. MMC/SD/SDIO 1 Interface Timing Requirements—High-Speed SD Mode[(1)(2)]

NO.	PARAMETER		OPP100		OPP50		UNIT
			MIN	MAX	MIN	MAX	
MMC/SD/SDIO 1 Interface (1.8-V IO) High-Speed SD Mode							
HSSDR253	$t_{su(CMDV-CLKH)}$	Setup time, sdmmc1_cmd valid before sdmmc1_clk rising clock edge	4.6		4.6		ns
HSSDR254	$t_{h(clkH-CMDIV)}$	Hold time, sdmmc1_cmd valid after sdmmc1_clk rising clock edge	2.1		2.1		ns
HSSDR257	$t_{su(datV-CLKH)}$	Setup time, sdmmc1_dat[n:0] valid before sdmmc1_clk rising clock edge	4.6		4.6		ns
HSSDR258	$t_{h(clkH-datIV)}$	Hold time, sdmmc1_dat[n:0] valid after sdmmc1_clk rising clock edge	2.1		2.1		ns
MMC/SD/SDIO 1 Interface (3.3-V IO) High-Speed SD Mode							
HSSDR253	$t_{su(CMDV-CLKH)}$	Setup time, sdmmc1_cmd valid before sdmmc1_clk rising clock edge	4.6		4.6		ns
HSSDR254	$t_{h(clkH-CMDIV)}$	Hold time, sdmmc1_cmd valid after sdmmc1_clk rising clock edge	2.1		2.1		ns
HSSDR257	$t_{su(datV-CLKH)}$	Setup time, sdmmc1_dat[n:0] valid before sdmmc1_clk rising clock edge	4.6		4.6		ns
HSSDR258	$t_{h(clkH-datIV)}$	Hold time, sdmmc1_dat[n:0] valid after sdmmc1_clk rising clock edge	2.1		2.1		ns

(1) In sdmmc1_dat[n:0], n up to 7

(2) See DM Operating Condition Addendum for CORE OPP voltages.

Table 6-192. MMC/SD/SDIO 1 Interface Switching Characteristics—High-Speed SD Mode[(4)(5)]

NO.	PARAMETER		OPP100		OPP50		UNIT
			MIN	MAX	MIN	MAX	
MMC/SD/SDIO 1 Interface (1.8-V IO) High-Speed SD Mode							
HSSDR251	$1 / t_{c(clk)}$	Frequency[(1)], output sdmmc1_clk		48		48	MHz
HSSDR252	$t_{w(clkH)}$	Typical pulse duration, output sdmmc1_clk high	0.5*P[(2)]		0.5*P[(2)]		ns
HSSDR252	$t_{w(clkL)}$	Typical pulse duration, output sdmmc1_clk low	0.5*P[(2)]		0.5*P[(2)]		ns
	$t_{dc(clk)}$	Duty cycle error, output sdmmc1_clk	–1042	1042	–1042	1042	ps
	$t_{j(clk)}$	Jitter standard deviation[(3)], output sdmmc1_clk	–65	65	–65	65	ps
	$t_{R(clk)}$	Rise time, output sdmmc1_clk		2750		2750	ps
	$t_{F(clk)}$	Fall time, output sdmmc1_clk		2750		2750	ps
HSSDR255	$t_{d(clkL-doV)}$	Delay time, sdmmc1_clk rising clock edge to sdmmc1_cmd transition	4.5	12.4	4.5	12.4	ns

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Table 6-192. MMC/SD/SDIO 1 Interface Switching Characteristics—High-Speed SD Mode[4][5] (continued)

NO.	PARAMETER		OPP100 MIN	OPP100 MAX	OPP50 MIN	OPP50 MAX	UNIT
	$t_{R(do)}$	Rise time, output sdmmc1_cmd		2750		2750	ps
	$t_{F(do)}$	Fall time, output sdmmc1_cmd		2750		2750	ps
HSSDR256	$t_{d(clkL-doV)}$	Delay time, sdmmc1_clk rising clock edge to sdmmc1_daty transition	4.5	12.4	4.5	12.4	ns
	$t_{R(do)}$	Rise time, output sdmmc1_dat[n:0]		2750		2750	ps
	$t_{F(do)}$	Fall time, output sdmmc1_dat[n:0]		2750		2750	ps
MMC/SD/SDIO 1 Interface (3.3-V IO) High-Speed SD Mode							
HSSDR251	$1 / t_{c(clk)}$	Frequency[1], output sdmmc1_clk		48		48	MHz
HSSDR252	$t_{w(clkH)}$	Typical pulse duration, output sdmmc1_clk high	0.5*P[2]		0.5*P[2]		ns
HSSDR252	$t_{w(clkL)}$	Typical pulse duration, output sdmmc1_clk low	0.5*P[2]		0.5*P[2]		ns
	$t_{dc(clk)}$	Duty cycle error, output sdmmc1_clk	–1042	1042	–1042	1042	ps
	$t_{j(clk)}$	Jitter standard deviation[3], output sdmmc1_clk	–65	65	–65	65	ps
	$t_{R(clk)}$	Rise time, output sdmmc1_clk		3012		3012	ps
	$t_{F(clk)}$	Fall time, output sdmmc1_clk		3012		3012	ps
HSSDR255	$t_{d(clkL-doV)}$	Delay time, sdmmc1_clk rising clock edge to sdmmc1_cmd transition	4.5	12.4	4.5	12.4	ns
	$t_{R(do)}$	Rise time, output sdmmc1_cmd		3012		3012	ps
	$t_{F(do)}$	Fall time, output sdmmc1_cmd		3012		3012	ps
HSSDR256	$t_{d(clkL-doV)}$	Delay time, sdmmc1_clk rising clock edge to sdmmc1_daty transition	4.5	12.4	4.5	12.4	ns
	$t_{R(do)}$	Rise time, output sdmmc1_dat[n:0]		3012		3012	ps
	$t_{F(do)}$	Fall time, output sdmmc1_dat[n:0]		3012		3012	ps

(1) Related to the output sdmmc1_clk maximum and minimum frequency.
(2) P = output sdmmc1_clk period in ns
(3) The jitter probability density can be approximated by a Gaussian function.
(4) In sdmmc1_dat[n:0], n up to 7
(5) See DM Operating Condition Addendum for CORE OPP voltages.

Figure 6-113. MMC/SD/SDIO 1 Interface—High-Speed SD Mode—Transmitter Mode[1]

(1) In sdmmc1_dat[n:0], n up to 7

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Figure 6-114. MMC/SD/SDIO 1 Interface—High-Speed SD Mode—Receiver Mode(1)

(1) In sdmmc1_dat[n:0], n up to 7

6.7.1.1.3 MMC/SD/SDIO 1 Interface—High-Speed SDR50 Mode

Table 6-194 and Table 6-195 assume testing over the recommended operating conditions and electrical characteristic conditions below (see Figure 6-115 through Figure 6-116).

Table 6-193. MMC/SD/SDIO 1 Interface Timing Conditions—High-Speed SDR50 Mode(1)(2)(3)(4)

TIMING CONDITION PARAMETER			VALUE		UNIT
			MIN	MAX	
Input Conditions					
t_R	Input signal rise time		1091	4284	ps
t_F	Input signal fall time		1091	4284	ps
PCB Conditions					
	Number of external peripherals			1	
	Far end load			10	pF
	Trace length			10	cm
	Characteristics impedance	SanDisk Extreme III cards	45	55	Ω
		Other card types	20	70	

(1) IO settings: SPEEDCTRL = 1
For more information, see
– The Control Module Functional Description / Extended-Drain I/O and PBIAS Cell / Extended-Drain I/O section or
– The Control Module / Control Module Functional Description / Functional Register Description / Signal Integrity Parameter Control Registers with Pad Group Assignment / Device Interfaces Signal Group Controls Mapping section
of the OMAP4430 TRM.

(2) In this table the rise and fall times are calculated for the V_{IL} / V_{IH} described in Section 3.3.11, *MMC/SDIO DC Electrical Characteristics*.

(3) For more information on SDMMC ESD guideline examples, see Section A.3.2.2.1, *ESD Implementation—MMC/SD/SDIO 1 Interface—SD Mode.*

(4) To have an idea of the output OMAP4 ball load supported for this application, you can consider the following:
Output OMAP4 ball load = Far End load + 1.34 pF/cm typical x trace length (cm).

Table 6-194. MMC/SD/SDIO 1 Interface Timing Requirements—High-Speed SDR50 Mode(1)(2)

NO.	PARAMETER		OPP100		OPP50		UNIT
			MIN	MAX	MIN	MAX	
MMC/SD/SDIO 1 Interface (1.8-V IO)							
HSSDR503	$t_{su(cmdV-clkH)}$	Setup time, sdmmc1_cmd valid before sdmmc1_clk rising clock edge	6		21.6		ns
HSSDR504	$t_{h(clkH-cmdV)}$	Hold time, sdmmc1_cmd valid after sdmmc1_clk rising clock edge	1.2		1.2		ns
HSSDR507	$t_{su(dV-clkH)}$	Setup time, sdmmc1_dat[n:0] valid before sdmmc1_clk rising clock edge	6		21.6		ns
HSSDR508	$t_{h(clkH-dV)}$	Hold time, sdmmc1_dat[n:0] valid after sdmmc1_clk rising clock edge	1.2		1.2		ns

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(1) In sdmmc1_dat[n:0], n up to 7
(2) See DM Operating Condition Addendum for CORE OPP voltages.

Table 6-195. MMC/SD/SDIO 1 Interface Switching Characteristics—High-Speed SDR50 Mode[4][5]

NO.	PARAMETER		OPP100		OPP50		UNIT
			MIN	MAX	MIN	MAX	
MMC/SD/SDIO 1 Interface (1.8-V IO)							
HSSDR501	$1 / t_{c(clk)}$	Frequency[1] output sdmmc1_clk		64		32	MHz
HSSDR502	$t_{w(clkL)}$	Pulse duration, output sdmmc1_clk low	0.5*P[2]		0.5*P[2]		ns
HSSDR502	$t_{w(clkH)}$	Pulse duration, output sdmmc1_clk high	0.5*P[2]		0.5*P[2]		ns
	$t_{dc(clk)}$	Duty cycle error, output sdmmc1_clk	–781	781	–1563	1563	ps
	$t_{j(clk)}$	Jitter standard deviation[3], output sdmmc1_clk	–65	65	–65	65	ps
	$t_{R(clk)}$	Rise time, output sdmmc1_clk		2750		2750	ps
	$t_{F(clk)}$	Fall time, output sdmmc1_clk		2750		2750	ps
HSSDR505	$t_{d(clkH-cmdV)}$	Delay time, output sdmmc1_clk rising clock edge to output sdmmc1_cmd valid	2.7	10.8	2.7	26.4	ns
HSSDR506	$t_{d(clkH-doV)}$	Delay time, output sdmmc1_clk rising clock edge to sdmmc1_dat[n:0] valid	2.7	10.8	2.7	26.4	ns
	$t_{R(cmd)}$	Rise time, output sdmmc1_cmd		2750		2750	ps
	$t_{F(cmd)}$	Fall time, output sdmmc1_cmd		2750		2750	ps
	$t_{R(DO)}$	Rise time, output sdmmc1_dat[n:0]		2750		2750	ps
	$t_{F(do)}$	Fall time, output sdmmc1_dat[n:0]		2750		2750	ps

(1) Related to the output sdmmc1_clk maximum and minimum frequency.
(2) P = output sdmmc1_clk period in ns
(3) The jitter probability density can be approximated by a Gaussian function.
(4) In sdmmc1_dat[n:0], n up to 7
(5) See DM Operating Condition Addendum for CORE OPP voltages.

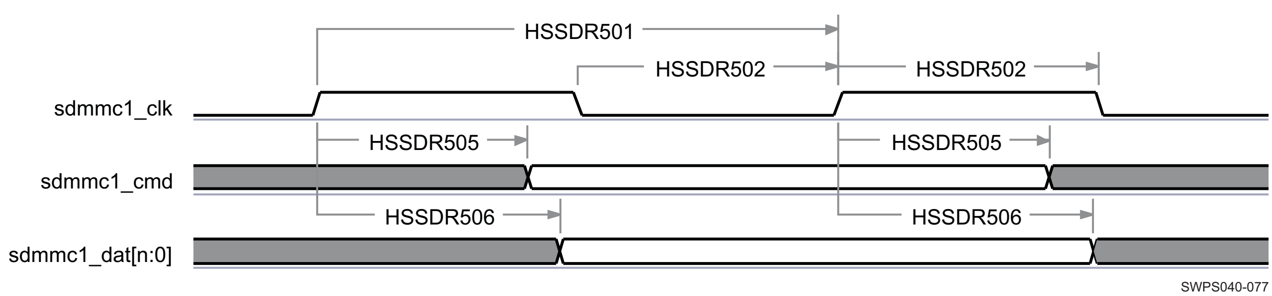

Figure 6-115. MMC/SD/SDIO 1 Interface—High-Speed SDR50—Transmitter Mode[1]

(1) In sdmmc1_dat[n:0], n up to 7

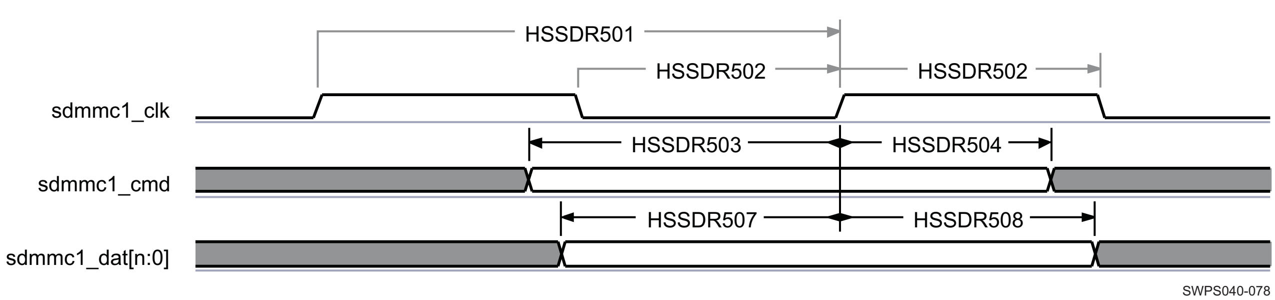

Figure 6-116. MMC/SD/SDIO 1 Interface—High-Speed SDR50—Receiver Mode[1]

(1) In sdmmc1_dat[n:0], n up to 7

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6.7.1.1.4 MMC/SD/SDIO 1 Interface—High-Speed SD Mode—DDR50

Table 6-197 and Table 6-198 assume testing over the recommended operating conditions and electrical characteristic conditions below (see Figure 6-117 through Figure 6-118).

Table 6-196. MMC/SD/SDIO 1 Interface Timing Conditions—High-Speed SD Mode—DDR50(1)(2)(3)(4)

TIMING CONDITION PARAMETER			VALUE		UNIT
			MIN	MAX	
Input Conditions					
t_R	Input signal rise time		700	2750	ps
t_F	Input signal fall time		700	2750	ps
PCB Conditions					
	Number of external peripherals			1	
	Far end load			10	pF
	Trace length			10	cm
	Characteristics impedance	SanDisk Extreme III cards	45	55	Ω
		Other card types	20	70	

(1) IO settings: SPEEDCTRL = 1
For more information, see
– The Control Module Functional Description / Extended-Drain I/O and PBIAS Cell / Extended-Drain I/O section or
– The Control Module / Control Module Functional Description / Functional Register Description / Signal Integrity Parameter Control Registers with Pad Group Assignment / Device Interfaces Signal Group Controls Mapping section
of the OMAP4430 TRM.

(2) In this table the rise and fall times are calculated for the V_{IL} / V_{IH} described in Section 3.3.11, *MMC/SDIO DC Electrical Characteristics*.

(3) For more information on SDMMC ESD guideline examples, see Section A.3.2.2.1, *ESD Implementation—MMC/SD/SDIO 1 Interface—SD Mode.*

(4) To have an idea of the output OMAP4 ball load supported for this application, you can consider the following:
Output OMAP4 ball load = Far End load + 1.34 pF/cm typical x trace length (cm).

Table 6-197. MMC/SD/SDIO 1 Interface Timing Requirements—High-Speed SD Mode—DDR50(1)(2)

NO.	PARAMETER		OPP100		OPP50		UNIT
			MIN	MAX	MIN	MAX	
MMC/SD/SDIO 1 Interface (1.8-V IO)							
HSSD3	$t_{su(cmdV-clkH)}$	Setup time, sdmmc1_cmd valid before sdmmc1_clk rising clock edge	5		25.3		ns
HSSD4	$t_{h(clkH-cmdV)}$	Hold time, sdmmc1_cmd valid after sdmmc1_clk rising clock edge	2		1.1		ns
HSSD7	$t_{su(dV-clkH)}$	Setup time, sdmmc1_dat[n:0] valid before sdmmc1_clk rising clock edge	0.9		10.2		ns
HSSD8	$t_{h(clkH-dV)}$	Hold time, sdmmc1_dat[n:0] valid after sdmmc1_clk rising clock edge	11.6		20.6		ns

(1) In sdmmc1_dat[n:0], n up to 7

(2) See DM Operating Condition Addendum for CORE OPP voltages.

Table 6-198. MMC/SD/SDIO 1 Interface Switching Characteristics—High-Speed SD Mode—DDR50(4)(5)

NO.	PARAMETER		OPP100		OPP50		UNIT
			MIN	MAX	MIN	MAX	
MMC/SD/SDIO 1 Interface (1.8-V IO)							
HSSD0	$1 / t_{c(clk)}$	Frequency(1) output sdmmc1_clk		48		24	MHz
HSSD1	$t_{w(clkL)}$	Pulse duration, output sdmmc1_clk low	0.5*P(2)		0.5*P(2)		ns
HSSD2	$t_{w(clkH)}$	Pulse duration, output sdmmc1_clk high	0.5*P(2)		0.5*P(2)		ns
	$t_{dc(clk)}$	Duty cycle error, output sdmmc1_clk	–521	521	–1042	1042	ps
	$t_{j(clk)}$	Jitter standard deviation(3), output sdmmc1_clk		65		65	ps

Table 6-198. MMC/SD/SDIO 1 Interface Switching Characteristics—High-Speed SD Mode—DDR50[(4)(5)] (continued)

NO.	PARAMETER		OPP100		OPP50		UNIT
			MIN	MAX	MIN	MAX	
	$t_{R(clk)}$	Rise time, output sdmmc1_clk		2750		2750	ps
	$t_{F(clk)}$	Fall time, output sdmmc1_clk		2750		2750	ps
HSSD5	$t_{d(clkH-cmdV)}$	Delay time, output sdmmc1_clk rising clock edge to output sdmmc1_cmd valid	2.3	14.1	3.3	33.9	ns
HSSD6	$t_{d(clkH-doV)}$	Delay time, output sdmmc1_clk rising clock edge to sdmmc1_dat[n:0] valid	–7.3	6.3	–16.2	15.2	ns
	$t_{R(cmd)}$	Rise time, output sdmmc1_cmd		2750		2750	ps
	$t_{F(cmd)}$	Fall time, output sdmmc1_cmd		2750		2750	ps
	$t_{R(DO)}$	Rise time, output sdmmc1_dat[n:0]		2750		2750	ps
	$t_{F(DO)}$	Fall time, output sdmmc1_dat[n:0]		2750		2750	ps

(1) Related to the output sdmmc1_clk maximum and minimum frequency.

(2) P = output sdmmc1_clk period in ns

(3) The jitter probability density can be approximated by a Gaussian function.

(4) In sdmmc1_dat[n:0], n up to 7

(5) See DM Operating Condition Addendum for CORE OPP voltages.

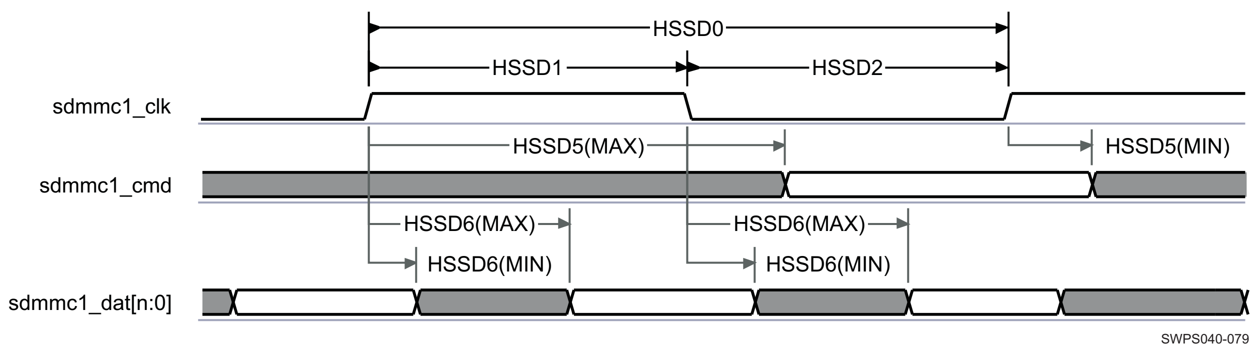

Figure 6-117. MMC/SD/SDIO 1 Interface—High-Speed SD—DDR50—Data/Command Transmit[(1)(2)]

(1) In sdmmc1_dat[n:0], n up to 7

(2) For further details about the registers used to configure SDMMC in DDR mode, please see the OMAP4430 TRM.

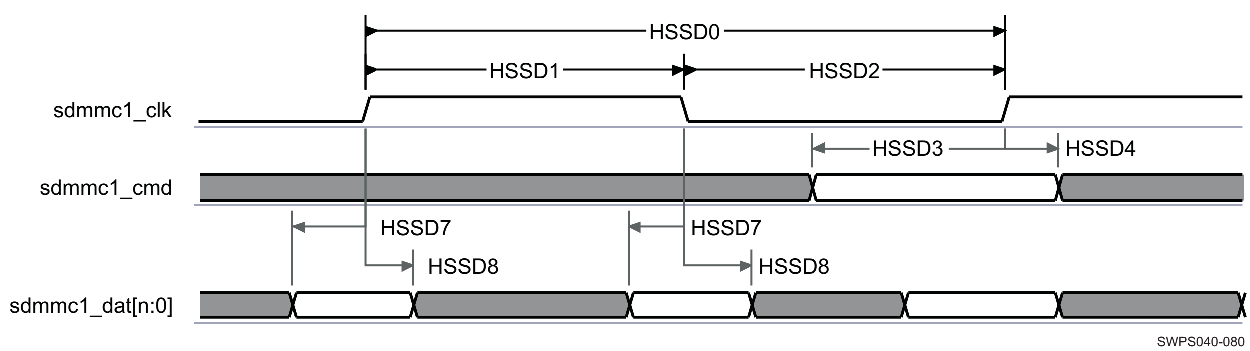

Figure 6-118. MMC/SD/SDIO 1 Interface—High-Speed SD—DDR50—Data/Command Receive[(1)(2)]

(1) In sdmmc1_dat[n:0], n up to 7

(2) For further details about the registers used to configure SDMMC in DDR mode, please see the OMAP4430 TRM.

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6.7.1.2 MMC/SD/SDIO 2 Interface

6.7.1.2.1 MMC/SD/SDIO 2 Interface—eMMC—High-Speed SDR JC64 Mode

Table 6-200 and Table 6-201 assume testing over the recommended operating conditions and electrical characteristic conditions below (see Figure 6-119 and Figure 6-120).

Table 6-199. MMC/SD/SDIO 2 Interface Timing Conditions—High-Speed SDR JC64 Mode(1)(2)(3)(4)(5)

TIMING CONDITION PARAMETER		VALUE		UNIT
		MIN	MAX	
For balls: AE5 / AF5 / AE4 / AF4 / AG3 / AF3 / AD2 / AD3 / AD4 / AC2 (Mux Mode 5)				
Input Conditions				
t_R	Input signal rise time	0.15	0.98	ns
t_F	Input signal fall time	0.15	0.98	ns
For balls: C12 / D12 / C13 / D13 / C15 / D15 / A16 / B16 / B11 / B12 (Mux Mode 1)				
Input Conditions				
t_R	Input signal rise time	0.11	1.01	ns
t_F	Input signal fall time	0.12	1.01	ns
PCB Conditions				
	Number of external peripherals		1	
	Far end load		5	pF
	Trace length		5	cm
	Characteristics impedance	30	55	Ω

(1) IO settings (Balls: AE5 / AF5 / AE4 / AF4 / AG3 / AF3 / AD2 / AD3 / AD4 / AC2 (Mux Mode 5)): LB0 = 1 and MB[1:0] = 11.
For more information, see Control Module / Control Module Functional Description/ Functional Register Description / Signal Integrity Parameter Control Registers with Pad Group Assignment / 50Ω Output Buffer I/Os with Combined Mode and Load Settings section of the OMAP4430 TRM.

(2) IO settings (Balls: C12 / D12 / C13 / D13 / C15 / D15 / A16 / B16 / B11 / B12 (Mux Mode 1)): LB0 = 0.
For more information, see Control Module / Control Module Functional Description/ Functional Register Description / Signal Integrity Parameter Control Registers with Pad Group Assignment section of the OMAP4430 TRM.

(3) In this table the rise and fall times are calculated for the V_{IL} / V_{IH} described in Section 3.3.11, *MMC/SDIO DC Electrical Characteristics*.

(4) For more information on SDMMC ESD guideline examples, see Section A.3.2.2.1, *ESD Implementation—MMC/SD/SDIO 1 Interface—SD Mode.*

(5) To have an idea of the output OMAP4 ball load supported for this application, you can consider the following:
Output OMAP4 ball load = Far End load + 1.34 pF/cm typical x trace length (cm).

Table 6-200. MMC/SD/SDIO 2 Interface Timing Requirements—High-Speed SDR JC64 Mode(1)(2)

NO.	PARAMETER		OPP100		OPP50		UNIT
			MIN	MAX	MIN	MAX	
For balls: AE5 / AF5 / AE4 / AF4 / AG3 / AF3 / AD2 / AD3 / AD4 / AC2 (Mux Mode 5)							
MMC3	$t_{su(cmdV-clkH)}$	Setup time, sdmmc2_cmd valid before sdmmc2_clk rising clock edge	6		6		ns
MMC4	$t_{h(clkH-cmdV)}$	Hold time, sdmmc2_cmd valid after sdmmc2_clk rising clock edge	1.6		1.6		ns
MMC7	$t_{su(dV-clkH)}$	Setup time, sdmmc2_dat[n:0] valid before sdmmc2_clk rising clock edge	6		6		ns
MMC8	$t_{h(clkH-dV)}$	Hold time, sdmmc2_dat[n:0] valid after sdmmc2_clk rising clock edge	1.6		1.6		ns
For balls: C12 / D12 / C13 / D13 / C15 / D15 / A16 / B16 / B11 / B12 (Mux Mode 1)							
MMC3	$t_{su(cmdV-clkH)}$	Setup time, sdmmc2_cmd valid before sdmmc2_clk rising clock edge	5.6		5.6		ns
MMC4	$t_{h(clkH-cmdV)}$	Hold time, sdmmc2_cmd valid after sdmmc2_clk rising clock edge	2.0		2.0		ns
MMC7	$t_{su(dV-clkH)}$	Setup time, sdmmc2_dat[n:0] valid before sdmmc2_clk rising clock edge	5.6		5.6		ns

Table 6-200. MMC/SD/SDIO 2 Interface Timing Requirements—High-Speed SDR JC64 Mode(1)(2) (continued)

NO.	PARAMETER		OPP100		OPP50		UNIT
			MIN	MAX	MIN	MAX	
MMC8	$t_{h(clkH-dV)}$	Hold time, sdmmc2_dat[n:0] valid after sdmmc2_clk rising clock edge	2.0		2.0		ns

(1) In sdmmc2_dat[n:0], n up to 7

(2) See DM Operating Condition Addendum for CORE OPP voltages.

Table 6-201. MMC/SD/SDIO Interface 2 Switching Characteristics—High-Speed SDR JC64 Mode(4)(5)(6)

NO.	PARAMETER		OPP100		OPP50		UNIT
			MIN	MAX	MIN	MAX	
For balls: AE5 / AF5 / AE4 / AF4 / AG3 / AF3 / AD2 / AD3 / AD4 / AC2 (Mux Mode 5)							
MMC1	$1 / t_{c(clk)}$	Frequency(1) output sdmmc2_clk		48		48	MHz
MMC2	$t_{w(clkL)}$	Pulse duration, output sdmmc2_clk low	0.5*P(2)		0.5*P(2)		ns
MMC2	$t_{w(clkH)}$	Pulse duration, output sdmmc2_clk high	0.5*P(2)		0.5*P(2)		ns
	$t_{dc(clk)}$	Duty cycle error, output sdmmc2_clk	–1042	1042	–1042	1042	ps
	$t_{j(clk)}$	Jitter standard deviation(3), output sdmmc2_clk	–65	65	–65	65	ps
	$t_{R(clk)}$	Rise time, output sdmmc2_clk		2263		2263	ps
	$t_{F(clk)}$	Fall time, output sdmmc2_clk		2136		2136	ps
MMC5	$t_{d(clkH-cmdV)}$	Delay time, sdmmc2_clk rising clock edge to sdmmc2_cmd transition	3.5	17	3.5	17	ns
	$t_{R(cmd)}$	Rise time, output sdmmc2_cmd		2263		2263	ps
	$t_{F(cmd)}$	Fall time, output sdmmc2_cmd		2136		2136	ps
MMC6	$t_{d(clkH-doV)}$	Delay time, sdmmc2_clk rising clock edge to sdmmc2_dat[n:0] transition	3.5	17	3.5	17	ns
	$t_{R(DO)}$	Rise time, output sdmmc2_dat[n:0]		2263		2263	ps
	$t_{F(do)}$	Fall time, output sdmmc2_dat[n:0]		2136		2136	ps
For balls: C12 / D12 / C13 / D13 / C15 / D15 / A16 / B16 / B11 / B12 (Mux Mode 1)							
MMC1	$1 / t_{c(clk)}$	Frequency(1) output sdmmc2_clk		48		48	MHz
MMC2	$t_{w(clkL)}$	Pulse duration, output sdmmc2_clk low	0.5*P(2)		0.5*P(2)		ns
MMC2	$t_{w(clkH)}$	Pulse duration, output sdmmc2_clk high	0.5*P(2)		0.5*P(2)		ns
	$t_{dc(clk)}$	Duty cycle error, output sdmmc2_clk	–1042	1042	–1042	1042	ps
	$t_{j(clk)}$	Jitter standard deviation(3), output sdmmc2_clk	–65	65	–65	65	ps
	$t_{R(clk)}$	Rise time, output sdmmc2_clk		2263		2263	ps
	$t_{F(clk)}$	Fall time, output sdmmc2_clk		2136		2136	ps
MMC5	$t_{d(clkH-cmdV)}$	Delay time, sdmmc2_clk rising clock edge to sdmmc2_cmd transition	3.5	16.9	3.5	16.9	ns
	$t_{R(cmd)}$	Rise time, output sdmmc2_cmd		2263		2263	ps
	$t_{F(cmd)}$	Fall time, output sdmmc2_cmd		2136		2136	ps
MMC6	$t_{d(clkH-doV)}$	Delay time, sdmmc2_clk rising clock edge to sdmmc2_dat[n:0] transition	3.5	16.9	3.5	16.9	ns
	$t_{R(DO)}$	Rise time, output sdmmc2_dat[n:0]		2263		2263	ps
	$t_{F(do)}$	Fall time, output sdmmc2_dat[n:0]		2136		2136	ps

(1) Related to the output sdmmcx_clk maximum and minimum frequency.

(2) P = output sdmmc2_clk period in ns

(3) The jitter probability density can be approximated by a Gaussian function.

(4) In sdmmc2_dat[n:0], n up to 7

(5) In this section, the MMC/SD/SDIO output data and command signals are driven on the falling clock edge.
In this case, the MMCHS_HCTL[2] HSPE bit is set to 0. The controller is by default in this mode to maximize hold timings.
For more information, see MMC/SD/SDIO / MMC/SD/SDIO Functional Description / Output Signals Generation / Generation on Falling Edge of MMC Clock section of the OMAP4430 TRM.

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(6) See DM Operating Condition Addendum for CORE OPP voltages.

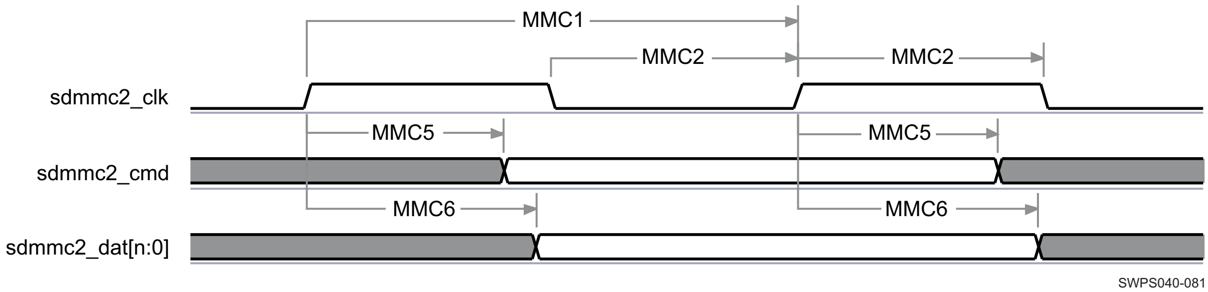

Figure 6-119. MMC/SD/SDIO 2 Interface—High-Speed SDR JC64—Transmitter Mode[(1)(2)]

(1) In sdmmc2_dat[n:0], n up to 7

(2) In this section, the MMC/SD/SDIO output data and command signals are driven on the falling clock edge.
In this case, the MMCHS_HCTL[2] HSPE bit is set to 0. The controller is by default in this mode to maximize hold timings.
For more information, see MMC/SD/SDIO / MMC/SD/SDIO Functional Description / Output Signals Generation / Generation on Falling Edge of MMC Clock section of the OMAP4430 TRM.

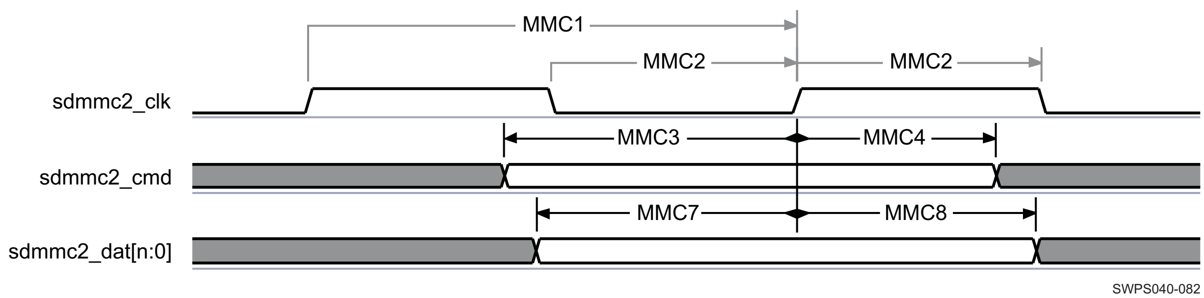

Figure 6-120. MMC/SD/SDIO 2 Interface—High-Speed SDR JC64—Receiver Mode[(1)]

(1) In sdmmc2_dat[n:0], n up to 7

6.7.1.2.2 MMC/SD/SDIO 2 Interface—eMMC—High-Speed DDR JC64 Mode

Table 6-203 and Table 6-204 assume testing over the recommended operating conditions and electrical characteristic conditions below (see Figure 6-121 and Figure 6-122).

Table 6-202. MMC/SD/SDIO 2 Interface Timing Conditions—High-Speed DDR JC64 Mode[(1)(2)(3)(4)(5)]

TIMING CONDITION PARAMETER		VALUE		UNIT
		MIN	MAX	
For Balls: AE5 / AF5 / AE4 / AF4 / AG3 / AF3 / AD2 / AD3 / AD4 / AC2 (Mux Mode 5)				
Input Conditions				
t_R	Input command signal rise time	0.15	0.98	ns
t_F	Input command signal fall time	0.15	0.98	ns
t_R	Input data signal rise time	0.15	0.98	ns
t_F	Input data signal fall time	0.15	0.98	ns
For Balls: C12 / D12 / C13 / D13 / C15 / D15 / A16 / B16 / B11 / B12 (Mux Mode 1)				
Input Conditions				
t_R	Input command signal rise time	0.11	1.01	ns
t_F	Input command signal fall time	0.12	1.01	ns
t_R	Input data signal rise time	0.11	1.01	ns
t_F	Input data signal fall time	0.12	1.01	ns
PCB Conditions				

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Table 6-202. MMC/SD/SDIO 2 Interface Timing Conditions—High-Speed DDR JC64 Mode(1)(2)(3)(4)(5) (continued)

TIMING CONDITION PARAMETER		VALUE		UNIT
		MIN	MAX	
	Number of external peripherals		1	
	Far end load		5	pF
	Trace length		5	cm
	Characteristics impedance	30	55	Ω

(1) IO settings (Balls: AE5 / AF5 / AE4 / AF4 / AG3 / AF3 / AD2 / AD3 / AD4 / AC2 (Mux Mode 5)): LB0 = 1 and MB[1:0] = 11. For more information, see Control Module / Control Module Functional Description/ Functional Register Description / Signal Integrity Parameter Control Registers with Pad Group Assignment / 50Ω Output Buffer I/Os with Combined Mode and Load Settings section of the OMAP4430 TRM.

(2) IO settings (Balls: C12 / D12 / C13 / D13 / C15 / D15 / A16 / B16 / B11 / B12 (Mux Mode 1)): LB0 = 0. For more information, see Control Module / Control Module Functional Description/ Functional Register Description / Signal Integrity Parameter Control Registers with Pad Group Assignment section of the OMAP4430 TRM.

(3) In this table the rise and fall times are calculated for the V_{IL} / V_{IH} described in Section 3.3.11, *MMC/SDIO DC Electrical Characteristics*.

(4) For more information on SDMMC ESD guideline examples, see Section A.3.2.2.1, *ESD Implementation—MMC/SD/SDIO 1 Interface—SD Mode.*

(5) To have an idea of the output OMAP4 ball load supported for this application, you can consider the following: Output OMAP4 ball load = Far End load + 1.34 pF/cm typical x trace length (cm).

Table 6-203. MMC/SD/SDIO 2 Interface Timing Requirements—High-Speed DDR JC64 Mode(1)(2)

NO.	PARAMETER		OPP100		OPP50		UNIT
			MIN	MAX	MIN	MAX	
For Balls: AE5 / AF5 / AE4 / AF4 / AG3 / AF3 / AD2 / AD3 / AD4 / AC2 (Mux Mode 5)							
DDReMMC3	$t_{su(dV-clkH)}$	Setup time, input sdmmc2_cmd valid before sdmmc2_clk rising clock edge	5.5		26		ns
DDReMMC4	$t_{h(clkH-dV)}$	Hold time, output sdmmc2_cmd valid after sdmmc2_clk rising clock edge	2.4		1.9		ns
DDReMMC7	$t_{su(dV-clkH)}$	Setup time, input sdmmc2_dat[n:0] valid before sdmmc2_clk rising clock edge	0.9		9.9		ns
DDReMMC8	$t_{h(clkH-dV)}$	Hold time, output sdmmc2_dat[n:0] valid after sdmmc2_clk rising clock edge	1.4		0.9		ns
For balls: C12 / D12 / C13 / D13 / C15 / D15 / A16 / B16 / B11 / B12 (Mux Mode 1)							
DDReMMC3	$t_{su(dV-clkH)}$	Setup time, input sdmmc2_cmd valid before sdmmc2_clk rising clock edge	5.5		26		ns
DDReMMC4	$t_{h(clkH-dV)}$	Hold time, output sdmmc2_cmd valid after sdmmc2_clk rising clock edge	2.4		1.9		ns
DDReMMC7	$t_{su(dV-clkH)}$	Setup time, input sdmmc2_dat[n:0] valid before sdmmc2_clk rising clock edge	1.4		10.4		ns
DDReMMC8	$t_{h(clkH-dV)}$	Hold time, output sdmmc2_dat[n:0] valid after sdmmc2_clk rising clock edge	0.9		0.4		ns

(1) In sdmmc2_dat[n:0], n up to 7

(2) See DM Operating Condition Addendum for CORE OPP voltages.

Table 6-204. MMC/SD/SDIO 2 Interface Switching Characteristics—High-Speed DDR JC64 Mode(4)(5)

NO.	PARAMETER		OPP100		OPP50		UNIT
			MIN	MAX	MIN	MAX	
For balls: AE5 / AF5 / AE4 / AF4 / AG3 / AF3 / AD2 / AD3 / AD4 / AC2 (Mux Mode 5)							
DDReMMC1	$1 / t_{c(clk)}$	Frequency(1) output sdmmc2_clk		48		24	MHz
DDReMMC2	$t_{w(clkL)}$	Pulse duration, output sdmmc2_clk low	0.5*P(2)		0.5*P(2)		ns
DDReMMC2	$t_{w(clkH)}$	Pulse duration, output sdmmc2_clk high	0.5*P(2)		0.5*P(2)		ns
	$t_{dc(clk)}$	Duty cycle error, output sdmmc2_clk	–1042	1042	–2083	2083	ps
	$t_{j(clk)}$	Jitter standard deviation(3), output sdmmc2_clk	–65	65	–65	65	ps

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Table 6-204. MMC/SD/SDIO 2 Interface Switching Characteristics—High-Speed DDR JC64 Mode[(4)(5)] (continued)

NO.	PARAMETER		OPP100		OPP50		UNIT
			MIN	MAX	MIN	MAX	
	$t_{R(clk)}$	Rise time, output sdmmc2_clk		2263		2263	ps
	$t_{F(clk)}$	Fall time, output sdmmc2_clk		2136		2136	ps
DDReMMC5	$t_{d(clkH-cmdV)}$	Delay time, sdmmc2_clk rising clock edge to sdmmc2_cmd transition	3.6	16.9	4	37.3	ns
	$t_{R(cmd)}$	Rise time, output sdmmc2_cmd		2263		2263	ps
	$t_{F(cmd)}$	Fall time, output sdmmc2_cmd		2136		2136	ps
DDReMMC6	$t_{d(clkH-doV)}$	Delay time, sdmmc2_clk rising clock edge to sdmmc2_dat[n:0] transition	3.1	6	3.5	15	ns
	$t_{R(DO)}$	Rise time, output sdmmc2_dat[n:0]		2263		2263	ps
	$t_{F(do)}$	Fall time, output sdmmc2_dat[n:0]		2136		2136	ps
For balls: C12 / D12 / C13 / D13 / C15 / D15 / A16 / B16 / B11 / B12 (Mux Mode 1)							
DDReMMC1	$1 / t_{c(clk)}$	Frequency[(1)] output sdmmc2_clk		48		24	MHz
DDReMMC2	$t_{w(clkL)}$	Pulse duration, output sdmmc2_clk low	0.5*P[(2)]		0.5*P[(2)]		ns
DDReMMC2	$t_{w(clkH)}$	Pulse duration, output sdmmc2_clk high	0.5*P[(2)]		0.5*P[(2)]		ns
	$t_{dc(clk)}$	Duty cycle error, output sdmmc2_clk	–1042	1042	–2083	2083	ps
	$t_{j(clk)}$	Jitter standard deviation[(3)], output sdmmc2_clk	–65	65	–65	65	ps
	$t_{R(clk)}$	Rise time, output sdmmc2_clk		2263		2263	ps
	$t_{F(clk)}$	Fall time, output sdmmc2_clk		2136		2136	ps
DDReMMC5	$t_{d(clkH-cmdV)}$	Delay time, sdmmc2_clk rising clock edge to sdmmc2_cmd transition	3.6	16.9	4	37.3	ns
	$t_{R(cmd)}$	Rise time, output sdmmc2_cmd		2263		2263	ps
	$t_{F(cmd)}$	Fall time, output sdmmc2_cmd		2136		2136	ps
DDReMMC6	$t_{d(clkH-doV)}$	Delay time, sdmmc2_clk rising clock edge to sdmmc2_dat[n:0] transition	3.1	6	3.5	15	ns
	$t_{R(DO)}$	Rise time, output sdmmc2_dat[n:0]		2263		2263	ps
	$t_{F(DO)}$	Fall time, output sdmmc2_dat[n:0]		2136		2136	ps

(1) Related to the output sdmmc2_clk maximum and minimum frequency.
(2) P = output sdmmc2_clk period in ns
(3) The jitter probability density can be approximated by a Gaussian function.
(4) In sdmmc2_dat[n:0], n up to 7
(5) See DM Operating Condition Addendum for CORE OPP voltages.

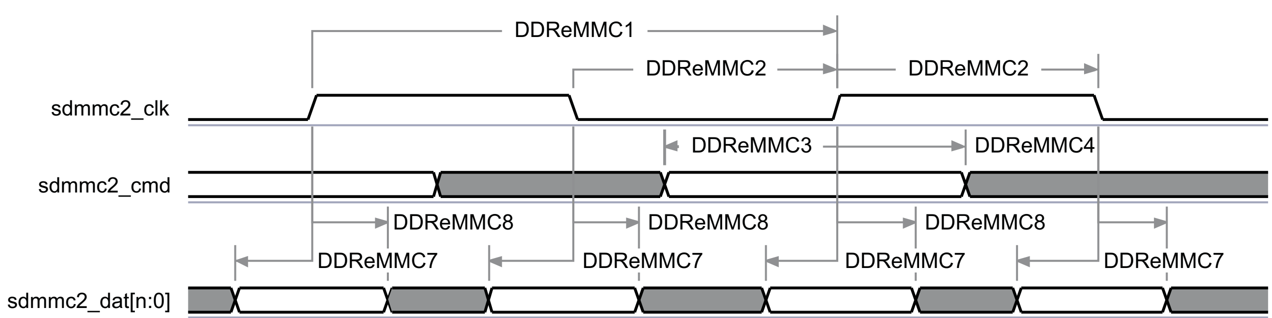

Figure 6-121. MMC/SD/SDIO 2 Interface—High-Speed DDR JC64—Receiver Mode[(1)]

(1) In sdmmc2_dat[n:0], n up to 7

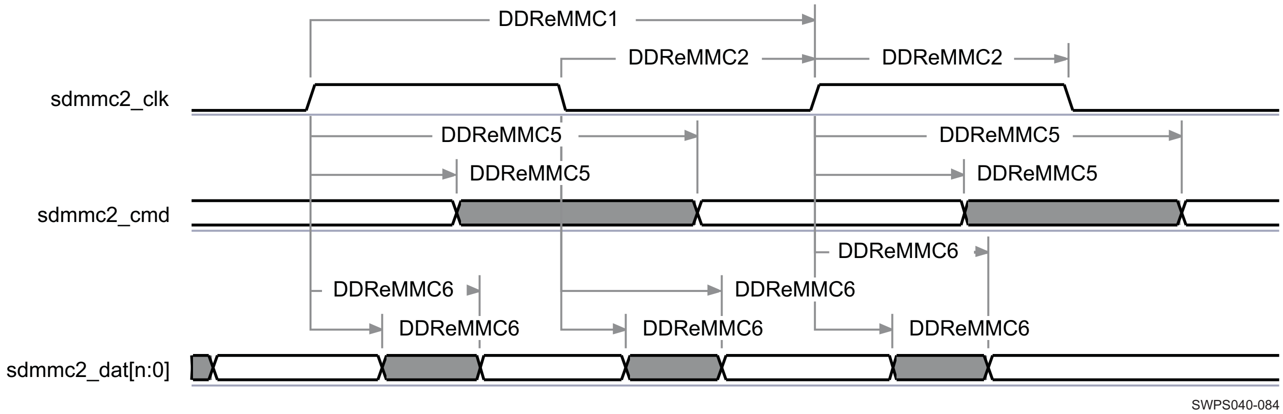

Figure 6-122. MMC/SD/SDIO 2 Interface—High-Speed DDR JC64—Transmitter Mode(1)

(1) In sdmmc2_dat[n:0], n up to 7

6.7.1.2.3 MMC/SD/SDIO 2 Interface—eMMC—Standard SDR JC64 Mode

Table 6-206 and Table 6-207 assume testing over the recommended operating conditions and electrical characteristic conditions below (see Figure 6-123 and Figure 6-124).

Table 6-205. MMC/SD/SDIO 2 Interface Timing Conditions—Standard SDR JC64 Mode(1)(2)(3)(4)

TIMING CONDITION PARAMETER		VALUE		UNIT
		MIN	MAX	
Input Conditions				
t_R	Input signal rise time	0.2	10	ns
t_F	Input signal fall time	0.2	10	ns
PCB Conditions				
	Number of external peripherals		1	
	Far end load		5	pF
	Trace length		5	cm
	Characteristics impedance	30	55	Ω

(1) IO settings (Balls: C12 / D12 / C13 / D13 / C15 / D15 / A16 / B16 / B11 / B12 (Mux Mode 1)): LB0 = 0.
For more information, see Control Module / Control Module Functional Description/ Functional Register Description / Signal Integrity Parameter Control Registers with Pad Group Assignment section of the OMAP4430 TRM.

(2) In this table the rise and fall times are calculated for the V_{IL} / V_{IH} described in Section 3.3.11, *MMC/SDIO DC Electrical Characteristics*.

(3) For more information on SDMMC ESD guideline examples, see Section A.3.2.2.1, *ESD Implementation—MMC/SD/SDIO 1 Interface—SD Mode.*

(4) To have an idea of the output OMAP4 ball load supported for this application, you can consider the following:
Output OMAP4 ball load = Far End load + 1.34 pF/cm typical x trace length (cm).

Table 6-206. MMC/SD/SDIO 2 Interface Timing Requirements—Standard SDR JC64 Mode(1)(2)

NO.	PARAMETER		OPP100		OPP50		UNIT
			MIN	MAX	MIN	MAX	
MMC3	$t_{su(cmdV-clkH)}$	Setup time, sdmmc2_cmd valid before sdmmc2_clk rising clock edge	3.5		3.5		ns
MMC4	$t_{h(clkH-cmdV)}$	Hold time, sdmmc2_cmd valid after sdmmc2_clk rising clock edge	8		8		ns
MMC7	$t_{su(dV-clkH)}$	Setup time, sdmmc2_dat[n:0] valid before sdmmc2_clk rising clock edge	3.5		3.5		ns
MMC8	$t_{h(clkH-dV)}$	Hold time, sdmmc2_dat[n:0] valid after sdmmc2_clk rising clock edge	8		8		ns

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(1) In sdmmc2_dat[n:0], n up to 7
(2) See DM Operating Condition Addendum for CORE OPP voltages.

Table 6-207. MMC/SD/SDIO 2 Interface Switching Characteristics—Standard SDR JC64 Mode[(4)(5)(6)]

NO.	PARAMETER		OPP100		OPP50		UNIT
			MIN	MAX	MIN	MAX	
MMC1	$1 / t_{c(clk)}$	Frequency[(1)] output sdmmc2_clk		24		24	MHz
MMC2	$t_{w(clkL)}$	Pulse duration, output sdmmc2_clk low	0.5*P[(2)]		0.5*P[(2)]		ns
MMC2	$t_{w(clkH)}$	Pulse duration, output sdmmc2_clk high	0.5*P[(2)]		0.5*P[(2)]		ns
	$t_{dc(clk)}$	Duty cycle error, output sdmmc2_clk	–2083	2083	–2083	2083	ps
	$t_{j(clk)}$	Jitter standard deviation[(3)], output sdmmc2_clk	–400	400	–400	400	ps
	$t_{R(clk)}$	Rise time, output sdmmc2_clk		7000		7000	ps
	$t_{F(clk)}$	Fall time, output sdmmc2_clk		7000		7000	ps
MMC5	$t_{d(clkH-cmdV)}$	Delay time, sdmmc2_clk rising clock edge to sdmmc2_cmd transition	4.1	37.2	4.1	37.2	ns
	$t_{R(cmd)}$	Rise time, output sdmmc2_cmd		7000		7000	ps
	$t_{F(cmd)}$	Fall time, output sdmmc2_cmd		7000		7000	ps
MMC6	$t_{d(clkH-doV)}$	Delay time, sdmmc2_clk rising clock edge to sdmmc2_dat[n:0] transition	4.1	37.2	4.1	37.2	ns
	$t_{R(DO)}$	Rise time, output sdmmc2_dat[n:0]		7000		7000	ps
	$t_{F(do)}$	Fall time, output sdmmc2_dat[n:0]		7000		7000	ps

(1) Related to the output sdmmcx_clk maximum and minimum frequency.
(2) P = output sdmmcx_clk period in ns
(3) The jitter probability density can be approximated by a Gaussian function.
(4) In sdmmcx_dat[n:0], n up to 7
(5) In this section, the MMC/SD/SDIO output data and command signals are driven on the falling clock edge.
In this case, the MMCHS_HCTL[2] HSPE bit is set to 0. The controller is by default in this mode to maximize hold timings.
For more information, see MMC/SD/SDIO / MMC/SD/SDIO Functional Description / Output Signals Generation / Generation on Falling Edge of MMC Clock section of the OMAP4430 TRM.
(6) See DM Operating Condition Addendum for CORE OPP voltages.

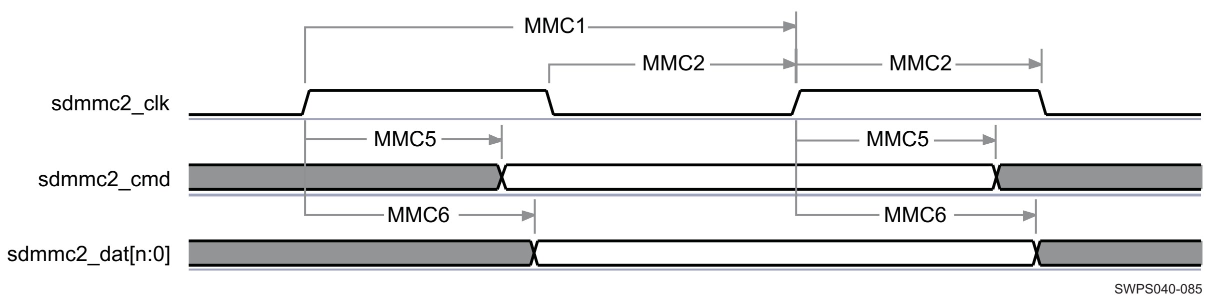

Figure 6-123. MMC/SD/SDIO 2 Interface—Standard SDR JC64—Transmitter Mode[(1)(2)]

(1) In sdmmc2_dat[n:0], n up to 7
(2) In this section, the MMC/SD/SDIO output data and command signals are driven on the falling clock edge.
In this case, the MMCHS_HCTL[2] HSPE bit is set to 0. The controller is by default in this mode to maximize hold timings.
For more information, see MMC/SD/SDIO / MMC/SD/SDIO Functional Description / Output Signals Generation / Generation on Falling Edge of MMC Clock section of the OMAP4430 TRM.

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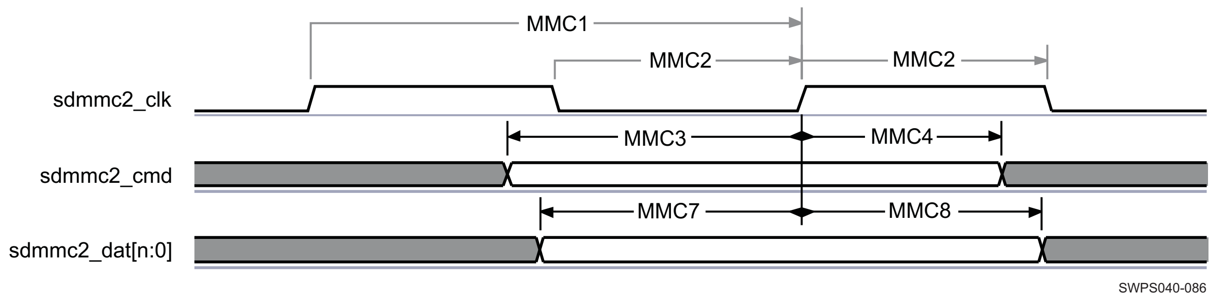

Figure 6-124. MMC/SD/SDIO 2 Interface—Standard SDR JC64—Receiver Mode(1)

(1) In sdmmc2_dat[n:0], n up to 7

6.7.1.3 MMC/SD/SDIO 3, 4, and 5 Interfaces

6.7.1.3.1 MMC/SD/SDIO 3, 4, and 5 Interfaces—High-Speed SDIO Mode

Table 6-209 and Table 6-210 assume testing over the recommended operating conditions and electrical characteristic conditions below (see Figure 6-125 and Figure 6-126).

Table 6-208. MMC/SD/SDIO 3, 4, and 5 Interface Timing Conditions—High-Speed SDIO Mode(1)(2)(3)(4)(5)

TIMING CONDITION PARAMETER		VALUE MIN	VALUE MAX	UNIT
For Balls: AB25 / AC27 / AB26 / AB27 / AA25 / AA26 (Mux Mode 1 – Interface 3) For Balls: AE21 / AF20 / AF21 / AE20 / AG20 / AH19 (Mux Mode 1 – Interface 4) For Balls: AE5 / AF5 / AE4 / AF4 / AG3 / AF3 (Mux Mode 0 – Interface 5)				
Input Conditions				
t_R	Input signal rise time	0.14	1.18	ns
t_F	Input signal fall time	0.11	1.18	ns
For balls: AG11 / AH11 / AE10 / AF10 / AG10 / AE9 (Mux Mode 2 – Interface 3) For balls: AG12 / AF12 / AE12 / AG13 / AE11 / AF11 (Mux Mode 2 – Interface 4)				
Input Conditions				
t_R	Input signal rise time	0.18	1.67	ns
t_F	Input signal fall time	0.17	1.58	ns
PCB Conditions				
	Number of external peripherals		1	
	Far end load		5	pF
	Trace length		5	cm
	Characteristics impedance	30	60	Ω

(1) IO settings (For balls: AB25 / AC27 / AB26 / AB27 / AA25 / AA26 (Mux Mode 1 – Interface 3)
For balls: AE21 / AF20 / AF21 / AE20 / AG20 / AH19 (Mux Mode 1 – Interface 4)
For balls: AE5 / AF5 / AE4 / AF4 / AG3 / AF3 (Mux Mode 0 – Interface 5)): LB0 = 1 and MB[1:0] = 11.
For more information, see Control Module / Control Module Functional Description/ Functional Register Description / Signal Integrity Parameter Control Registers with Pad Group Assignment / 50Ω Output Buffer I/Os with Combined Mode and Load Settings section of the OMAP4430 TRM.

(2) IO settings (For balls: AG11 / AH11 / AE10 / AF10 / AG10 / AE9 (Mux Mode 2 – Interface 3)
For balls: AG12 / AF12 / AE12 / AG13 / AE11 / AF11 (Mux Mode 2 – Interface 4)): DS0 = 0.
For more information, see Control Module / Control Module Functional Description/ Functional Register Description / Signal Integrity Parameter Control Registers with Pad Group Assignment / I/O cells with Configurable Output Driver Impedance section of the OMAP4430 TRM.

(3) In this table the rise and fall times are calculated for the V_{IL} / V_{IH} described in Section 3.3.11, *MMC/SDIO DC Electrical Characteristics*.

(4) For more information on SDMMC ESD guideline examples, see Section A.3.2.2.1, *ESD Implementation—MMC/SD/SDIO 1 Interface—SD Mode.*

(5) To have an idea of the output OMAP4 ball load supported for this application, you can consider the following:
Output OMAP4 ball load = Far End load + 1.34 pF/cm typical x trace length (cm).

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Table 6-209. MMC/SD/SDIO 3, 4, and 5 Interface Timing Requirements—High-Speed SDIO Mode(1)(2)(3)

NO.	PARAMETER		OPP100		OPP50		UNIT
			MIN	MAX	MIN	MAX	
For Balls: AB25 / AC27 / AB26 / AB27 / AA25 / AA26 (Mux Mode 1 – Interface 3) For Balls: AE21 / AF20 / AF21 / AE20 / AG20 / AH19 (Mux Mode 1 – Interface 4) For Balls: AE5 / AF5 / AE4 / AF4 / AG3 / AF3 (Mux Mode 0 – Interface 5)							
HSSDIO3	$t_{su(cmdV-clkH)}$	Setup time,sdmmcx_cmd valid before sdmmcx_clk rising clock edge	4.5		4.5		ns
HSSDIO4	$t_{h(clkH-cmdV)}$	Hold time,sdmmcx_cmd valid after sdmmcx_clk rising clock edge	2.3		2.3		ns
HSSDIO7	$t_{su(dV-clkH)}$	Setup time,sdmmcx_dat[n:0] valid before sdmmcx_clk rising clock edge	4.5		4.5		ns
HSSDIO8	$t_{h(clkH-dV)}$	Hold time, sdmmcx_dat[n:0] valid after sdmmcx_clk rising clock edge	2.3		2.3		ns
For Balls: AG11 / AH11 / AE10 / AF10 / AG10 / AE9 (Mux Mode 2 – Interface 3) For Balls: AG12 / AF12 / AE12 / AG13 / AE11 / AF11 (Mux Mode 2 – Interface 4)							
HSSDIO3	$t_{su(cmdV-clkH)}$	Setup time,sdmmcx_cmd valid before sdmmcx_clk rising clock edge	4.1		4.1		ns
HSSDIO4	$t_{h(clkH-cmdV)}$	Hold time,sdmmcx_cmd valid after sdmmcx_clk rising clock edge	1.9		1.9		ns
HSSDIO7	$t_{su(dV-clkH)}$	Setup time,sdmmcx_dat[n:0] valid before sdmmcx_clk rising clock edge	4.1		4.1		ns
HSSDIO8	$t_{h(clkH-dV)}$	Hold time, sdmmcx_dat[n:0] valid after sdmmcx_clk rising clock edge	1.9		1.9		ns

(1) In sdmmcx, x is equal to 3, 4 or 5.
(2) In sdmmcx_dat[n:0], n up to 3.
(3) See DM Operating Condition Addendum for CORE OPP voltages.

Table 6-210. MMC/SD/SDIO 3, 4, and 5 Interface Switching Characteristics—High-Speed SDIO Mode(4)(5)(6)

NO.	PARAMETER		OPP100		OPP50		UNIT
			MIN	MAX	MIN	MAX	
For Balls: AB25 / AC27 / AB26 / AB27 / AA25 / AA26 (Mux Mode 1 – Interface 3) For Balls: AE21 / AF20 / AF21 / AE20 / AG20 / AH19 (Mux Mode 1 – Interface 4) For Balls: AE5 / AF5 / AE4 / AF4 / AG3 / AF3 (Mux Mode 0 – Interface 5)							
HSSDIO1	$1 / t_{c(clk)}$	Frequency(1) output sdmmcx_clk		48		48	MHz
HSSDIO2	$t_{w(clkL)}$	Pulse duration, output sdmmcx_clk low	0.5*P(2)		0.5*P(2)		ns
HSSDIO2	$t_{w(clkH)}$	Pulse duration, output sdmmcx_clk high	0.5*P(2)		0.5*P(2)		ns
	$t_{dc(clk)}$	Duty cycle error, output sdmmcx_clk	–1042	1042	–1042	1042	ps
	$t_{j(clk)}$	Jitter standard deviation(3), output sdmmcx_clk	–65	65	–65	65	ps
	$t_{R(clk)}$	Rise time, output sdmmcx_clk		2263		2263	ps
	$t_{F(clk)}$	Fall time, output sdmmcx_clk		2136		2136	ps
HSSDIO5	$t_{d(clkH-cmdV)}$	Delay time, sdmmcx_clk rising clock edge to sdmmcx_cmd transition	2.6	13.9	2.6	13.9	ns
	$t_{R(cmd)}$	Rise time, output sdmmcx_cmd		2263		2263	ps
	$t_{F(cmd)}$	Fall time, output sdmmcx_cmd		2136		2136	ps
HSSDIO6	$t_{d(clkH-doV)}$	Delay time, sdmmcx_clk rising clock edge to sdmmcx_dat[n:0] transition	2.6	13.9	2.6	13.9	ns
	$t_{R(DO)}$	Rise time, output sdmmcx_dat[n:0]		2263		2263	ps
	$t_{F(DO)}$	Fall time, output sdmmcx_dat[n:0]		2136		2136	ps
For Balls: AG11 / AH11 / AE10 / AF10 / AG10 / AE9 (Mux Mode 2 – Interface 3) For Balls: AG12 / AF12 / AE12 / AG13 / AE11 / AF11 (Mux Mode 2 – Interface 4)							
HSSDIO1	$1 / t_{c(clk)}$	Frequency(1) output sdmmcx_clk		48		48	MHz
HSSDIO2	$t_{w(clkL)}$	Pulse duration, output sdmmcx_clk low	0.5*P(2)		0.5*P(2)		ns
HSSDIO2	$t_{w(clkH)}$	Pulse duration, output sdmmcx_clk high	0.5*P(2)		0.5*P(2)		ns

Table 6-210. MMC/SD/SDIO 3, 4, and 5 Interface Switching Characteristics—High-Speed SDIO Mode(4)(5)(6) (continued)

NO.	PARAMETER		OPP100		OPP50		UNIT
			MIN	MAX	MIN	MAX	
	$t_{dc(clk)}$	Duty cycle error, output sdmmcx_clk	–1042	1042	–1042	1042	ps
	$t_{j(clk)}$	Jitter standard deviation(3), output sdmmcx_clk	–65	65	–65	65	ps
	$t_{R(clk)}$	Rise time, output sdmmcx_clk		2263		2263	ps
	$t_{F(clk)}$	Fall time, output sdmmcx_clk		2136		2136	ps
HSSDIO5	$t_{d(clkH-cmdV)}$	Delay time, sdmmcx_clk rising clock edge to sdmmcx_cmd transition	2.5	13.9	2.5	13.9	ns
	$t_{R(cmd)}$	Rise time, output sdmmcx_cmd		2263		2263	ps
	$t_{F(cmd)}$	Fall time, output sdmmcx_cmd		2136		2136	ps
HSSDIO6	$t_{d(clkH-doV)}$	Delay time, sdmmcx_clk rising clock edge to sdmmcx_dat[n:0] transition	2.5	13.9	2.5	13.9	ns
	$t_{R(DO)}$	Rise time, output sdmmcx_dat[n:0]		2263		2263	ps
	$t_{F(DO)}$	Fall time, output sdmmcx_dat[n:0]		2136		2136	ps

(1) Related to the output sdmmcx_clk maximum and minimum frequency.
(2) P = output sdmmcx_clk period in ns
(3) The jitter probability density can be approximated by a Gaussian function.
(4) In sdmmcx, x is equal to 3, 4 or 5.
(5) In sdmmcx_dat[n:0], n up to 3.
(6) See DM Operating Condition Addendum for CORE OPP voltages.

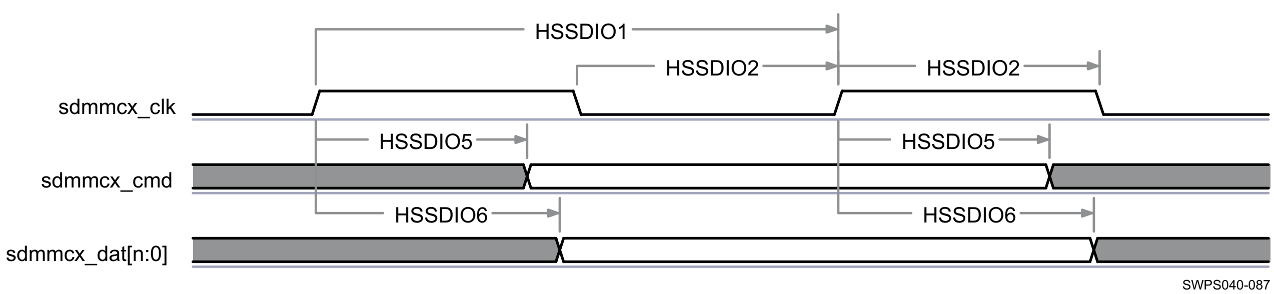

Figure 6-125. MMC/SD/SDIO 3, 4, and 5 Interfaces—High-Speed SDIO—Transmitter Mode(1)

(1) In sdmmcx, x = 3, 4, or 5. In sdmmcx_dat[n:0], n up to 3.

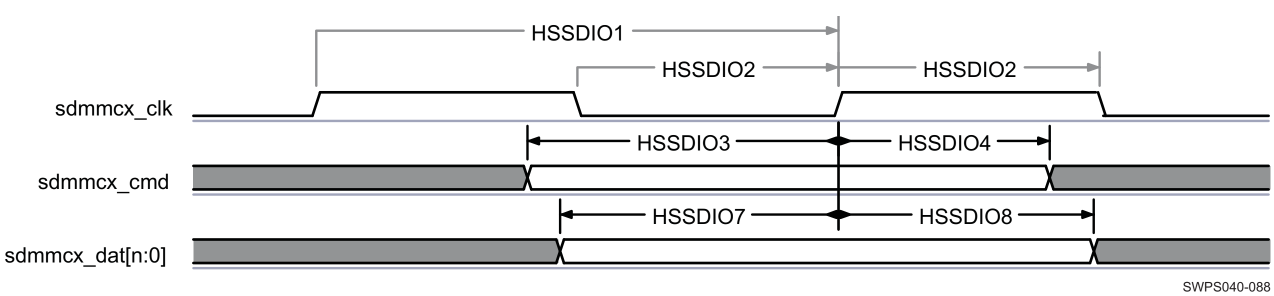

Figure 6-126. MMC/SD/SDIO 3, 4, and 5 Interfaces—High-Speed SDIO—Receiver Mode(1)

(1) In sdmmcx, x = 3, 4, or 5. In sdmmcx_dat[n:0], n up to 3.

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6.8 Test Interfaces

6.8.1 Digital Processing Manager Interface (DPM)

6.8.1.1 Trace Port Interface Unit (TPIU)

6.8.1.1.1 TPIU PLL DDR Mode – 160 MHz

Table 6-212 assumes testing over the recommended operating conditions and electrical characteristic conditions below (see Figure 6-127).

Table 6-211. TPIU Timing Conditions—PLL DDR Transmit Mode[(1)(2)(3)(8)]

TIMING CONDITION PARAMETER		VALUE		UNIT
		MIN	MAX	
PCB Conditions[(6)(7)]				
	Number of external peripherals		1	
	Far end load		10[(4)]	pF
	Trace length		10[(5)]	cm
	Characteristics impedance	40	60	Ω

(1) IO settings (balls: M2 / N2 / P2 / V1 / V2 / W1 / W2 / W3 / W4 / Y2 / Y3 / Y4 / AA1 / AA2 / AA3 / AA4 / AB2 / AB3 / AB4 / AC4): DS0 = 1.
For more information, see Control Module / Control Module Functional Description/ Functional Register Description / Signal Integrity Parameter Control Registers with Pad Group Assignment / I/O cells with Configurable Output Driver Impedance section of the OMAP4430 TRM.

(2) For more information regarding the subsystem multiplexing, see Section 2.4.5.3, *TPIU.*

(3) In this table the rise and fall times are calculated for 20% to 80% of VDDS. For more information on the corresponding OMAP4 VDDS power supply name, see Table 2-1, POWER [9] column with the ball name.

(4) Either use a far end load less than 10 pF, or add an external buffer in case of higher loads.

(5) Either use a maximum trace length equals to 10 cm, or a 5-cm cable and a 5-cm PCB.

(6) A serial resistor of 15 Ω is recommended to be added to limit the overshoot and the undershoot on far end signals.

(7) It is also recommended to minimize the number of vias by layer transitions.

(8) To have an idea of the output OMAP4 ball load supported for this application, you can consider the following:
Output OMAP4 ball load = Far End load + 1.34 pF/cm typical x trace length (cm).

Table 6-212. TPIU Switching Characteristics—PLL DDR Transmit Mode[(5)]

NO.	PARAMETER		OPP100		OPP50		UNIT
			MIN	MAX	MIN	MAX	
TPIU1	$1 / t_{c(clk)}$	Frequency[(1)], output clock atpiu_clk		160		160	MHz
TPIU2	$t_{w(clkH)}$	Pulse duration, output clock atpiu_clk high	0.5*P[(2)]		0.5*P[(2)]		ns
TPIU3	$t_{w(clkL)}$	Pulse duration, output clock atpiu_clk low	0.5*P[(2)]		0.5*P[(2)]		ns
	$t_{dc(clk)}$	Duty cycle error, output clock atpiu_clk	–333	333	–333	333	ps
	$t_{j(clk)}$	Jitter standard deviation[(3)], output clock atpiu_clk		65		65	ps
	$t_{R(clk)}$	Rise time, output clock atpiu_clk		2.62		2.62	ns
	$t_{F(clk)}$	Fall time, output clock atpiu_clk		2		2	ns
TPIU4	$t_{d(clk-ctlV)}$	Delay time, output clock atpiu_clk low/high to output control atpiu_cntl transition		0.884		0.884	ns
TPIU5	$t_{d(clk-dataV)}$	Delay time, output clock atpiu_clk low/high to output data atpiu_d[n:0][(4)] transition		0.884		0.884	ns
	$t_{R(DO)}$	Rise time, output data atpiu_d[n:0][(4)] and output control atpiu_cntl		2.62		2.62	ns
	$t_{F(DO)}$	Fall time, output data atpiu_d[n:0][(4)] and output control atpiu_cntl		2		2	ns

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(1) Related to the atpiu_clk maximum frequency.
(2) P = atpiu_clk period in ns
(3) The jitter probability density can be approximated by a Gaussian function.
(4) In atpiu_d[n:0], n is equal to 15 or 17.
(5) See DM Operating Condition Addendum for CORE OPP voltages.

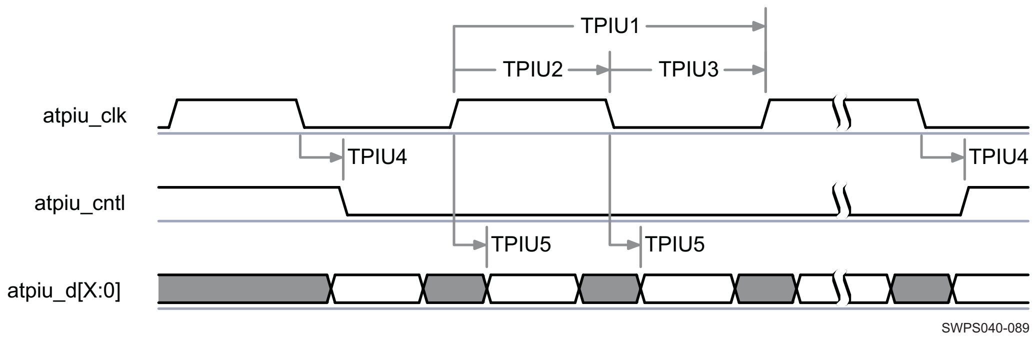

Figure 6-127. TPIU—PLL DDR Transmit Mode[(1)]

(1) In d[X:0], X is equal to 15 or 17.

6.8.1.2 System Trace Module Interface (STM)

The System Trace Module interface (STM) module provides real-time software tracing functionality to the OMAP4430 device.

The trace interface has four trace data pins and a trace clock pin.

This interface is a dual edge interface:

- The data are available on rising and falling edge of STM clock.
- But can be also configured in single-edge mode where data are available on the falling edge of STM clock.

Serial interface operates in clock stop regime: serial clock is not free-running; when there is no trace data, there is no trace clock.

6.8.1.2.1 STM – Lauterbach DDR Transmit Mode

Table 6-214 assumes testing over the recommended operating conditions and electrical characteristic conditions below (see Figure 6-128).

Table 6-213. STM Timing Conditions—Lauterbach DDR Transmit Mode[(1)(3)(8)]

TIMING CONDITION PARAMETER		VALUE		UNIT
		MIN	MAX	
PCB Conditions[(6)(7)]				
	Number of external peripherals		1	
	Far end load		10[(4)]	pF
	Trace length		10[(5)]	cm
	Characteristics impedance	45	60	Ω

(1) IO settings (Balls in Option 1: M2 / N2 / P2 / V1 / V2[(2)]
Balls in Option 2: AA4 / AB2 / AB3 / AB4 / AC4[(2)]
Balls in Option 3: M2 / N2[(2)]):
DS0 = 1.
For more information, see Control Module / Control Module Functional Description/ Functional Register Description / Signal Integrity Parameter Control Registers with Pad Group Assignment / I/O cells with Configurable Output Driver Impedance section of the OMAP4430 TRM.
(2) For more information regarding the subsystem multiplexing, see Section 2.4.5.4, *STM.*

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(3) In this table the rise and fall times are calculated for 20% to 80% of VDDS. For more information on the corresponding OMAP4 VDDS power supply name, see Table 2-1, POWER [9] column with the ball name.
(4) Either use a far end load less than 10 pF, or add an external buffer in case of higher loads.
(5) Either use a maximum trace length equals to 10 cm, or a 5-cm cable and a 5-cm PCB.
(6) A serial resistor of 15 Ω is recommended to be added to limit the overshoot and the undershoot on far end signals.
(7) It is also recommended to minimize the number of vias by layer transitions.
(8) To have an idea of the output OMAP4 ball load supported for this application, you can consider the following: Output OMAP4 ball load = Far End load + 1.34 pF/cm typical x trace length (cm).

Table 6-214. STM Switching Characteristics—Lauterbach DDR Transmit Mode[(4)]

NO.	PARAMETER		OPP100		OPP50		UNIT
			MIN	MAX	MIN	MAX	
STM1	$1 / t_{c(clk)}$	Frequency[(1)], output clock astm_clk		100		100	MHz
STM2	$t_{w(clkH)}$	Pulse duration, output clock astm_clk high	0.5*P[(2)]		0.5*P[(2)]		ns
STM3	$t_{w(clkL)}$	Pulse duration, output clock astm_clk low	0.5*P[(2)]		0.5*P[(2)]		ns
	$t_{dc(clk)}$	Duty cycle error, output clock astm_clk	–625	625	–1000	1000	ps
	$t_{j(clk)}$	Jitter standard deviation[(3)], output clock astm_clk		65		129	ps
	$t_{R(clk)}$	Rise time, output clock astm_clk		1.74		3.45	ns
	$t_{F(clk)}$	Fall time, output clock astm_clk		1.74		3.45	ns
STM4	$t_{d(clk-dataV)}$	Delay time, output clock astm_clk low/high to output control astm_d[3:0] valid	1.456	3.886	1.606	6.828	ns
	$t_{R(DO)}$	Rise time, output data astm_d[3:0]		1.74		3.45	ns
	$t_{F(DO)}$	Fall time, output data astm_d[3:0]		1.74		3.45	ns

(1) Related to the astm_clk maximum frequency.
(2) P = astm_clk period in ns
(3) The jitter probability density can be approximated by a Gaussian function.
(4) See DM Operating Condition Addendum for CORE OPP voltages.

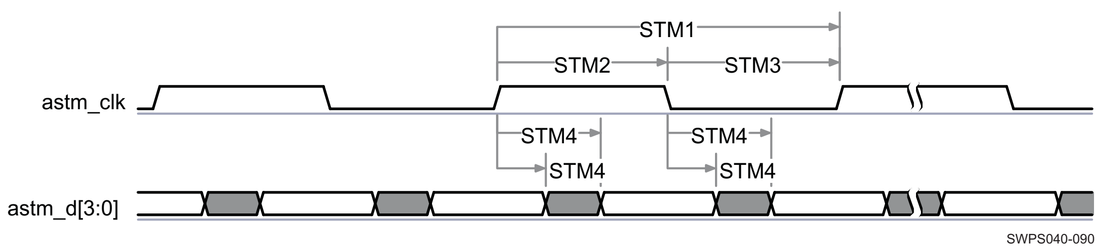

Figure 6-128. STM—Lauterbach DDR Transmit Mode

6.8.1.2.2 STM—MIPI Transmit Mode

6.8.1.2.2.1 STM—MIPI Transmit—DDR Mode

Table 6-216 assumes testing over the recommended operating conditions and electrical characteristic conditions below (see Figure 6-129).

Table 6-215. STM Timing Conditions—MIPI DDR Transmit Mode[(1)(3)(8)]

TIMING CONDITION PARAMETER		VALUE		UNIT
		MIN	MAX	
PCB Conditions[(6)(7)]				
	Number of external peripherals		1	
	Far end load		10[(4)]	pF
	Trace length		10[(5)]	cm

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Table 6-215. STM Timing Conditions—MIPI DDR Transmit Mode[(1)(3)(8)] (continued)

TIMING CONDITION PARAMETER		VALUE		UNIT
		MIN	MAX	
	Characteristics impedance	45	60	Ω

(1) IO settings (Balls in Option 1: M2 / N2 / P2 / V1 / V2[(2)]
Balls in Option 2: AA4 / AB2 / AB3 / AB4 / AC4[(2)]
Balls in Option 3: M2 / N2[(2)]): DS0 = 1.
For more information, see Control Module / Control Module Functional Description/ Functional Register Description / Signal Integrity Parameter Control Registers with Pad Group Assignment / I/O cells with Configurable Output Driver Impedance section of the OMAP4430 TRM.

(2) For more information regarding the subsystem multiplexing, see Section 2.4.5.4, *STM.*

(3) In this table the rise and fall times are calculated for 20% to 80% of VDDS. For more information on the corresponding OMAP4 VDDS power supply name, see Table 2-1, POWER [9] column with the ball name.

(4) Either use a far end load less than 10 pF, or add an external buffer in case of higher loads.

(5) Either use a maximum trace length equals to 10 cm, or a 5-cm cable and a 5-cm PCB.

(6) A serial resistor of 15 Ω is recommended to be added to limit the overshoot and the undershoot on far end signals.

(7) It is also recommended to minimize the number of vias by layer transitions.

(8) To have an idea of the output OMAP4 ball load supported for this application, you can consider the following:
Output OMAP4 ball load = Far End load + 1.34 pF/cm typical x trace length (cm).

Table 6-216. STM Switching Characteristics—MIPI DDR Transmit Mode[(4)]

NO.	PARAMETER		OPP100		OPP50		UNIT
			MIN	MAX	MIN	MAX	
STM1	$1 / t_{c(clk)}$	Frequency[(1)], output clock astm_clk		100		100	MHz
STM2	$t_{w(clkH)}$	Pulse duration, output clock astm_clk high	0.5*P[(2)]		0.5*P[(2)]		ns
STM3	$t_{w(clkL)}$	Pulse duration, output clock astm_clk low	0.5*P[(2)]		0.5*P[(2)]		ns
	$t_{dc(clk)}$	Duty cycle error, output clock astm_clk	–625	625	–625	625	ps
	$t_{j(clk)}$	Jitter standard deviation[(3)], output clock astm_clk		65		65	ps
	$t_{R(clk)}$	Rise time, output clock astm_clk		1.73		1.73	ns
	$t_{F(clk)}$	Fall time, output clock astm_clk		1.73		1.73	ns
STM4	$t_{d(clk-dataV)}$	Delay time, output clock astm_clk low/high to output control astm_d[3:0] valid	1.955	3.387	1.955	3.387	ns
	$t_{R(DO)}$	Rise time, output data astm_d[3:0]		1.73		1.73	ns
	$t_{F(DO)}$	Fall time, output data astm_d[3:0]		1.73		1.73	ns

(1) Related to astm_clk maximum frequency.

(2) P = astm_clk period in ns

(3) The jitter probability density can be approximated by a Gaussian function.

(4) See DM Operating Condition Addendum for CORE OPP voltages.

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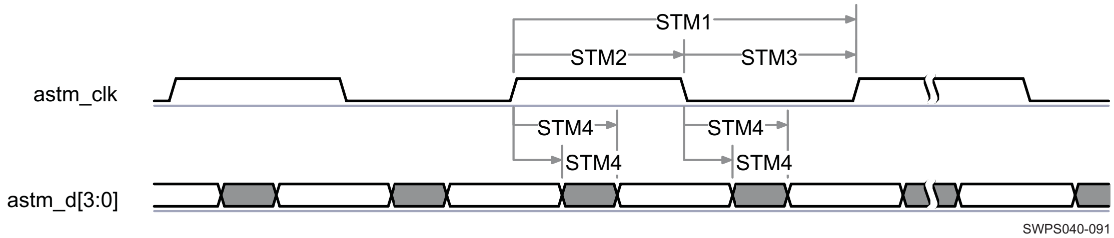

Figure 6-129. STM—MIPI DDR Transmit Mode

6.8.1.2.2.2 STM—MIPI Transmit—SDR Mode

Table 6-218 assumes testing over the recommended operating conditions and electrical characteristic conditions below (see Figure 6-130).

Table 6-217. STM Timing Conditions—MIPI SDR Transmit Mode(1)(3)(8)

TIMING CONDITION PARAMETER		VALUE		UNIT
		MIN	MAX	
PCB Conditions(6)(7)				
	Number of external peripherals		1	
	Far end load		10(4)	pF
	Trace length		10(5)	cm
	Characteristics impedance	45	60	Ω

(1) IO settings (Balls in Option 1: M2 / N2 / P2 / V1 / V2(2)
Balls in Option 2: AA4 / AB2 / AB3 / AB4 / AC4(2)
Balls in Option 3: M2 / N2(2)): DS0 = 1.
For more information, see Control Module / Control Module Functional Description/ Functional Register Description / Signal Integrity Parameter Control Registers with Pad Group Assignment / I/O cells with Configurable Output Driver Impedance section of the OMAP4430 TRM.

(2) For more information regarding the subsystem multiplexing, see Section 2.4.5.4, *STM.*

(3) In this table the rise and fall times are calculated for 20% to 80% of VDDS. For more information on the corresponding OMAP4 VDDS power supply name, see Table 2-1, POWER [9] column with the ball name.

(4) Either use a far end load less than 10 pF, or add an external buffer in case of higher loads.

(5) Either use a maximum trace length equals to 10 cm, or a 5-cm cable and a 5-cm PCB.

(6) A serial resistor of 15 Ω is recommended to be added to limit the overshoot and the undershoot on far end signals.

(7) It is also recommended to minimize the number of vias by layer transitions.

(8) To have an idea of the output OMAP4 ball load supported for this application, you can consider the following:
Output OMAP4 ball load = Far End load + 1.34 pF/cm typical x trace length (cm).

Table 6-218. STM Switching Characteristics—MIPI SDR Transmit Mode(4)

NO.	PARAMETER		OPP100		OPP50		UNIT
			MIN	MAX	MIN	MAX	
STM1	$1 / t_{c(clk)}$	Frequency(1), output clock astm_clk		100		100	MHz
STM2	$t_{w(clkH)}$	Pulse duration, output clock astm_clk high	0.5*P(2)		0.5*P(2)		ns
STM3	$t_{w(clkL)}$	Pulse duration, output clock astm_clk low	0.5*P(2)		0.5*P(2)		ns
	$t_{dc(clk)}$	Duty cycle error, output clock astm_clk	–500	500	–1000	1000	ps
	$t_{j(clk)}$	Jitter standard deviation(3), output clock astm_clk		65		129	ps
	$t_{R(clk)}$	Rise time, output clock astm_clk		1.73		6.90	ns
	$t_{F(clk)}$	Fall time, output clock astm_clk		1.73		6.90	ns
STM4	$t_{d(clk-dataV)}$	Delay time, output clock astm_clk low/high to output control astm_d[3:0] valid	–2.296	2.296	–6.313	6.313	ns
	$t_{R(DO)}$	Rise time, output data astm_d[3:0]		1.73		6.90	ns
	$t_{F(DO)}$	Fall time, output data astm_d[3:0]		1.73		6.90	ns

(1) Related to the astm_clk maximum frequency.

(2) P = astm_clk period in ns

(3) The jitter probability density can be approximated by a Gaussian function.

(4) See DM Operating Condition Addendum for CORE OPP voltages.

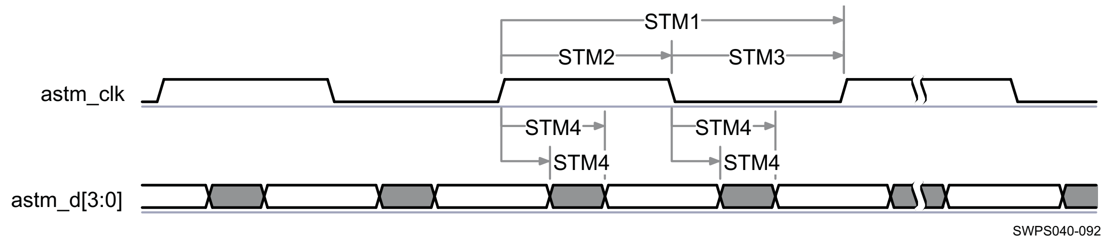

Figure 6-130. STM—MIPI SDR Transmit Mode

6.8.2 JTAG Interface (JTAG)

The JTAG TAP controller handles standard IEEE JTAG interfaces. The following section defines the Timing requirements for several tools used to test the OMAP4430 as:

- Free-running clock tool, like XDS560 and XDS510 tools
- Adaptive clock tool, like RealView® ICE tool and Lauterbach™ tool

6.8.2.1 JTAG—Free-Running Clock Mode

Table 6-220 and Table 6-221 assume testing over the recommended operating conditions and electrical characteristic conditions below (see Figure 6-131).

Table 6-219. JTAG Timing Conditions—Free-running Clock Mode(1)(3)(4)

TIMING CONDITION PARAMETER		VALUE		UNIT
		MIN	MAX	
Input Conditions				
t_R	Input signal rise time	5		ns
t_F	Input signal fall time	5		ns
PCB Conditions				
	Number of external peripherals		1	
	Far end load		30	pF
	Trace length		See(2)	cm
	Characteristics impedance	40	60	Ω

(1) Corresponding balls: AH2 / AG1 / AE3 / AH1 / AE1 / AE2

(2) Maximum PCB trace length = 5 cm and maximum cable = 15 cm

(3) For more information on JTAG ESD guideline example, see Section A.3.2.2.3, *ESD Implementation—JTAG and cJTAG Interfaces.*

(4) To have an idea of the output OMAP4 ball load supported for this application, you can consider the following:
Output OMAP4 ball load = Far End load + 1.34 pF/cm typical x trace length (cm).

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Table 6-220. JTAG Timing Requirements—Free-running Clock Mode[4][5]

NO.	PARAMETER		OPP100		OPP50		UNIT
			MIN	MAX	MIN	MAX	
JT4	$1 / t_{c(tck)}$	Frequency[1], input clock jtag_tck		20		15	MHz
JT5	$t_{w(tckL)}$	Pulse duration, input clock jtag_tck low	0.5*P[2]		0.5*P[2]		ns
JT6	$t_{w(tckH)}$	Pulse duration, input clock jtag_tck high	0.5*P[2]		0.5*P[2]		ns
	$t_{dc(tck)}$	Duty cycle error, input clock jtag_tck	–2500.0	2500.0	–3333.0	3333.0	ps
	$t_{j(tck)}$	Cycle jitter[3], input clock jtag_tck	–2500.0	2500.0	–3333.0	3333.0	ps
JT7	$t_{su(tdiV-rtckH)}$	Setup time, input data jtag_tdi valid before output clock jtag_rtck high	1.8		9.0		ns
JT8	$t_{h(tdiV-rtckH)}$	Hold time, input data jtag_tdi valid after output clock jtag_rtck high	1.5		2.0		ns
JT9	$t_{su(tmsV-rtckH)}$	Setup time, input mode select jtag_tms_tmsc valid before output clock jtag_rtck high	1.8		9.0		ns
JT10	$t_{h(tmsV-rtckH)}$	Hold time, input mode select jtag_tms_tmsc valid after output clock jtag_rtck high	1.5		2.0		ns

(1) Related to the input maximum frequency supported by the JTAG module.
(2) P = jtag_tck period in ns
(3) Maximum cycle jitter supported by jtag_tck input clock.
(4) The timing requirements are assured for the cycle jitter and duty cycle error conditions specified.
(5) See DM Operating Condition Addendum for CORE OPP voltages.

Table 6-221. JTAG Switching Characteristics—Free-running Clock Mode[4]

NO.	PARAMETER		OPP100		OPP50		UNIT
			MIN	MAX	MIN	MAX	
JT1	$1 / t_{c(rtck)}$	Frequency[1], output clock jtag_rtck		20		15	MHz
JT2	$t_{w(rtckL)}$	Pulse duration, output clock jtag_rtck low	0.5*PO[2]		0.5*PO[2]		ns
JT3	$t_{w(rtckH)}$	Pulse duration, output clock jtag_rtck high	0.5*PO[2]		0.5*PO[2]		ns
	$t_{dc(rtck)}$	Duty cycle error, output clock jtag_rtck	–2500.0	2500.0	–3333.0	3333.0	ps
	$t_{j(rtck)}$	Jitter standard deviation[3], output clock jtag_rtck		33.3		33.3	ps
	$t_{R(rtck)}$	Rise time, output clock jtag_rtck		4.0		4.0	ns
	$t_{F(rtck)}$	Fall time, output clock jtag_rtck		4.0		4.0	ns
JT11	$t_{d(rtckL-tdoV)}$	Delay time, output clock jtag_rtck low to output data jtag_tdo valid	–9.3	12.1	–16.4	16.4	ns
	$t_{R(tdo)}$	Rise time, output data jtag_tdo		4.0		4.0	ns
	$t_{F(tdo)}$	Fall time, output data jtag_tdo		4.0		4.0	ns

(1) Related to the jtag_rtck maximum frequency.
(2) PO = jtag_rtck period in ns
(3) The jitter probability density can be approximated by a Gaussian function.
(4) See DM Operating Condition Addendum for CORE OPP voltages.

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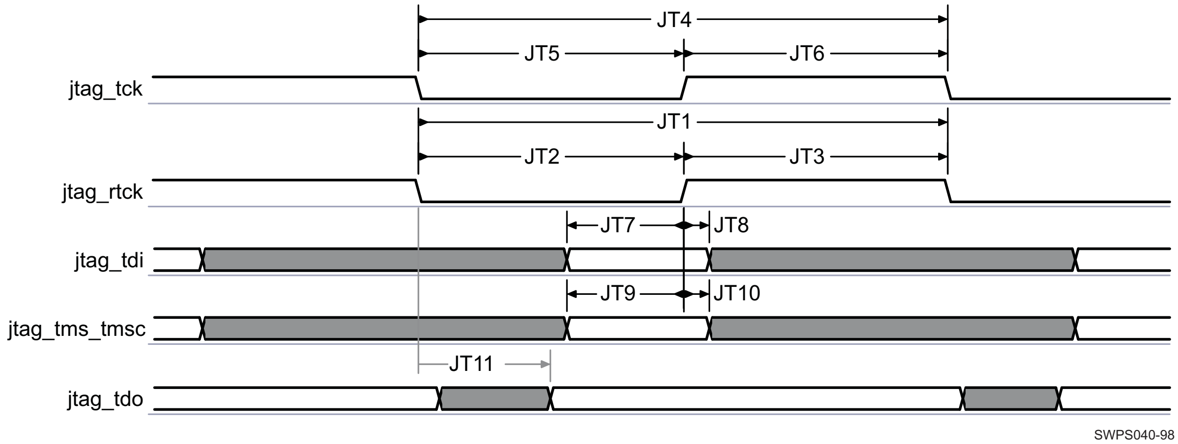

Figure 6-131. JTAG Interface Timing—Free-running Clock Mode

6.8.2.2 JTAG—Adaptive Clock Mode

Table 6-223 and Table 6-224 assume testing over the recommended operating conditions and electrical characteristic conditions below (see Figure 6-132).

Table 6-222. JTAG Timing Conditions—Adaptive Clock Mode(1)(3)(4)

TIMING CONDITION PARAMETER		VALUE		UNIT
		MIN	MAX	
Input Conditions				
t_R	Input signal rise time	5		ns
t_F	Input signal fall time	5		ns
PCB Conditions				
	Number of external peripherals		1	
	Far end load		30	pF
	Trace length		See(2)	cm
	Characteristics impedance	40	60	Ω

(1) Corresponding balls: AH2 / AG1 / AE3 / AH1 / AE1 / AE2

(2) Maximum PCB trace length = 5 cm and maximum cable = 15 cm

(3) For more information on JTAG ESD guideline example, see Section A.3.2.2.3, *ESD Implementation—JTAG and cJTAG Interfaces.*

(4) To have an idea of the output OMAP4 ball load supported for this application, you can consider the following:
Output OMAP4 ball load = Far End load + 1.34 pF/cm typical x trace length (cm).

Table 6-223. JTAG Timing Requirements—Adaptive Clock Mode(4)(5)

NO.	PARAMETER		OPP100		OPP50		UNIT
			MIN	MAX	MIN	MAX	
JA4	$1 / t_{c(tck)}$	Frequency(1), input clock jtag_tck		20		15	MHz
JA5	$t_{w(tckL)}$	Pulse duration, input clock jtag_tck low	0.5*P(2)		0.5*P(2)		ns
JA6	$t_{w(tckH)}$	Pulse duration, input clock jtag_tck high	0.5*P(2)		0.5*P(2)		ns
	$t_{dc(lclk)}$	Duty cycle error, input clock jtag_tck	–2500.0	2500.0	–3333.0	3333.0	ps
	$t_{j(lclk)}$	Cycle jitter(3), input clock jtag_tck	–1500.0	1500.0	–2000.0	2000.0	ps
JA7	$t_{su(tdiV-tckH)}$	Setup time, input data jtag_tdi valid before input clock jtag_tck high	13.8		18.4		ns
JA8	$t_{h(tdiV-tckH)}$	Hold time, input data jtag_tdi valid after input clock jtag_tck high	13.8		18.4		ns
JA9	$t_{su(tmsV-tckH)}$	Setup time, jtag_tms valid before jtag_tck high	13.8		18.4		ns

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Table 6-223. JTAG Timing Requirements—Adaptive Clock Mode[4][5] (continued)

NO.	PARAMETER		OPP100		OPP50		UNIT
			MIN	MAX	MIN	MAX	
JA10	$t_{h(tmsV-tckH)}$	Hold time, jtag_tms valid after jtag_tck high	13.8		18.4		ns

(1) Related to the input maximum frequency supported by the JTAG module.
(2) P = jtag_tck period in ns
(3) Maximum cycle jitter supported by jtag_tck input clock.
(4) The timing requirements are assured for the cycle jitter and duty cycle error conditions specified.
(5) See DM Operating Condition Addendum for CORE OPP voltages.

Table 6-224. JTAG Switching Characteristics—Adaptive Clock Mode[4]

NO.	PARAMETER		OPP100		OPP50		UNIT
			MIN	MAX	MIN	MAX	
JA1	$1 / t_{c(rtck)}$	Frequency[1], output clock jtag_rtck		20		15	MHz
JA2	$t_{w(rtckL)}$	Pulse duration, output clock jtag_rtck low	0.5*PO[2]		0.5*PO[2]		ns
JA3	$t_{w(rtckH)}$	Pulse duration, output clock jtag_rtck high	0.5*PO[2]		0.5*PO[2]		ns
	$t_{dc(rtck)}$	Duty cycle error, output clock jtag_rtck	–2500.0	2500.0	–3333.0	3333.0	ps
	$t_{j(rtck)}$	Jitter standard deviation[3], output clock jtag_rtck		33.3		33.3	ps
	$t_{R(rtck)}$	Rise time, output clock jtag_rtck		4.0		4.0	ns
	$t_{F(rtck)}$	Fall time, output clock jtag_rtck		4.0		4.0	ns
JA11	$t_{d(rtckL-tdoV)}$	Delay time, output clock jtag_rtck low to output data jtag_tdo valid	–14.6	14.6	–19.7	19.7	ns
	$t_{R(tdo)}$	Rise time, output data jtag_tdo		4.0		4.0	ns
	$t_{F(tdo)}$	Fall time, output data jtag_tdo		4.0		4.0	ns

(1) Related to the jtag_rtck maximum frequency.
(2) PO = jtag_rtck period in ns
(3) The jitter probability density can be approximated by a Gaussian function.
(4) See DM Operating Condition Addendum for CORE OPP voltages.

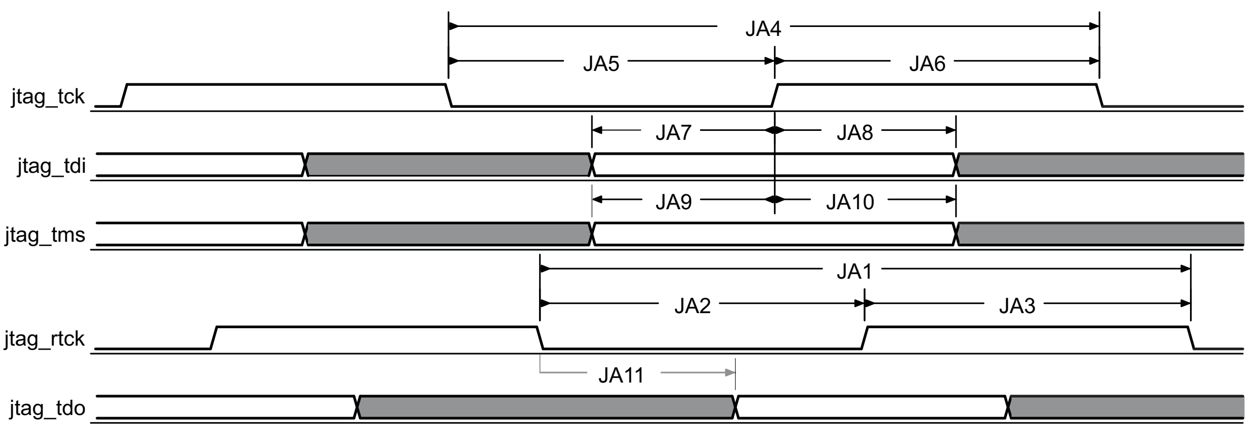

Figure 6-132. JTAG Interface Timing—Adaptive Clock Mode

6.8.3 cJTAG Interface (cJTAG)

The cJTAG module is a component which can run a 2-pin communication protocol on top of an IEEE 1149.1 JTAG Test Access Port (TAP). The cJTAG logic serializes the IEEE 1149.1 transactions, using a variety of compression formats, to reduce the number of pins needed to implement a JTAG debug and boundary scan port. The OMAP4430 platform implements only a basic 3-pin scan configuration.

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Table 6-226 and Table 6-227 assume testing over the recommended operating conditions and electrical characteristic conditions below (see Figure 6-133).

Table 6-225. cJTAG Timing Conditions—Normal Mode(1)(3)(4)

TIMING CONDITION PARAMETER		VALUE		UNIT
		MIN	MAX	
Input Conditions				
t_R	Input signal rise time	2		ns
t_F	Input signal fall time	2		ns
PCB Conditions				
	Number of external peripherals		1	
	Far end load		30	pF
	Trace length		See(2)	cm
	Characteristics impedance	40	60	Ω

(1) Corresponding balls: AH2 / AG1 / AE3 / AH1 / AE1 / AE2

(2) Maximum PCB trace length = 5 cm and maximum cable = 10 cm

(3) For more information on JTAG ESD guideline example, see Section A.3.2.2.3, *ESD Implementation—JTAG and cJTAG Interfaces.*

(4) To have an idea of the output OMAP4 ball load supported for this application, you can consider the following:
Output OMAP4 ball load = Far End load + 1.34 pF/cm typical x trace length (cm).

Table 6-226. cJTAG Timing Requirements—Normal Mode(4)(5)

NO.	PARAMETER		OPP100		OPP50		UNIT
			MIN	MAX	MIN	MAX	
For MMC PADs							
CJ1	$1 / t_{c(tck)}$	Frequency(1), input clock jtag_tck		17.5		14	MHz
CJ2	$t_{w(tckL)}$	Pulse duration, input clock jtag_tck low	0.5*P(2)		0.5*P(2)		ns
CJ3	$t_{w(tckH)}$	Pulse duration, input clock jtag_tck high	0.5*P(2)		0.5*P(2)		ns
	$t_{dc(tck)}$	Duty cycle error, input clock jtag_tck	–2857.0	2857.0	–3571.0	3571.0	ps
	$t_{j(tck)}$	Cycle jitter(3), input clock jtag_tck	–2714.0	2714.0	–3143.0	3143.0	ps
CJ4	$t_{su(tmscV-tckL)}$	Setup time, input mode select jtag_tms_tmsc valid before input clock jtag_tck low	11.4		14.5		ns
CJ5	$t_{h(tmscV-tckL)}$	Hold time, input mode select jtag_tms_tmsc valid after input clock jtag_tck low	4.4		5.5		ns
For JTAG PADs							
CJ1	$t_{c(tck)}$	Frequency(1), input clock jtag_tck		20		19	MHz
CJ2	$t_{w(tckL)}$	Pulse duration, input clock jtag_tck low	0.5*P(2)		0.5*P(2)		ns
CJ3	$t_{w(tckH)}$	Pulse duration, input clock jtag_tck high	0.5*P(2)		0.5*P(2)		ns
	$t_{dc(tck)}$	Duty cycle error, input clock jtag_tck	–2500.0	2500.0	–2632.0	2632.0	ps
	$t_{j(tck)}$	Cycle jitter(3), input clock jtag_tck	–2500.0	2500.0	–2579.0	2579.0	ps
CJ4	$t_{su(tmscV-tckL)}$	Setup time, input mode select jtag_tms_tmsc valid before input clock jtag_tck low	9.8		10.4		ns
CJ5	$t_{h(tmscV-tckL)}$	Hold time, input mode select jtag_tms_tmsc valid after input clock jtag_tck low	3.8		4.0		ns

(1) Related to the input maximum frequency supported by the JTAG module.

(2) P = jtag_tck period in ns

(3) Maximum cycle jitter supported by jtag_tck input clock.

(4) The timing requirements are assured for the cycle jitter and duty cycle error conditions specified.

(5) See DM Operating Condition Addendum for CORE OPP voltages.

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Table 6-227. cJTAG Switching Characteristics—Normal Mode(1)

NO.	PARAMETER		OPP100		OPP50		UNIT
			MIN	MAX	MIN	MAX	
For MMC PADs							
CJ6	$t_{d(tckL-tmscV)}$	Delay time, input clock jtag_tck low to output mode select jtag_tms_tmsc valid	3.4	23.0	4.3	29.7	ns
	$t_{R(tmsc)}$	Rise time, output mode select jtag_tms_tmsc		4.0		4.0	ns
	$t_{F(tmsc)}$	Fall time, output mode select jtag_tms_tmsc		4.0		4.0	ns
For JTAG PADs							
CJ6	$t_{d(tckL-tmscV)}$	Delay time, input clock jtag_tck low to output mode select jtag_tms_tmsc valid	3.0	19.7	3.2	20.9	ns
	$t_{R(tmsc)}$	Rise time, output mode select jtag_tms_tmsc		4.0		4.0	ns
	$t_{F(tmsc)}$	Fall time, output mode select jtag_tms_tmsc		4.0		4.0	ns

(1) See DM Operating Condition Addendum for CORE OPP voltages.

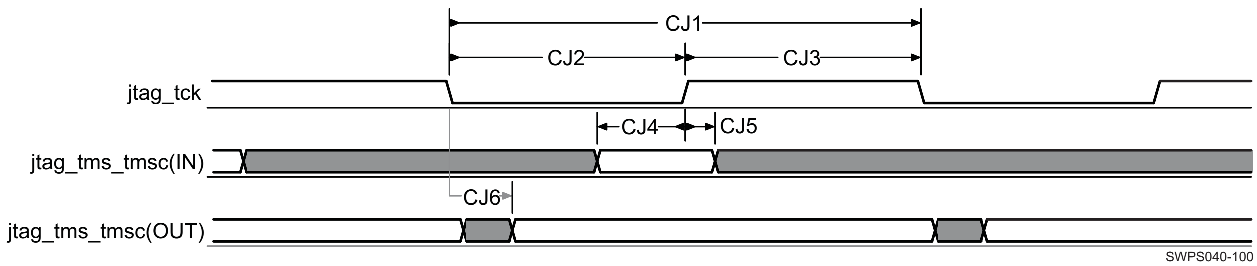

Figure 6-133. cJTAG Interface Timing—Normal Mode

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7 Thermal Management

For reliability and operability concerns, the absolute maximum junction temperature of OMAP4430 has to be below 125ºC and the maximum average junction temperature has to be below 110ºC.

Depending on the thermal mechanical design (Smartphone, Tablet, Personal Navigation Device, etc), the system thermal management software, and worst case thermal application, the junction temperature might be exposed to higher values than those specified above.

Therefore, it is recommended to perform thermal simulations at device level (Smartphone, Tablet, Personal Navigation Device, etc) with the measured power of the worst case UC of the device.

Based on the results, if the temperature limits are exceeded, an OMAP level software thermal policy can be set up; for detailed information, see SWPA184, *OMAP4430 Thermal Management*, application note.

The OMAP level thermal policy relies on a PCB sensor. Therefore, it is recommended to have such sensors located on the PCB; for more information, see Section 7.2, *PCB Sensor Recommendation*. In addition, it is recommended to avoid having another significant thermal source near the OMAP4430.

The risks of not managing this junction temperature are hazardous heating, power supply clamping, reliability issues, and malfunction.

7.1 Package Thermal Characteristics

Table 7-1 provides the thermal resistance characteristics for the package used on this device.

Table 7-1. Thermal Resistance Characteristics

PACKAGE	POWER (W)(4)	θ_{JA}(°C/W)(2)	Ψ_{JB}(°C/W)(3)(4)	BOARD TYPE
OMAP4430	2	22	10	2S2P(1)

(1) The board types are defined by JEDEC (reference JEDEC standard JESD51-9, Test Board for Array Surface Mount Package Thermal Measurements). Note that the board temperature is measured at 1 mm from the package edge.

(2) Θ_{JA} (Theta-JA) = Thermal Resistance Junction-to-Ambient, °C/W.

(3) Ψ_{JB} (Psi-JB) = Thermal Resistance Psi Junction-to-Board, °C/W derived from thermal simulation following JEDEC reference (JEDEC standard JESD51-9, *Test Board for Array Surface Mount Package Thermal Measurements*).

(4) $T_J = P * \Psi_{JB} + T_B$
With P is the dissipated power, T_B = 85°C, T_J = 105°C, dissipated power P = 2 W.

CAUTION

Ψ_{JB} (Psi-JB) value is dependent on the board (PCB) and the power distribution related to the power use case: 10ºC/W is given for a 2-W dissipated power in a JEDEC PCB. Depending on the device power distribution and the PCB, the Ψ_{JB} (Psi-JB) could vary between 9ºC/W and 14ºC/W.

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7.2 Temperature Sensor Recommendation

7.2.1 PCB Temperature Sensor

To manage the OMAP4430 junction temperature, an external PCB temperature sensor is required.

The accuracy of the temperature sensor is critical to optimize the OMAP performance; the minimum recommended accuracy is ±2ºC; see the TI TMP102 temperature sensor component. The temperature sensor can be located at three different positions to correctly monitor the OMAP4430 junction temperature:

- pos 1: 1 mm of the package
- pos 2: 1 mm of the package
- pos 3: On the bottom layer of the PCB, underneath OMAP4430 (top layer) in the center of the package

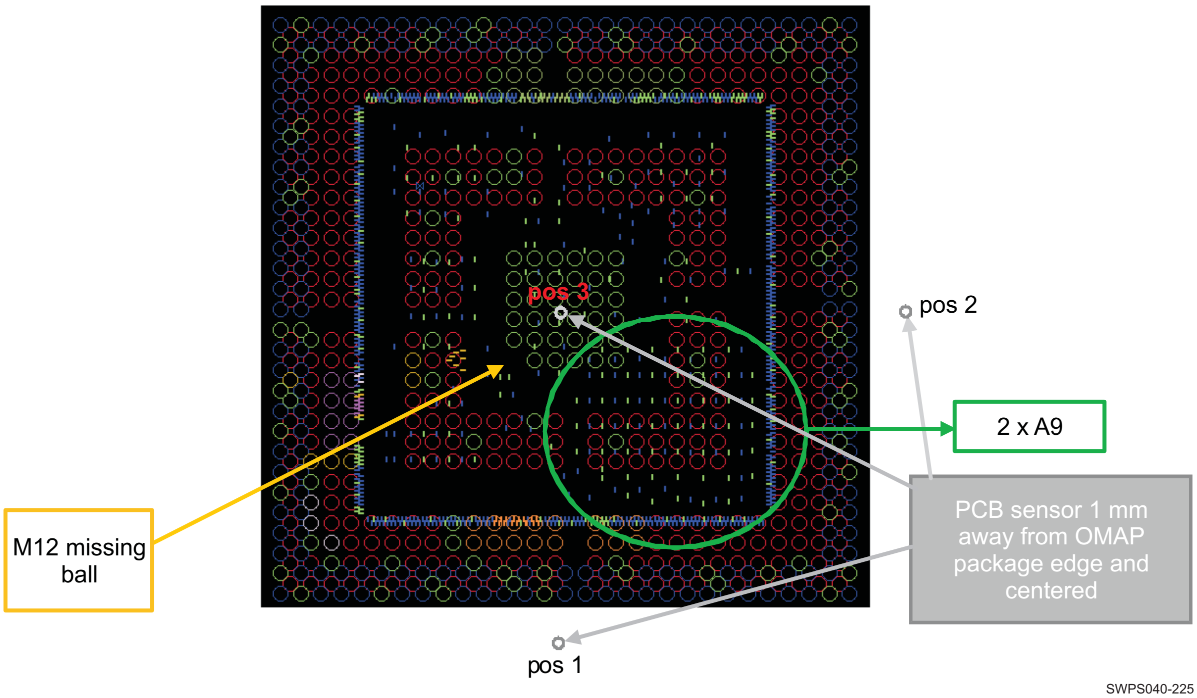

Figure 7-1. PCB Temperature Sensor Recommendation

7.2.2 Junction Temperature Sensor

The OMAP4430 device supplies a temperature sensor feature which is in the band gap voltage and temperature sensor (VBGAPTS) module. An analog-to-digital converter (ADC) converts the silicon temperature into an 8-bit output decimal value.

NOTE

For more information, see Control Module / Control Module Functional Description / Band Gap Voltage and Temperature Sensor / Temperature Sensor section of the OMAP4430 TRM.

Table 7-2 gives the temperature sensor characteristics.

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Table 7-2. Temperature Sensor Characteristics

PARAMETER	MIN	TYP	MAX	UNIT
ADC resolution (DTEMP[7:0])		8		Bit
ADC temperature step		1.5		°C
ADC temperature accuracy for temperature range –40°C to 125°C			±7(1)	°C

(1) The maximum accuracy ±7°C means the worst case of the ADC accuracy.

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8 Package Characteristics

8.1 Device Nomenclature

8.1.1 Standard Package Symbolization

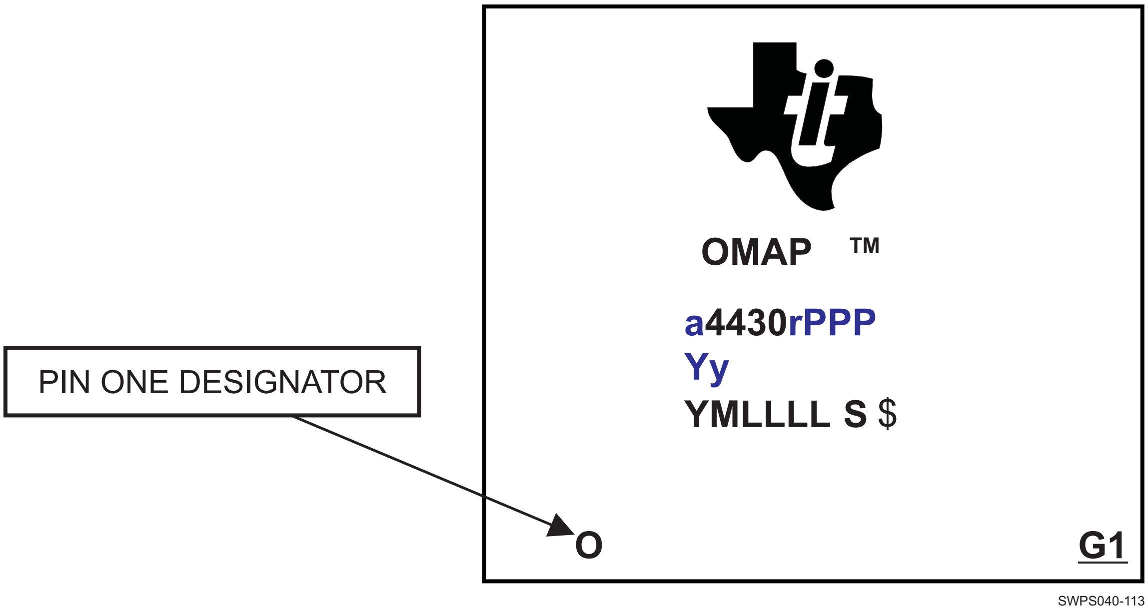

Figure 8-1. Printed Device Reference

NOTE

- Black: Static field
- **Blue**: Variable field coded with letters and/or numbers
- **Green**: Variable fields coded with numbers

The letters and numbers fields are interleaved to facilitate the parameters reading.

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8.1.2 SAP Part Number

The actual part number used in the system follows this syntax (SAP allows a maximum of 14 characters):

- SAP part number in Tray: a**4430**rFZYyPPP
- SAP part number in Tape & Reel: a**4430**rFZYyPPP**R**

8.1.3 Device Naming Convention

Table 8-1. Nomenclature Description

FIELD PARAMETER	FIELD DESCRIPTION	VALUE	DESCRIPTION
a	Qualification status[(1)]	X	Experimental / Prototype / Preproduction / Sample
		BLANK	Qualified / Production device
r	Device revision	SDC	ES1.0
		A	ES2.0
		C	ES2.1
		D	ES2.2
		F	ES2.3
PPP	Package designator	CBL	CBL S-FBGA-N547 (Prototype only)
		CBS	ES2.0 ES2.1 ES2.2 CBS S-FBGA-N547 (Prototype and Production)
A	Reserved	XX	Reserved
Yy	Device type	BLANK	General purpose (Prototype and Production)
		XX	Reserved
Z	Device Speed	2	OMAP4430-1200 (1200 MHz)
		BLANK or 0	OMAP4430-1000 (1000 MHz)
		8	OMAP4430-800 (800 MHz)
YM	Year and month numbers		
LLLL	Assembly lot number		
S	Reserved		
$			
O	Pin one designator		
G1	ECAT—Green package designator		

(1) To designate the stages in the product development cycle, TI assigns prefixes to the part numbers of OMAP 4 processors. These prefixes represent evolutionary stages of product development from engineering prototypes through fully qualified production devices. Device development indicator:

– X : Experimental, preproduction, sample or prototype device. Device may not meet all product qualification conditions and may not fully comply with TI Specifications.
– BLANK: Device is qualified and released to production. TI's standard warranty applies to production devices.

Experimental / Prototype devices are shipped against the following disclaimer: "This product is still in development and is intended for internal evaluation purposes." Notwithstanding any provision to the contrary, TI makes no warranty expressed, implied, or statutory, including any implied warranty of merchantability of fitness for a specific purpose, of this device

NOTE

BLANK in the symbol or part number is collapsed so there are no gaps between characters.

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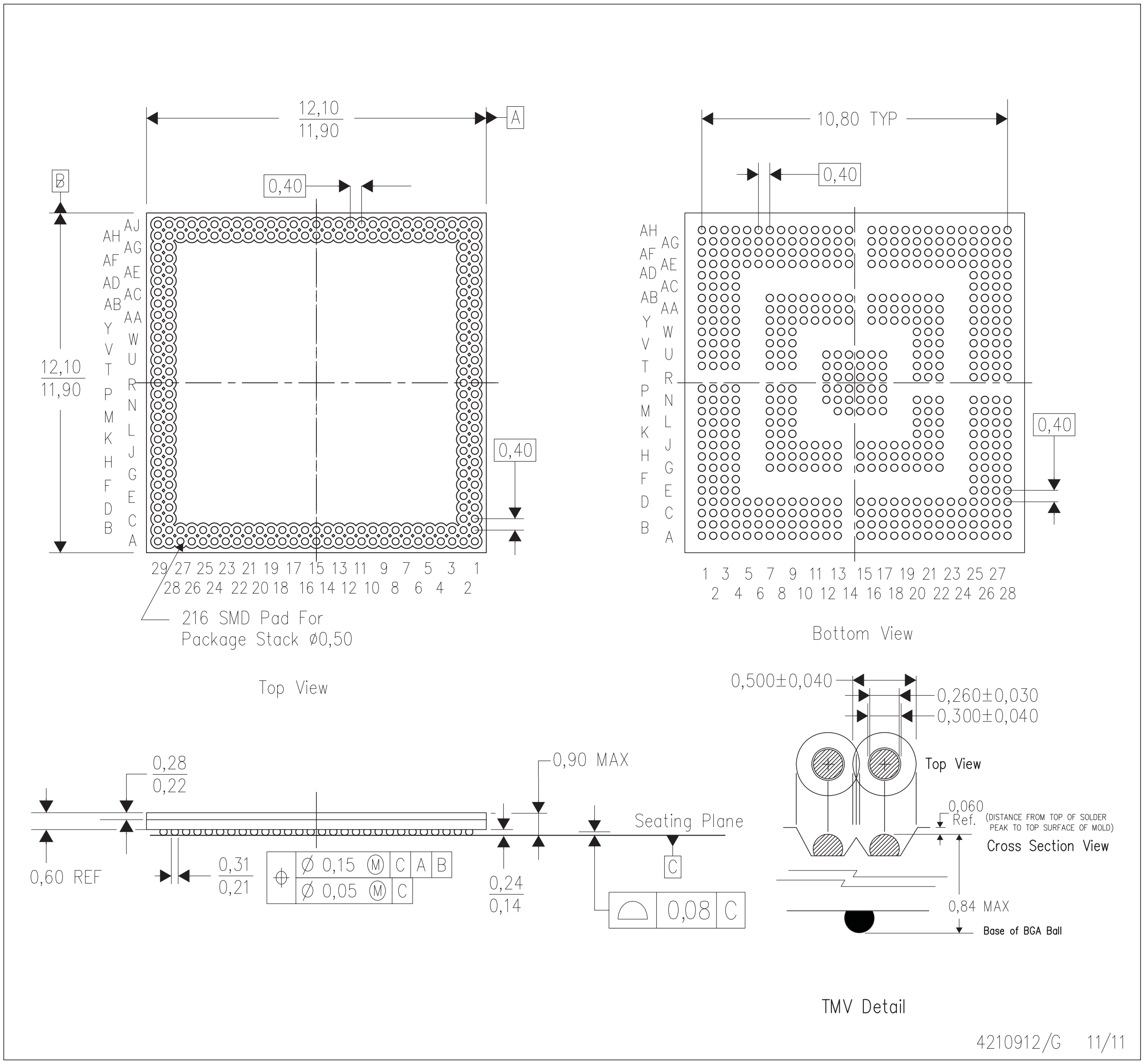
8.2 Mechanical Data

Figure 8-2 shows the mechanical package.

CBS (S–PBGA–N547) TMV PACKAGE PLASTIC BALL GRID ARRAY



NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
- B. This drawing is subject to change without notice.
- C. Flip chip application only.
- D. Pb–free die bump and solder ball.

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Figure 8-2. Production Mechanical Package

A OMAP4430 Processor Multimedia Device PCB Guideline

A.1 Introduction

NOTE

OMAP™ 4 processors are intended for manufacturers of Smartphones and other mobile devices.

NOTE

Notwithstanding any provision to the contrary, TI makes no warranty expressed, implied, or statutory, including any implied warranty of merchantability of fitness for a specific purpose, for customer boards. The data described in this appendix are intended as guidelines only.

This appendix must be used in complement to the OMAP4430 data manual. It provides:

- Guidelines for the design of the PCB focusing first on power delivery network (PDN) implementation which is essential to achieve desired level of performance on OMAP4430 and OMAP4460.
- General principles and step-by-step approach for good PDN implementation and specific requirements for the different power supplies of OMAP4.
- Methodology and requirements to meet the PCB routing of OMAP4430 differential interfaces (MIPI CSI and DSI, USB and HDMI) and TV-OUT interface.
- PCB requirements for general purposes interface using CMOS driver to meet timing requirements and minimize overshoot-undershoot at the far end peripheral.

A.2 Initial Requirements and Guidelines

A.2.1 Introduction to the PCB Guidelines

The recommendation for board stackup is an 8-layer design in either 2+x+2 or 3+x+3 where x represents the number of core layers with 2 or 3 build-up layers depending upon number of signals routed on PCB.

Table A-1. PCB Stackup—8 Layers

PCB STACK-UP 2+4+2		THICKNESS (µm)	PCB STACK-UP 3+2+3		THICKNESS (µm)
Layer 1 (top)	Signal	20	Layer 1 (top)	Signal	20
Dielectric		70	Dielectric		70
Layer 2	GND plane	20	Layer 2	GND plane	20
Dielectric		70	Dielectric		70
Layer 3	Signal	30	Layer 3	Signal	20
Dielectric		100	Dielectric		70
Layer 4	Signal	30	Layer 4	Signal	30
Dielectric		100	Dielectric		200
Layer 5	PWR plane	30	Layer 5	PWR plane	30
Dielectric		100	Dielectric		70
Layer 6	Signal / GND	30	Layer 6	Signal / GND	20
Dielectric		70	Dielectric		70
Layer 7	Signal	20	Layer 7	Signal	20
Dielectric		70	Dielectric		70
Layer 8	Signal / GND	20	Layer 8	Signal / GND	20
Total (µm)		780	**Total (µm)**		800

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The 10-layer implementation can be considered as well in case of requirements for small PCB form factors.

Table A-2. PCB Stackup—10 Layers

PCB STACK-UP 3+4+3		THICKNESS (µm)
Layer 1 (top)	Signal	20
Dielectric		70
Layer 2	GND plane	20
Dielectric		70
Layer 3	Signal	20
Dielectric		70
Layer 4	Signal	30
Dielectric		100
Layer 5	PWR plane	30
Dielectric		100
Layer 6	GND plane	30
Dielectric		100
Layer 7	Signal	30
Dielectric		70
Layer 8	Signal	20
Dielectric		70
Layer 9	Plane	20
Dielectric		70
Layer 8 (Bottom)	Signal	20
Total (µm)		960

- The power delivery network (PDN) must be optimized for low trace resistance and low trace inductance between the power management IC (PMIC) and OMAP4 especially for vdd_mpu, vdd_iva_audio, and vdd_core power supplies (ranked by order of criticality per their respective peak currents)
- Optimize routing power routing between vdd_mpu and the PMIC.
- OMAP4430-1000, OMAP4430-800, and OMAP4460 devices have different peak currents for vdd_mpu. Hence, specific PDN must be designed for vdd_mpu. For more information on OMAP4460 PCB guideline, see the OMAP4460 ES1.0 data manual, Appendix A, *OMAP4460 Processor Multimedia Device PCB Guideline*.
- It is highly recommended to run board frequency domain analysis on vdd_mpu, vdd_iva_audio, and vdd_core power supplies to check if proper board decoupling is implemented and confirm that respective target impedances are met. For more information on target impedance, see Section 3.4, *External Capacitors*.
- Characteristic impedance for single-ended interfaces is recommended to be between 30 Ω and 60 Ω and in some specific cases between 40 Ω and 55 Ω to minimize overshoot and undershoot on far end loads.

  For more information see Section A.3, *Single-Ended Interfaces*.
- Characteristic impedance for single-ended interfaces must meet 50-Ω (±10%) and 100-Ω differential impedance.

  For more information see Section A.4, *Differential Interface PCB Guidelines*.
- Characteristic impedance for TVOUT (cvideo_tvout) node of video DAC interface needs to be 75 Ω (±10%).

  For more information see Section A.5, *TVOUT Interface in OMAP4*, or Section 5, *Video DAC Specifications*.

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- External interface using connector must be protected following the IEC61000-4-2 level 4 system ESD (±8 kV in contact mode or ±15 kV air discharge mode).

  See also the respective sections of USBA0 PHY (Section A.4.4.3, *ESD Implementation—USBA0 PHY*), HDMI (Section A.4.5, *HDMI Interface in OMAP4*), Video DAC (Section A.5.3, *ESD Implementation—TVOUT*), SDMMC1 (Section A.3.2.2.1, *ESD Implementation—MMC/SD/SDIO 1 Interface—SD Mode*), Keypad (Section A.3.2.2.2, *ESD Implementation—KeyPAD Interface*) and JTAG or cJTAG (Section A.3.2.2.3, *ESD Implementation—JTAG and cJTAG Interfaces*) interfaces for specific ESD requirements and implementation proposals.
- LPDDR2 memory:
  - OMAP4 supports two LPDDR2 channels. Each of these channels supports up to two chip selects. Up to four LPDDR2 memory dies can be connected on top of OMAP4 package via Package-on-Package implementation. Powers for LPDDR2 memory are connected via feedthrough in OMAP4430 package.
  - The memory component LPDDR2-S4A and LPDDR2-S4B memory have different voltage requirements. The S4B type needs a single 1.2-V source to supply vdd2 and vddq/vddca.

A.2.2 PCB Power General Routing Guidelines

In this section you will find the necessary steps for the PCB power general routing:

- **Section A.2.2.1, Step 1:** Requirements and guidelines for PCB stack-up
- **Section A.2.2.2, Step 2:** Physical layout guidelines of the PDN
- **Section A.2.2.3, Step 3:** Static IR drop guidelines of PDN. Minimize resistance, avoid neck-down, and reduce current density.

A.2.2.1 Step 1: PCB Stack-up Guidelines

The PCB stack-up (layer assignment) is an important factor in determining the optimal performance of the power distribution system. An optimized PCB stack-up for higher power integrity performance can be achieved by following these requirements:

- Power and ground plane pairs must be closely coupled together. The capacitance formed between the planes can decouple the power supply at high frequencies. Whenever possible, the power and the ground planes must be solid to provide continuous return path for return current.
- Use a thin dielectric thickness between the power and ground plane pair. Capacitance is inversely proportional to the separation of the plane pair. Minimizing the separation distance (the dielectric thickness) will maximize the capacitance.
- Keep the power and ground plane pair as close as possible to the TOP and BOTTOM surfaces (see Figure A-1). This will help in minimizing the decoupling capacitors mounting, via, and the power/ground plane pair spreading loop inductance.

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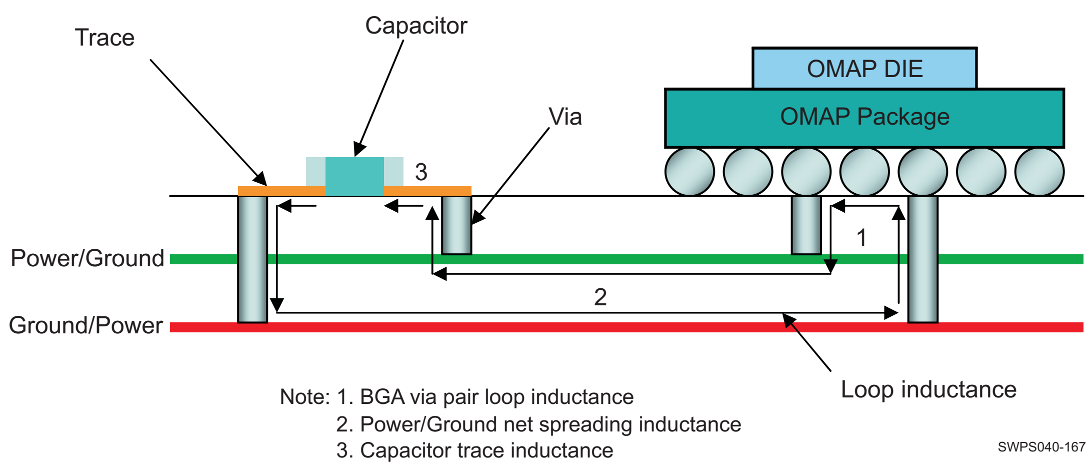

Figure A-1. Minimize Loop Inductance With Proper Layer Assignment

The placement of power and ground planes in the PCB stackup (determined by layer assignment) has a significant impact on the parasitic inductances of power current path as shown in Figure A-1. For this reason, it is recommended to consider layer order in the early stages of the PCB PDN design cycle, putting high priority supplies in the top half of the stackup and low-priority supplies in the bottom half of the stackup as shown in the examples below (vias have parasitic inductances which impact the bottom layers more, so it is advised to put the sensitive and high priorities power supplies on the top layers).

Figure A-2 and Figure A-3 show examples of typical PCB stack-up designed with power integrity in mind.

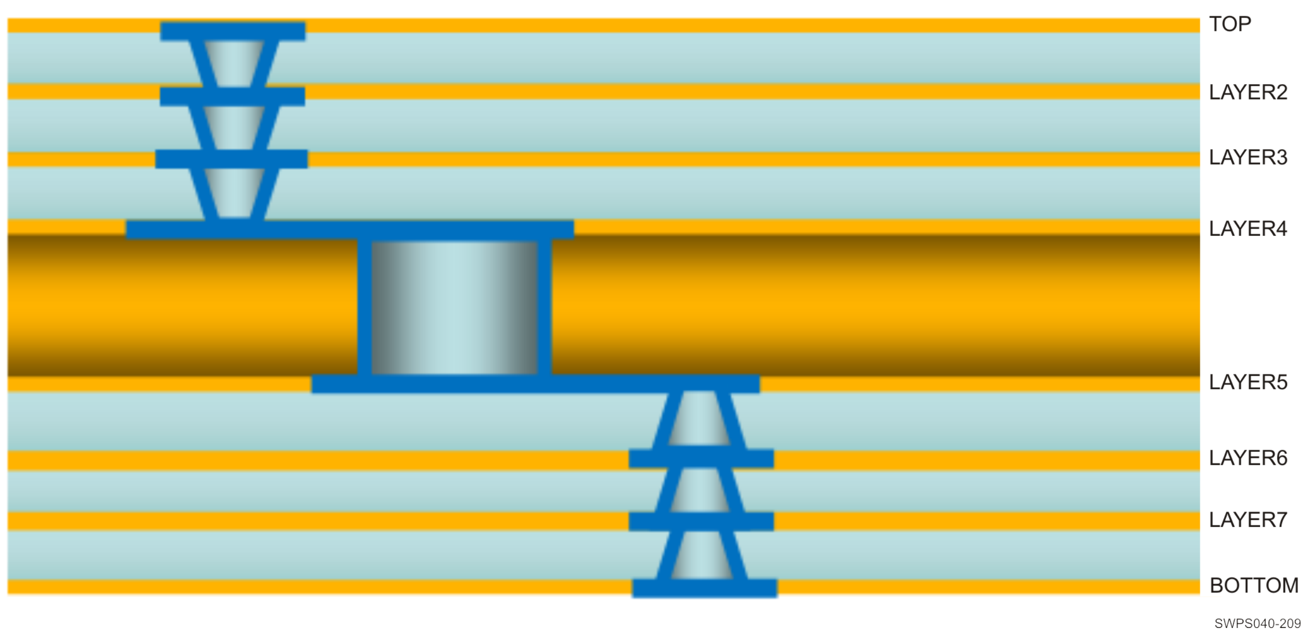

Figure A-2. Layer PCB With High Density Interconnect (HDI) Vias(1)

(1) Recommendation:
- GND on layer 2
- The signal escape on layer 3 and layer 4, PWR on layer 5

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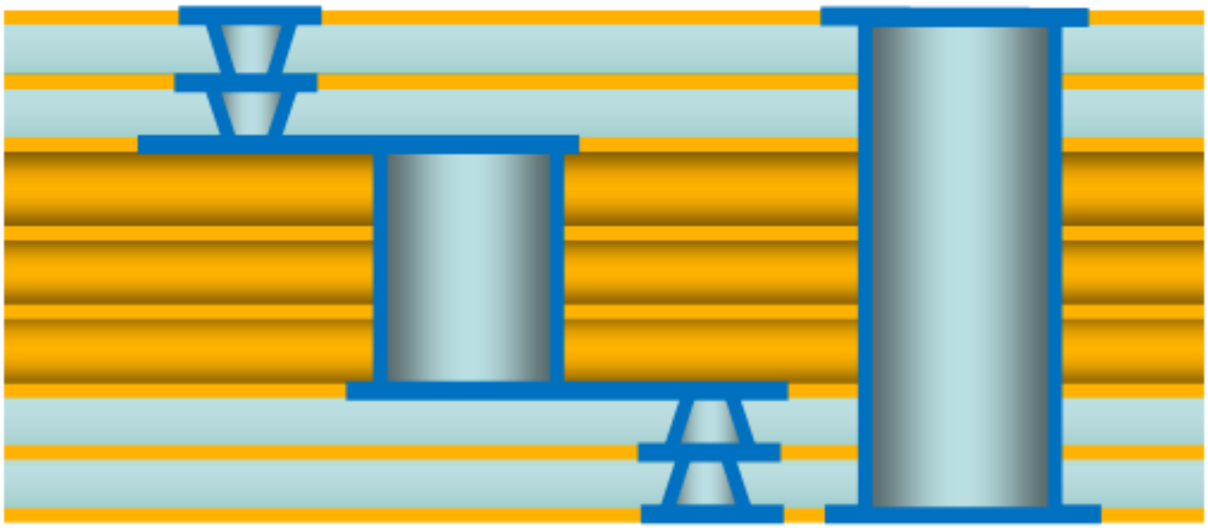

Figure A-3. Layer PCB With Plated Though Holes (PTH) Vias(1)

(1) 2-4-2 PCB only possible if the interfaces number is reduced.
Recommendation:
- GND on layer 2
- Signal escape on layer 3 and layer 4, PWR on layer 5

A.2.2.2 Step 2: Physical Layout Guidelines of the PDN

A critical step in designing an optimized PDN is that proper care must be taken to making sure that the initial layout is done with good power integrity design guidelines in mind. The following points are important requirements that will be needed to be implemented in the PCB PDN design:

- External trace routing between components must be as wide as possible. The wider the traces the lower the dc resistance and consequently the lower the static IR drop.
- Whenever possible, try aiming for a ratio of 1:1 or better for component (for example, capacitors and resistors) pins and vias. Do not share vias among multiple capacitors.
- Placement of the vias must be as close as possible to the solder pad.

Figure A-4 shows an example of acceptable width for power net routing but with poor via placement.

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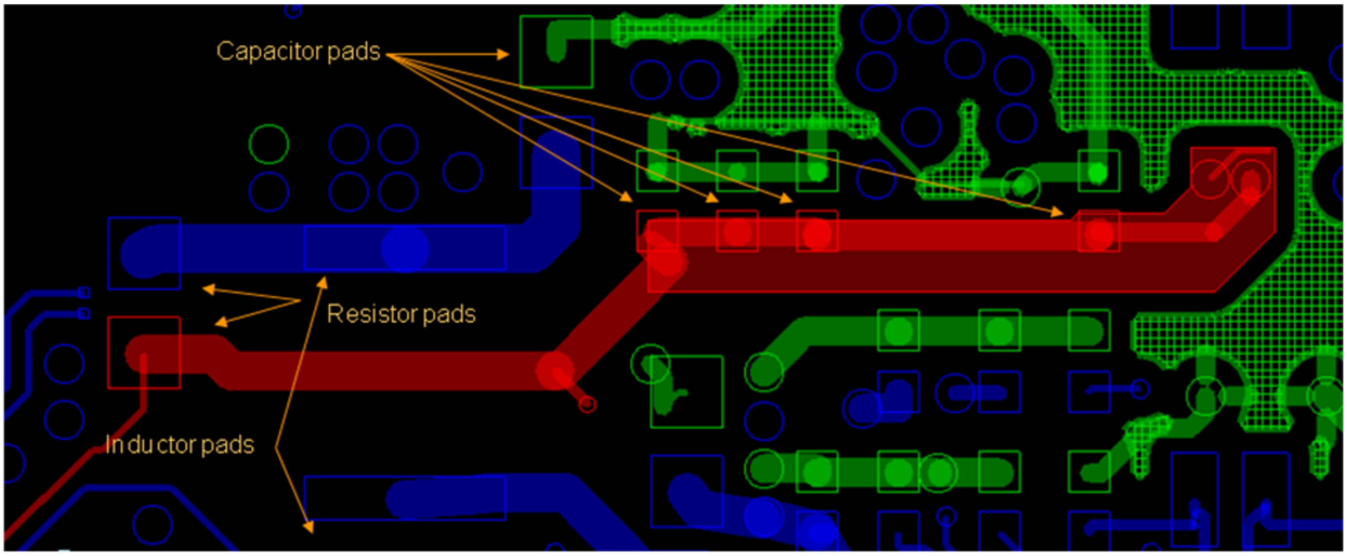

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Figure A-4. Poor Via Assignment for PDN

Figure A-5 shows an improved power net routing with appropriate via assignment and placement respectively.

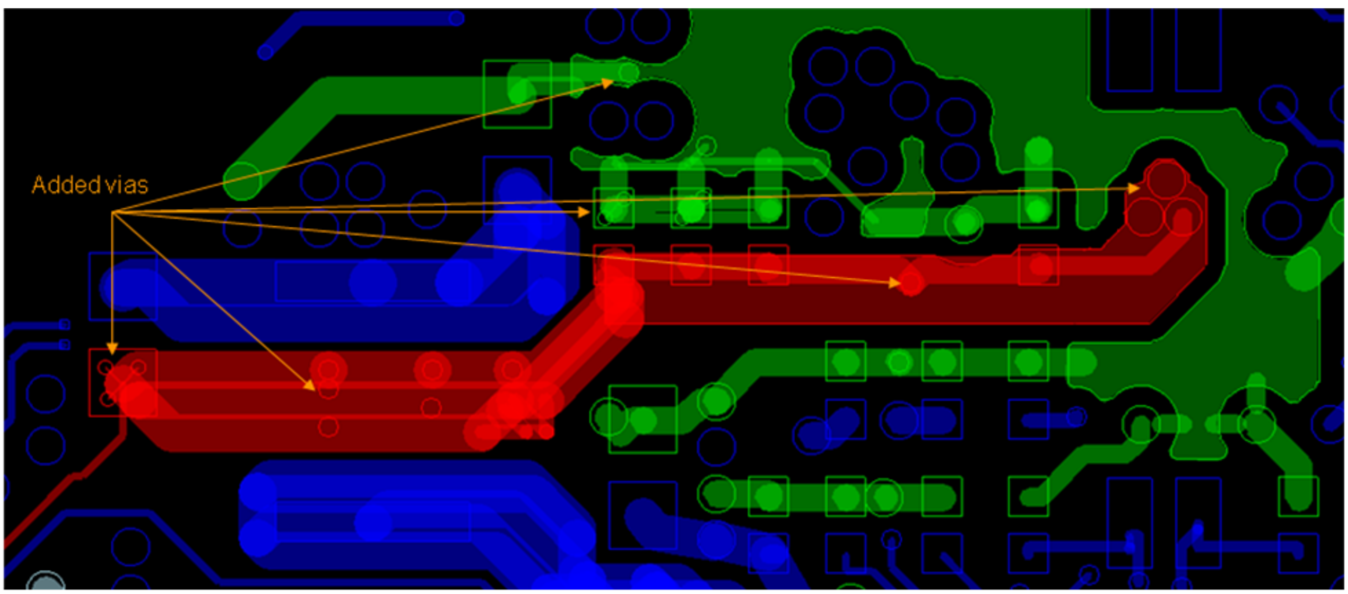

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Figure A-5. Improved Via Assignment for PDN

- To avoid the maximum current carrying capacity of each transitional via, an evaluation must be performed to determine the appropriate number of vias required to connect components.

  Figure A-6 and Figure A-7 show examples of via starvation on a power net transitioning from top routing layer to internal layers and the improved layout, respectively.

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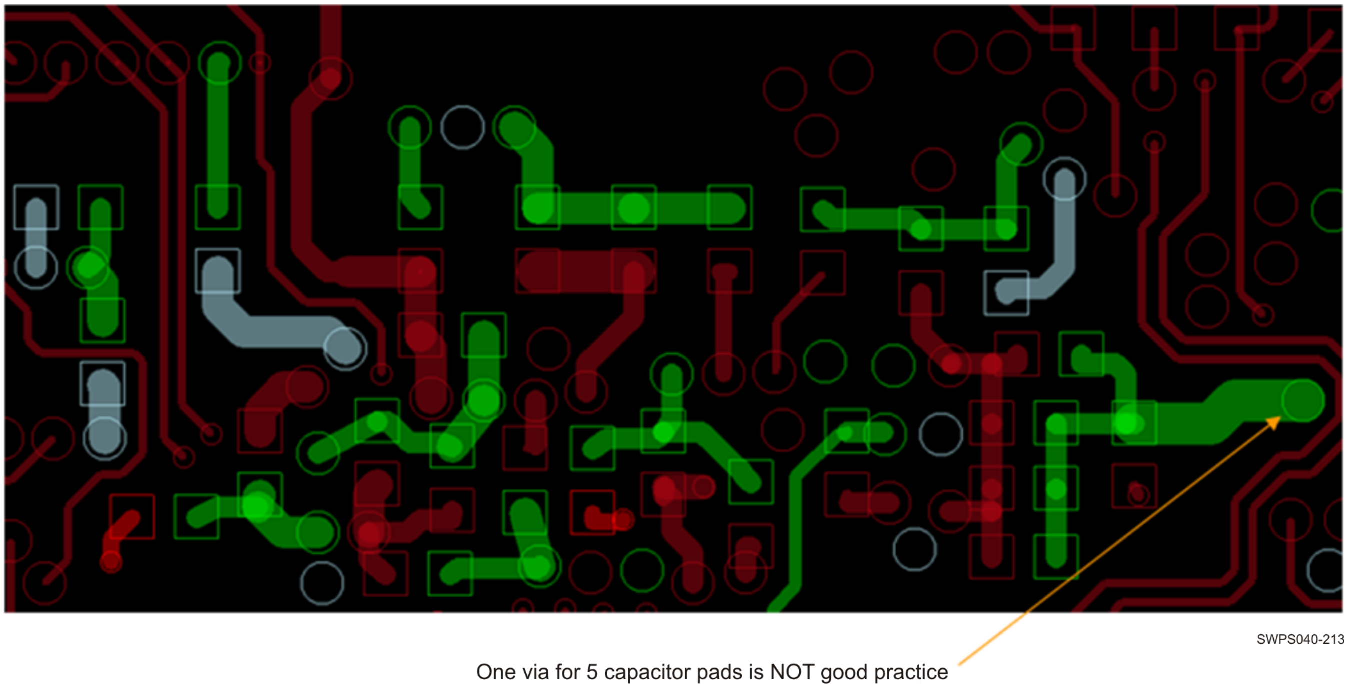

Figure A-6. Via Starvation

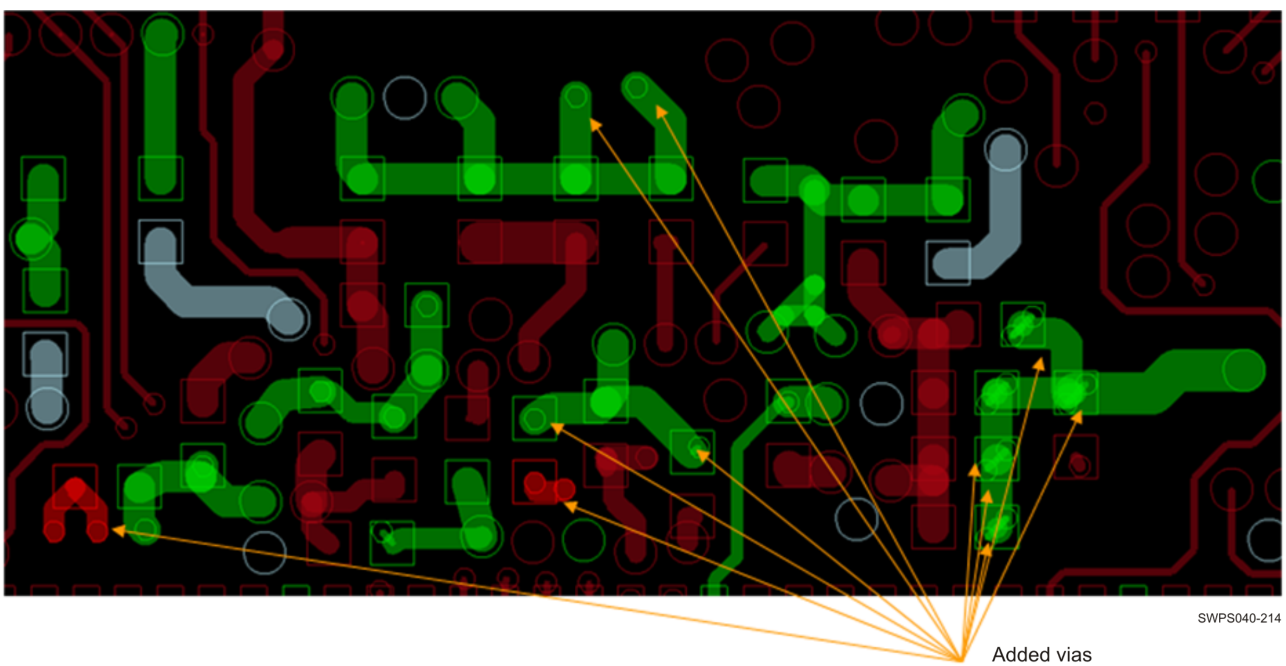

Figure A-7. Improved Layout With More Transitional Vias

- It is also a good practice to perform static IR drop. This analysis can assess the appropriate number of vias and geometrical trace width dimensions required for expected IR drop requirement.
- Whenever possible for the internal layers (routing and plane), wide traces and copper area fills are preferred for PDN layout. The routing power nets in plane provide for more interplane capacitance and improve high frequency performance of the PDN.

- Try to avoid different power nets (for example, VDD_MPU with VDD_CORE) coupling on the PCB by using coplanar shielding whenever appropriate.

  Figure A-8 represents an example of coplanar shielding for power nets.

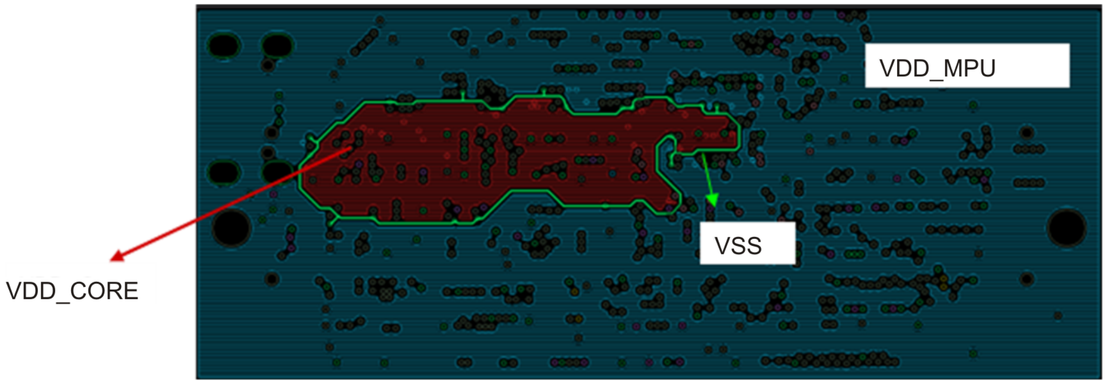

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Figure A-8. Coplanar Shielding of Power Net Using Ground Guard-band

- Decoupling capacitors must be mounted with minimum impact to inductance. A real capacitor has characteristics not only of capacitance but also inductance and resistance.

  Figure A-9shows the parasitic model of a real capacitor. A real capacitor must be treated as an RLC circuit with effective series resistance (ESR) and effective series inductance (ESL).

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Figure A-9. Characteristics of a Real Capacitor With ESL and ESR

The magnitude of the impedance of this series model is given as:

$$|Z| = \sqrt{ESR^2 + \left(\omega ESL - \frac{1}{\omega C}\right)^2}$$

$$\text{where: } \omega = 2\pi f$$

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Figure A-10. Series Model Impedance Equation

Figure A-11 shows the resonant frequency response of a typical capacitor with self-resonant frequency of 55 MHz. The impedance of the capacitor is a combination of its series resistance and reactive capacitance and inductance as shown in the equation above.

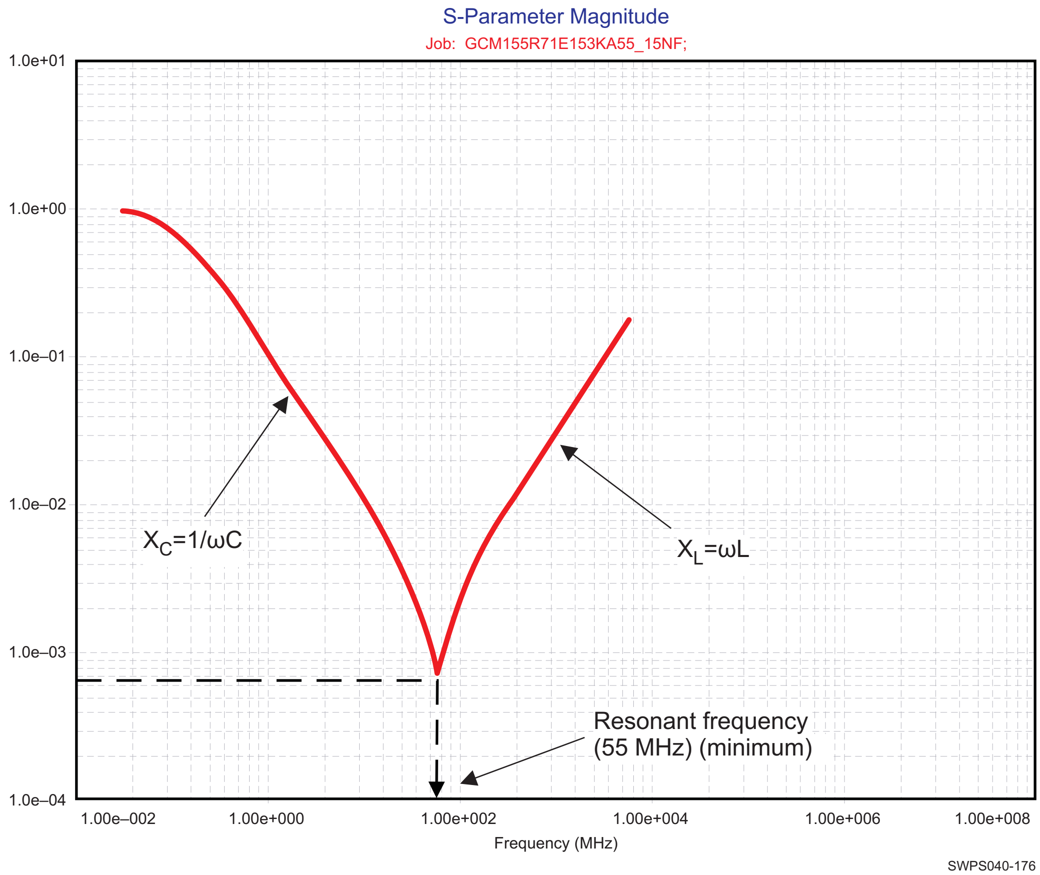

Figure A-11. Typical Impedance Profile of a Capacitor

Since a capacitor has series inductance and resistance that will impact its effectiveness, it is important that the following recommendations are adopted in placing them on the power distribution network. Whenever possible, please mount the capacitor with the geometry that will minimize the mounting inductance and resistance. This was shown earlier in Figure A-1. The capacitor mounting inductance and resistance here includes the inductance and resistance of the pads, trace, and vias.

The length of a trace use to connect a capacitor has a big impact on parasitic inductance and resistance of the mounting. This trace must be as short and wide as possible. Wherever possible, minimize the trace by locating vias near the solder pad landing. Further improvements can be made to the mounting by placing vias to the side of capacitor lands or doubling the number of vias as shown in Figure A-12. If the PCB manufacturing processes allow and if cost-effective, via-in-pad (VIP) geometries are strongly recommended.

In addition to mounting inductance and resistance associated with placing a capacitor on the PCB, the effectiveness of a decoupling capacitor also depends on the spreading inductance and resistance that the capacitor sees with respect to the load. The spreading inductance and resistance is strongly dependent on the layer assignment in the PCB stack-up (as shown in Figure A-2).

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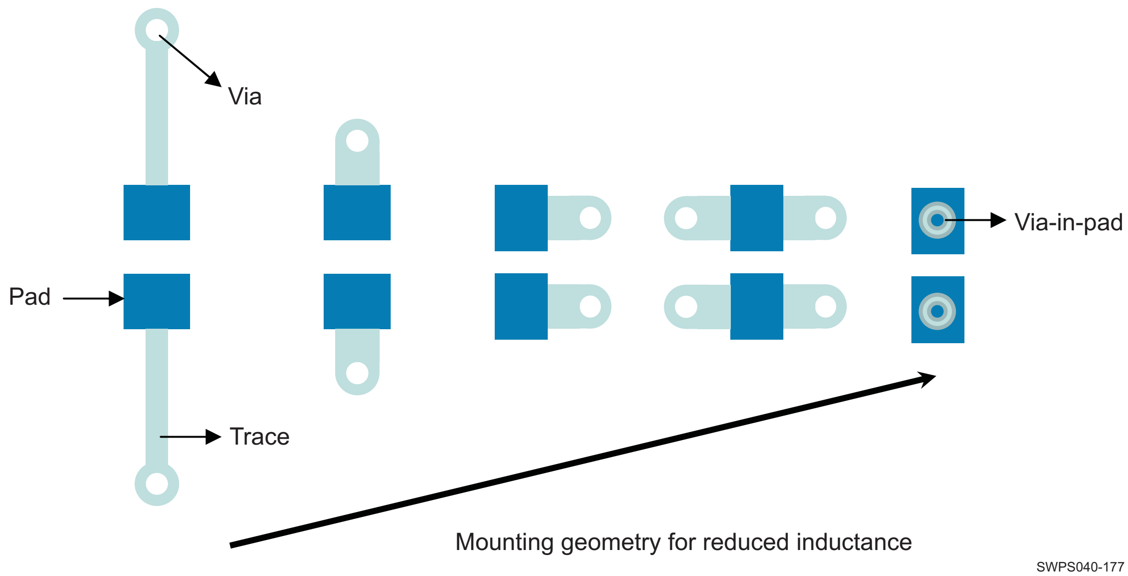

Figure A-12. Capacitor Placement Geometry for Improved Mounting Inductance

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A.2.2.3 Step 3: Static IR Drop PDN Guidelines

Delivering reliable power to circuits is always a critical importance because IR drops can happen at every level in a chip, package, and board system. Components that are distant from their associated power source are particularly susceptible to IR drop. The designs that rely on battery power must minimize voltage drop to avoid unacceptable power loss. Early dc assessments help determine power distribution basics such as the best available entry point for power, layer stackup choices, and estimates for the amount of copper needed to carry the current.

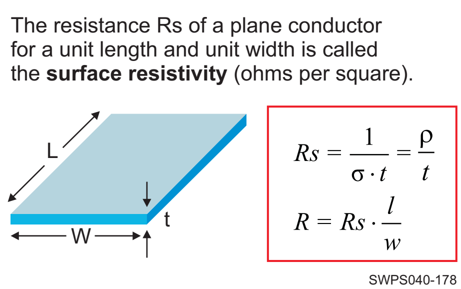

Figure A-13. Depiction of Sheet Resistivity and Resistance

Ohm's Law (V = I * R) relates conduction current to voltage drop and at dc the relation coefficient is a constant representing the resistance of the conductor. Conductors also dissipate power due to their resistance. Both voltage drop and power dissipation are proportional to the resistance of the conductor.

System-level IR drop budget is made up of three portions: on-chip, package and PCB board. Static IR or dc analysis/design methodology consists of designing the power distribution network such that the voltage drop (under dc operating conditions) across power and ground pads of the transistors of the application processor device is within a specified value of the nominal voltage for proper functionality of the device.

Figure A-14 shows the PCB-level static IR drop budget is defined between the pins of the power management device PMIC/VRM and the BGA pads on the PCB to the application processor device to which the PMIC is supplying power.

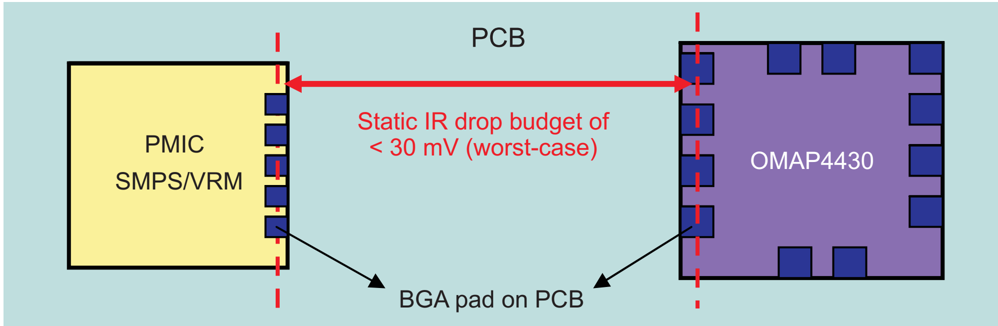

Figure A-14. Static IR Drop Budget for PCB Only

The total system-level margin allowed for proper device functionality is given, allowable voltage variation at the BGA of the device is specified at 1.5% of the nominal voltage. For a 1.35-V supply, this must be ≤20 mV.

It is highly recommended to connect the VRM or the PMIC as close as physically possible on the PCB to the OMAP4430 device.

To accurately analyze PCB static IR drop, the actual geometry of the PDN must often be properly modeled and simulated to accurately characterize long distribution paths, low weight copper, electro-migration violations of current-carrying vias, and swiss-cheese effects. It is recommended to perform the following analyses:

1. Lumped resistance/IR drop analysis
2. Distributed resistance/IR drop analysis

The requirements are present to perform both analyses and to show compliance. In the following sections each methodology is described in detail and examples provided of analysis flow that can be used by the PCB designer to validate compliance to the requirements on their PCB PDN design.

A.2.3 Lumped and Distributed Resistance/IR Drop Analysis Methodology

Lumped methodology consists of grouping all of the power/ground pins of the PMIC and the processor device; this is followed by extracting the lumped resistance or dc voltage drop of the equivalent path by applying a voltage source at the PMIC end and a current sink at the device end. Figure A-15 describes the pin-grouping concept.

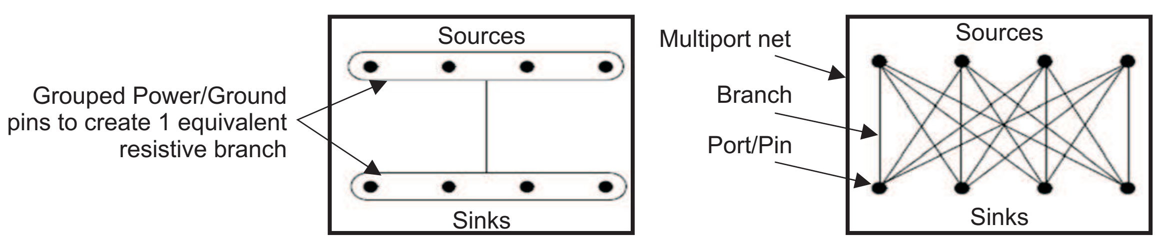

Figure A-15. Pin-grouping Concept: Lumped and Distributed Methodologies

The lumped methodology consists of importing the PCB layout database (from Cadence Allegro tool or any other layout design tool) into the static IR drop modeling and simulation tool of preference for the PCB designer. This is followed by applying the correct PCB stack-up information (thickness, material properties) of the PCB dielectric and metallization layers. The material properties of dielectric consist of permittivity (Dk) and loss tangent (Df).

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For the conductor layers, the correct conductivity needs to be programmed into the simulation tool. This is followed by pin-grouping of the power and ground nets, and applying appropriate voltage/current sources.

The current and voltage information can be obtained from the power and voltage specifications of the device under different operating conditions / use-modes. After running the simulation, the lumped resistance and lumped IR drop can be examined as shown in Figure A-15.

A.2.4 System ESD Generic Guidelines

NOTE

IEC61000-4-2: The ESD discharges described in this section apply only to HDMI, USBA0 PHY, SD/MMC card cage, composite video, JTAG, cJTAG, and points and surfaces of the Equipment Under Test (EUT) that are accessible to the end-user during normal use.

The following exclusions apply (that is, discharges are not applied to these items):

- In the case of the contacts of coaxial and multipin connectors which are provided with a metallic connector shell, contact discharges are only applied to the metallic shell contacts. Falling into this category:

  HDMI/USB connectors, SD/MMC card cage, audio headset jack connector
- Those points and surfaces which are only accessible under service by the end-user. Examples of these rarely accessed points are battery contacts while changing batteries. Falling into this category:

  Battery connector
- Those points and surfaces which are only accessible under maintenance. In this case, special ESD mitigation procedures are given in the accompanying documentation. Falling into this category:

  JTAG test points
- Those points and surfaces of equipment which are no longer accessible after fixed installation or after following the instructions for use, for example, the bottom and/or wall side of equipment or areas behind fitted connectors. Potentially falling into this category:

  Audio speaker spring contacts

A.2.4.1 IEC61000-4-2 Standard Overview—System ESD

System ESD differs from the usual component level ESD tests such as HBM (ANSI/ESDA/JEDEC JS-001-2010) or CDM (JESD22 C101) described in Table 3-1, *Absolute Maximum Ratings.* HBM and CDM are tests to evaluate product robustness to ESD events in the manufacturing environment. System ESD is designed to evaluate events that occur when the end-users interact with the final product as they use it. IEC 61000-4-2 is one of the major system level standards used to qualify products for human contact. Sometimes these events are referred to as EMC immunity events.

The standard defines immunity requirements for ESD which can be coupled into the equipment directly (contact discharge) or indirectly through radiation .The charging model is defined with a discharging 150-pF capacitor through a 330-Ω resistor. Direct coupling includes any user accessible entry points such as external connectors, keypad, panel displays, equipment housings, etc.

The ESD stress level is divided into four levels. Level 1 is considered the least severe while Level 4 is the most severe. IEC 61000-4-2 also specifies the ESD current waveform and parameters shown in Figure A-16 and Table A-3. The rise time is extremely fast, defined as 0.7 to 1 ns to reach the first peak, with a second peak at 30 ns and a total duration of only 60 ns.

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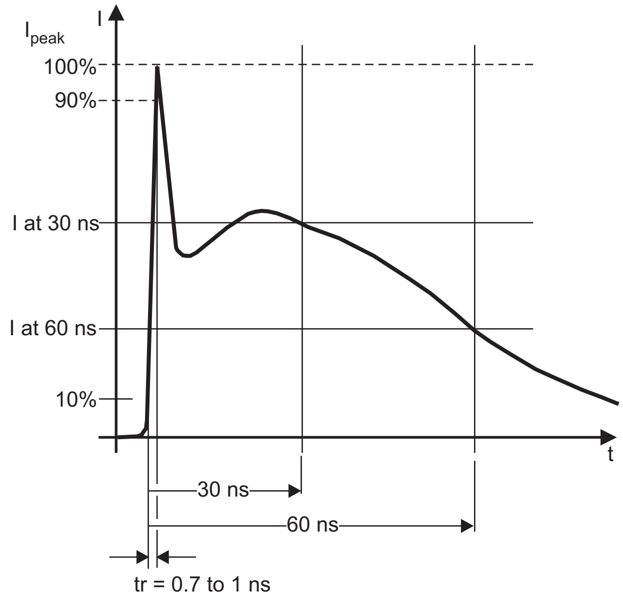

Figure A-16. IEC61000-4-2 Waveform

Table A-3. Waveform Parameters

LEVEL	INDICATED VOLTAGE (kV)	FIRST PEAK CURRENT of DISCHARGE ±10% (A)	RISE TIME, t_R, WITH DISCHARGE SWITCH (ns)	CURRENT (±30%) at 30 ns	CURRENT (±30%) at 60 ns
1	2	7.5	0.7 to 1	4	2
2	4	15	0.7 to 1	8	4
3	6	22.5	0.7 to 1	12	6
4	8	30	0.7 to 1	16	8

Test results are classified in terms of the loss of function or degradation of performance for the system under test .The recommended classification is as follows:

1. Normal performance within limits specified by the manufacturer
2. Temporary loss of function or degradation of performance which ceases after the disturbance ceases, and the system recovers its normal performance without operator intervention
3. Temporary loss of function or degradation of performance, the correction of which requires operator intervention
4. Loss of function or degradation of performance which is not recoverable, due to damage to hardware or software, or loss of data

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A.2.4.2 Objective and Limitation of the Protection Strategy

CAUTION

System level (IEC61000-4-2) ESD results are dependent on the product (Boards and Mechanics) implementation and the components being used. Thus, the protection strategy defined in this document, does not assure to meet IEC61000-4-2 compliance requirement on any final product. Document suggestions must be considered as guidance to help protecting OMAP4430 exposed interfaces against physical damage. Soft failures cannot be simulated and are not accounted for in these recommendations.

The protection strategy is intended to protect against ±8 kV direct contact discharge. The protection strategy is based upon simulations replicating a general board design with an IEC ESD pulse exhibiting the current waveform as defined in Figure A-16, *IEC61000-4-2 Waveform,* and Table A-3, *Waveform Parameters.* External protections, additional isolation resistors, and other passives have been selected or dimensioned accordingly.

Part numbers that are different than the provided reference schematic are not assured to meet system level ESD requirements.

A.2.4.3 Concept of Isolation Impedance

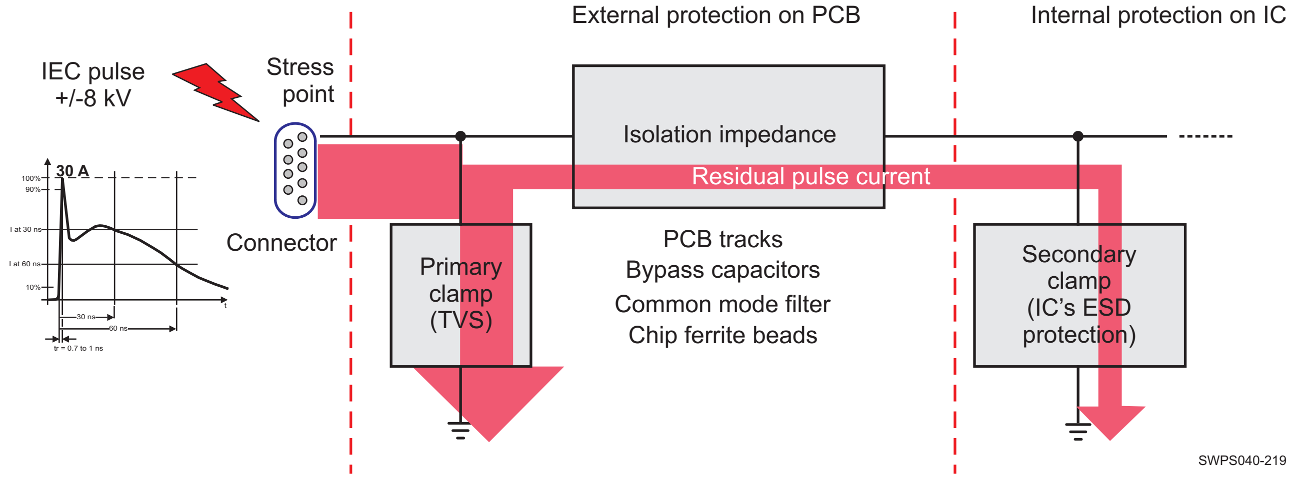

Figure A-17. Simplified Current Distribution

Under an ESD event the external and internal ESD protection turns on and current is distributed between internal and external ESD protection; the distribution ratio being defined, at first order, by the ratio between the dynamic resistances Rdyn of the two protections. To further minimize the current flowing into the internal protection IC, whenever possible (signal integrity constraints), isolation impedance can be increased by taking advantage of the PCB implementation:

- PCB routing track length
- Decoupling capacitor on power supply
- Common mode filter on differential lines
- Chip ferrite bead
- Isolation resistors

A.2.4.4 System ESD Generic PCB Guideline

External interface using a connector must be protected by following the IEC61000-4-2 level 4 system ESD (±8 kV in contact mode or ±15 kV air discharge mode).

Protection devices must be placed close to the ESD source which means close to the connector. This allows the device to subtract the energy associated with ESD strike before it reaches the internal circuitry of the application board.

To help minimize the residual voltage pulse that will be built-up at the protection device, due to its nonzero turn-on impedance, it is mandatory to route the ESD device with minimum stub length so that the low-resistive, low-inductive path from the signal to the ground is granted and not increasing the impedance between signal and ground.

For ESD protection array being railed to a power supply when no decoupling capacitor is available in close vicinity, consider using a decoupling capacitor (≥ 0.1 μF) tight to the VCC pin of the ESD protection. A positive strike will be partially diverted to this capacitance resulting in a lower residual voltage pulse.

Ensure that there is enough metallization for the supply of signals at the interconnect side (VCC and GND in Figure A-18) from connector to external protection because the interconnect may see between 15-A to 30-A current in a short period of time during the ESD event.

NOTE

System level ESD results (IEC61000-4-2 level 4) are dependent on the components being connected to the product.

Part numbers that are different than the reference board specification are not assured to meet system level ESD requirements.

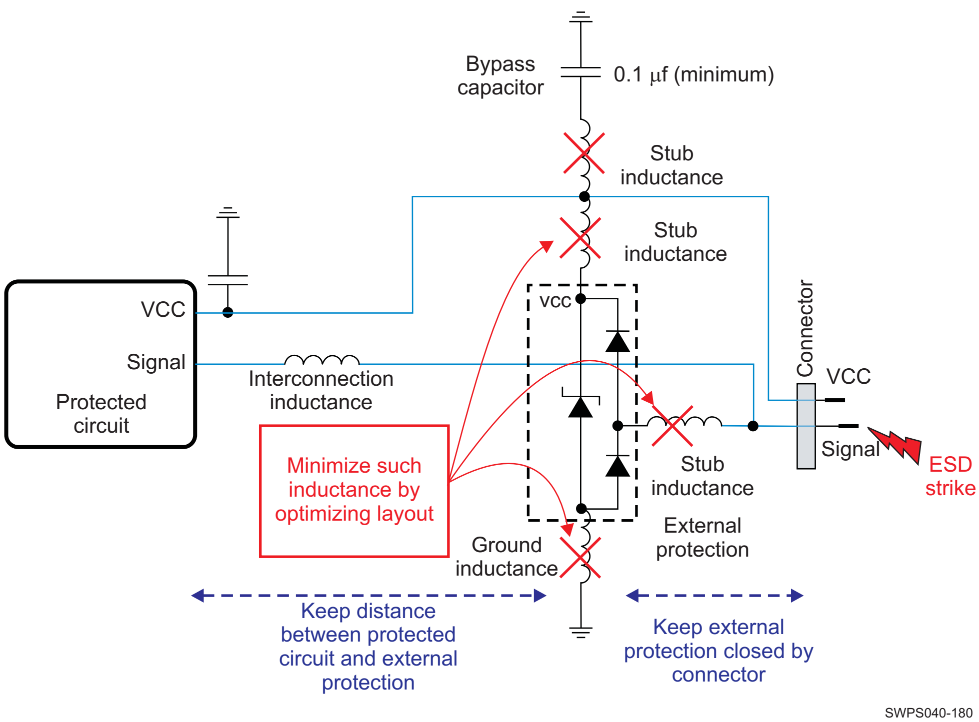

Figure A-18. Placement Recommendation for an ESD External Protection

A.2.4.5 Miscellaneous EMC Guidelines to Mitigate ESD Immunity

- Avoid running critical signal traces (clocks, resets, interrupts, control signals, etc.) near PCB edges.
- Add high frequency filtering: Decoupling capacitors close to the receivers rather than close to the drivers to minimize ESD coupling
- Put a ground (guard) ring around the entire periphery of the PCB to act as a lightning rod

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- Connect the guard ring to the PCB ground plane to provide low impedance path for ESD-coupled current on the ring
- Fill unused portions of the PCB with ground plane.
- Minimize circuit loops between power and ground by using multilayer PCB with dedicated power and ground planes
- Shield long line length (strip lines) to minimize radiated ESD
- Avoid running traces over split ground planes. It is better to use a bridge connecting the two planes in one area

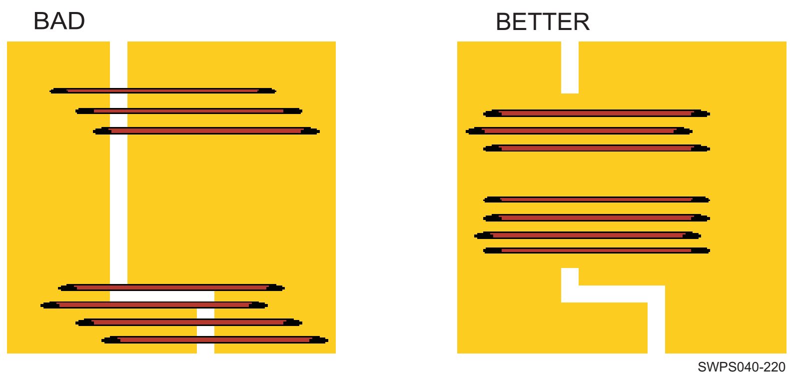

Figure A-19. Trace Examples

- Always route signal traces and their associated ground returns as close to one another as possible to minimize the loop area enclosed by current flow:
  - At high frequencies current follows the path of least inductance.
  - At low frequencies current flows through the path of least resistance.

A.3 Single-Ended Interfaces

A.3.1 General Routing Guidelines

The following paragraphs detail the routing guidelines that must be observed when routing the various functional LVCMOS interfaces.

- Line spacing:
  - For a line width equal to W, the spacing between two lines must be 2W, at least. This minimizes the crosstalk between switching signals between the different lines. On the PCB, this is not achievable everywhere (for example, when breaking signals out from the OMAP4430 package), but it is recommended to follow this rule as much as possible. When violating this guideline, minimize the length of the traces running parallel to each other (See Figure A-24).
- Length matching:
  - For bus or traces at frequencies lesser than 10 MHz: the trace length matching (maximum length difference between the longest and the shortest lines) must be less than 25 mm.
  - For bus or traces at frequencies greater than 10 MHz: the trace length matching (maximum length difference between the longest and the shortest lines) must be less than 2.5 mm.
- Characteristic impedance
  - Characteristic impedance for single-ended interfaces is recommended to be between 30 and 60 Ω and in some specific cases between 40 and 55 Ω to minimize overshoot and undershoot on far-end loads.

A.3.2 Single-Ended PCB Guideline in OMAP4

A.3.2.1 OMAP4430 Single-Ended Interfaces—PCB Guideline

The following interfaces follow the general guideline of single-ended interfaces.

A.3.2.1.1 OMAP4430 Single-Ended Interfaces—GPMC PCB Guideline

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NOTE

GPMC: For more information on PCB guideline, see Section 6.4.1, *General-Purpose Memory Controller (GPMC),* especially the timing condition tables, PCB Conditions part.

A.3.2.1.2 OMAP4430 Single-Ended Interfaces—DISPC PCB Guideline

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NOTE

DISPC: For more information on PCB guideline, see Section 6.5.2.1.1, *DSS—DISPC—Quad eXtended Graphics Array (QXGA) Application—SDR Mode,* especially the timing condition tables, PCB Conditions part.

A.3.2.1.3 OMAP4430 Single-Ended Interfaces—RFBI LCD Panel PCB Guideline

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NOTE

RFBI MIPI DBI 2.0: For more information on PCB guideline, see Section 6.5.2.2.1, *DSS—Remote Frame Buffer Interface (RFBI)—MIPI DBI2.0—LCD Panel,* especially the timing condition tables, PCB Conditions part.

A.3.2.1.4 OMAP4430 Single-Ended Interfaces—RFBI DLP Pico PCB Guideline

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NOTE

RFBI MIPI Pico DLP: For more information on PCB guideline, see Section 6.5.2.2.2, *DSS—Remote Frame Buffer Interface (RFBI)—Pico DLP,* especially the timing condition tables, PCB Conditions part.

A.3.2.1.5 OMAP4430 Single-Ended Interfaces—McBSP PCB Guideline

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NOTE

McBSP: For more information on PCB guideline, see Section 6.6.1, *Multichannel Buffered Serial Port (McBSP),* especially the timing condition tables, PCB Conditions part.

A.3.2.1.6 OMAP4430 Single-Ended Interfaces—McASP PCB Guideline

---

NOTE

McASP: For more information on PCB guideline, see Section 6.6.2, *Multichannel Buffered Serial Port (McASP)*, especially the timing condition tables, PCB Conditions part.

A.3.2.1.7 OMAP4430 Single-Ended Interfaces—McSPI PCB Guideline

---

NOTE

McSPI: For more information on PCB guideline, see Section 6.6.3, *Multichannel Serial Port Interface (McSPI)*, especially the timing condition tables, PCB Conditions part.

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A.3.2.1.8 OMAP4430 Single-Ended Interfaces—DMIC PCB Guideline

NOTE

DMIC: For more information on PCB guideline, see Section 6.6.4, *Digital Microphone (DMIC)*, especially the timing condition tables, PCB Conditions part.

A.3.2.1.9 OMAP4430 Single-Ended Interfaces—McPDM PCB Guideline

NOTE

McPDM: For more information on PCB guideline, see Section 6.6.5, *Multichannel Pulse Density Modulation (McPDM)*, especially the timing condition tables, PCB Conditions part.

A.3.2.1.10 OMAP4430 Single-Ended Interfaces—SlimBus PCB Guideline

NOTE

SlimBus: For more information on PCB guideline, see Section 6.6.6, *SlimBus*, especially the timing condition tables, PCB Conditions part.

A.3.2.1.11 OMAP4430 Single-Ended Interfaces—HSI PCB Guideline

NOTE

HSI: For more information on PCB guideline, see Section 6.6.7, *High-Speed Synchronous Interface (HSI)*, especially the timing condition tables, PCB Conditions part.

A.3.2.1.12 OMAP4430 Single-Ended Interfaces—USB PCB Guideline

NOTE

USB: For more information on PCB guideline, see Section 6.6.8, *Universal Serial Bus (USB)*, especially the timing condition tables, PCB Conditions part.

A.3.2.1.13 OMAP4430 Single-Ended Interfaces—I^2C PCB Guideline

NOTE

I^2C: For more information on PCB guideline, see Section 6.6.9, *Inter-Integrated Circuit Interface (I^2C)*, especially the timing condition tables, PCB Conditions part.

A.3.2.1.14 OMAP4430 Single-Ended Interfaces—UART PCB Guideline

NOTE

UART: For more information on PCB guideline, see Section 6.6.11, *Universal Asynchronous Receiver Transmitter (UART)*, especially the timing condition tables, PCB Conditions part.

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A.3.2.1.15 OMAP4430 Single-Ended Interfaces—SDMMC PCB Guideline

NOTE

SDMMC: For more information on PCB guideline, see Section 6.7.1, *Multimedia Memory Card and Secure Digital IO Card (SDMMC)*, especially the timing condition tables, PCB Conditions part.

For more information on SDMMC ESD guideline examples, see Section A.3.2.2.1, *ESD Implementation—MMC/SD/SDIO 1 Interface—SD Mode.*

A.3.2.1.16 OMAP4430 Single-Ended Interfaces—TPIU PCB Guideline

NOTE

TPIU: For more information on PCB guideline, see Section 6.8.1.1, *Trace Port Interface Unit (TPIU),* especially the timing condition tables, PCB Conditions part.

A.3.2.1.17 OMAP4430 Single-Ended Interfaces—STM PCB Guideline

NOTE

STM: For more information on PCB guideline, see Section 6.8.1.2, *System Trace Module Interface (STM),* especially the timing condition tables, PCB Conditions part.

A.3.2.1.18 OMAP4430 Single-Ended Interfaces—JTAG PCB Guideline

NOTE

JTAG: For more information on PCB guideline, see Section 6.8.2, *JTAG Interface (JTAG),* especially the timing condition tables, PCB Conditions part.

A.3.2.1.19 OMAP4430 Single-Ended Interfaces—cJTAG PCB Guideline

NOTE

cJTAG: For more information on PCB guideline, see Section 6.8.3, *cJTAG Interface (cJTAG),* especially the timing condition tables, PCB Conditions part.

A.3.2.1.20 OMAP4430 Single-Ended Interfaces—KeyPad PCB Guideline

NOTE

Here is the routing of the keypad row and column signals (for all keypad signals):

- The trace impedance must be between 20 Ω and 70 Ω.
- Maximum trace length is equal to 20 cm.

A.3.2.1.21 OMAP4430 Single-Ended Interfaces—DM Timer PCB Guideline

NOTE

Here is the routing for all DM timer signals:

- The trace impedance must be between 20 Ω and 70 Ω.
- Maximum trace length is equal to 7 cm.

A.3.2.2 OMAP4430 Single-Ended Interfaces—OMAP4430 System ESD Guideline

A.3.2.2.1 ESD Implementation—MMC/SD/SDIO 1 Interface—SD Mode

NOTE

For more information on system ESD, see Section A.2.4, *System ESD Generic Guideline*.

NOTE

For more information on far-end load, trace length, and characteristics impedance for SD card types, see Section 6.7.1.1, *MMC/SD/SDIO 1 Interface*.

Figure A-20 shows a proposal of SDMMC1 implementation with an external SD card configuration.

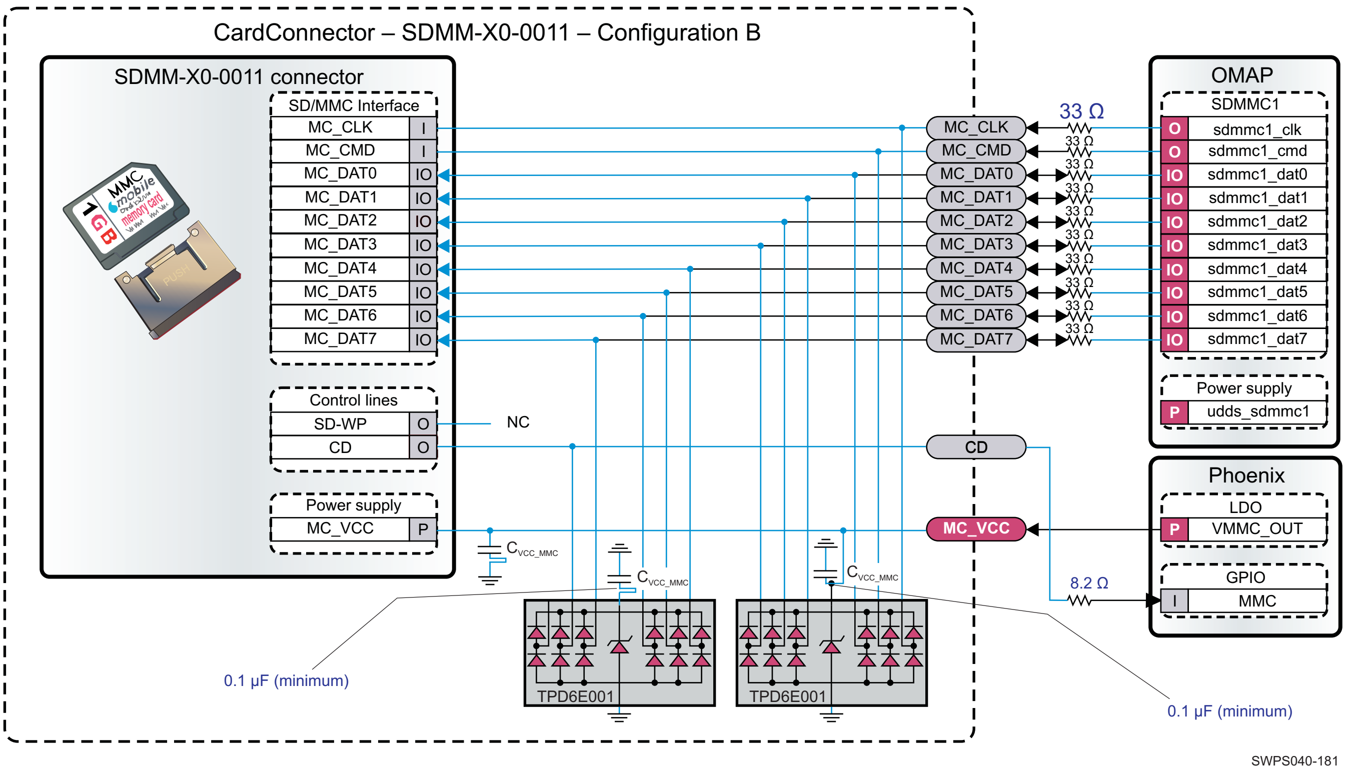

Figure A-20. SDMMC1 Implementation Proposal With External SD Card

Some guidelines regarding system ESD:

- It is recommended to use an ESD protection array in conjunction with serial resistors placed between the protection device and OMAP4430 SDMMC pins. The ESD protection has to be placed close to the SD card connector and the serial resistor has to be placed close to the OMAP device. The value recommended for the serial resistor is 33 Ω ±5%.
- SD, MMC, or dual-support SD/MMC connectors must have card detect option and may have write protect pins. In this case, it is recommended to use an ESD external protection device. In addition, for the CD connector pin (for example attached to the TLW6030 MMC pin), a resistor needs to be placed between the PMIC and the external protection.
- ESD protection devices must have a low turn-on resistance (R_{DYN} ≤ 1 Ω).

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CAUTION

System level ESD results are dependent on the components being connected to the product.

Part numbers that are different than the reference board specification (see Table A-4) are not assured to meet system level ESD requirements.

Table A-4. SDMMC Component Reference

INTERFACE	DEVICE	SUPPLIER	PART NUMBER
SDMMC	TVS	TI	TPD6E001RSE
	C	Murata	[0.1 uF/10V/0402] GRM155R71A104KA0

A.3.2.2.2 ESD Implementation—KeyPAD Interface

NOTE

For more information on system ESD, see Section A.2.4, *System ESD Generic Guideline*.

To protect against electromagnetic interference (EMI), the ESD recommendation is to implement an EMI filter array. An alternate solution is to use ESD protection array. To further enhance ESD robustness, 5-Ω serial resistors may be placed in between protection device and OMAP4430 keypad. ESD protection device must exhibit a low turn-on resistance (≤ 1 Ω typical).

Table A-5. Keypad Components Reference

INTERFACE	DEVICE	SUPPLIER	PART NUMBER
Keypad	EMIF	TI	TPD6F003

A.3.2.2.3 ESD Implementation—JTAG and cJTAG Interfaces

NOTE

For more information on system ESD, see Section A.2.4, *System ESD Generic Guideline*.

NOTE

For more information on JTAG and cJTAG far end load, trace length and characteristics impedance, see Section 6.8.2, *JTAG Interface (JTAG)*, or Section 6.8.3, *cJTAG Interface (cJTAG)*.

For a system having JTAG test points accessible to end users (example when located under battery pack for handheld device), system ESD protection can be achieved using TPD6E001 to target 8 kV direct contact. Additional resistors of 3.9 Ω could be used to strengthen ESD robustness.

ESD protection device must exhibit a low turn-on resistance (≤ 1 Ω typical).

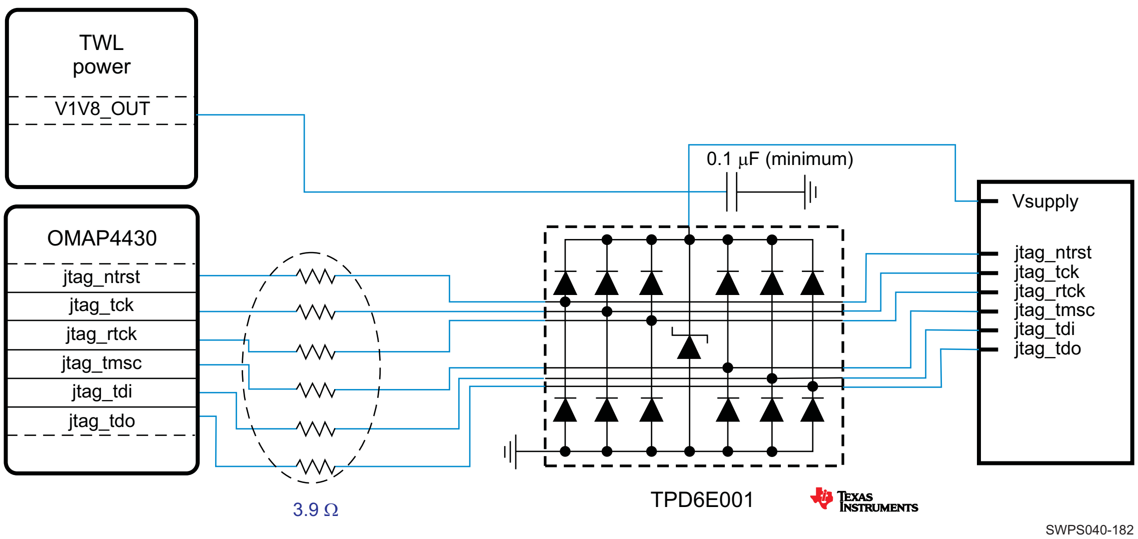

Figure A-21. JTAG ESD Protection Example

CAUTION

System level ESD results are dependent on the components being connected to the product.

Part numbers that are different than the reference board specification (see Table A-6) are not assured to meet system level ESD requirements.

Table A-6. JTAG Component Reference

INTERFACE	DEVICE	SUPPLIER	PART NUMBER
JTAG	TVS	TI	TPD6E001RSE
	C	Murata	[0.1 uF/10V/0402] GRM155R71A104KA0

A.4 Differential Interface PCB Guidelines

A.4.1 General Routing Guidelines

The following general routing guidelines describe the routing guidelines for MIPI differential lanes.

Each guideline is depicted in detail in Section A.4.2, *Three-step Design and Validation Methodology for OMAP Boards*.

For more information, you can also refer to the MIPI D-PHY specification v1.00.

- As much as possible, no other high frequency signals must be routed in close proximity to the differential pair.
- Must be routed as differential traces on the same layer. The trace width and spacing must be chosen to yield a 100-Ω differential impedance, along with a 50-Ω single-ended impedance for each signal of the pair.
- Due to the fact that the MIPI signals are used for low-power, single-ended signaling in addition to their high-speed differential implementation, the pairs must be loosely coupled.
- The flight time for the signals must not exceed 2 ns, which assuming a PCB constructed from standard FR-4 material, would imply a maximum trace length of approximately 10” (25.4 cm).
- Minimize external components on differential lanes (like external ESD, probe points).
- Through-hole pins are not recommended.
- Differential lanes mustn’t cross image planes (ground planes).

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- No sharp bend on differential lanes.
- Number of vias on the differential pairs must be minimized.
- Shielded routing is to be promoted as much as possible (for instance, signals must be routed on internal layers that are inside power and/or ground planes).

A.4.2 Three-step Design and Validation Methodology for OMAP Boards

A.4.2.1 Three-step Design and Validation Methodology—General Guidelines

The following requirements are not dependent on the IO names, such as CSI, DSI, HDMI, and USB, because the differential interfaces basically have the same requirements for the PCB lines.

On the other hand, the PCB requirement is dependent on the operating speed of the circuits because the length mismatch is given by the bit time (UI) of the signal.

The PCB guidelines for the OMAP differential interfaces are based on the three-step design and validation methodology in Figure A-22.

The three-step methodology provides a guideline for the design of the PCB differential lines as well as a validation methodology of the designed differential lines to ensure that the PCB differential lines are designed well.

The first step is the general guidelines showing the ideal condition of the PCB differential lines. The first step is important for the PCB designers since it shows the general requirements for the PCB differential lines.

The second step is the length mismatch requirement to satisfy the system-level specification of the differential interfaces along with the OMAP package. Step 1 and Step 2 comprise the design guideline.

As a validation methodology, the third step is the frequency-domain specification of the differential lines that the lines need to satisfy in the frequency domain. If the PCB lines satisfy the frequency-domain specification, the design is done. Otherwise, the lines need to be improved.

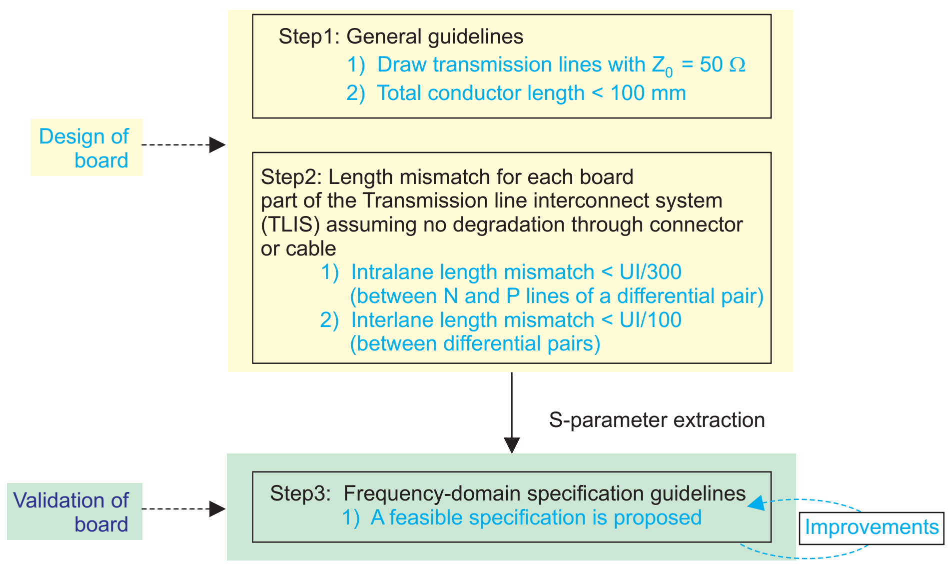

Figure A-22. Summary of Three-step PCB Design and Validation Methodology for OMAP4 Differential Interfaces

The differential interfaces are connected from the OMAP circuit to the device circuit through the OMAP package, OMAP board, cable, device board, and device package.

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In this section, the guidelines for the OMAP PCB differential lines are presented.

The PCB guidelines are developed to align the OMAP board with the OMAP package since the specification of the differential interfaces has one consolidated requirement for the package and board, which can be tested by measurement equipment such as oscilloscopes.

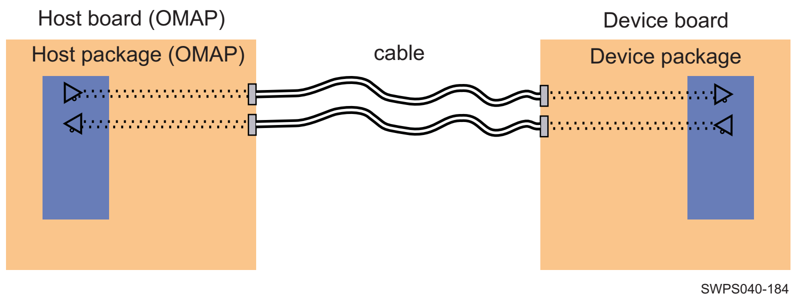

Figure A-23. Transmission Line Interconnect System (TLIS)

The ideal electrical condition of the PCB differential lines is basically the same for all the OMAP differential interfaces, which are shown as:

- Single-ended Z_0 = 50 Ω, differential Z_0 = 100 Ω
- Negligible length mismatch among differential lines.

The loss of the differential lines is not a big concern since the loss causes intersymbol interference (ISI) that can be compensated by equalization techniques. But, for the differential interfaces without equalization techniques, the length is recommended to be kept at a minimum for a smaller ISI. For the OMAP board, we recommend that the length of the PCB differential lines be less than 100 mm.

In the above requirements, the length mismatch requirement is not clear. It is always better to have smaller length mismatch. But, how small is good enough? Toclarify the length mismatch requirement for the OMAP board lines, we recommend using the below conditions:

- Intralane length mismatch < (UI / 300)
- Interlane length mismatch < (UI / 100)

UI is the bit time of the signal. The intralane length mismatch is the length mismatch between the N and P lines of a differential pair, and the interlane length mismatch is between the differential pairs.

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A.4.2.2 Step 1: General Guidelines for OMAP Boards

NOTE

The OMAP differential interfaces, such as CSI and DSI, require the PCB differential lines with the following two conditions:

- Single-ended Z_0 = 50 Ω, differential Z_0 = 100 Ω
- Total conductor length < 100 mm

The total conductor length is limited for the PCB lines not to have too much intersymbol interference (ISI). In general, the conductor length is recommended to be kept at a minimum for a smaller ISI.

In Step 1, the general rule of thumb for the space S = 2 * W is not designated. It is because although the S = 2 * W rule is a good rule of thumb, it is not always the best solution.

Sometimes, the lines with ground guard between the lines are better. It remains up to the PCB designers whether the S = 2 * W rule is used or not.

However, the electrical performance needs to be better than the frequency-domain specification in Step 3. The S = 2 * W rule is generally recommended.

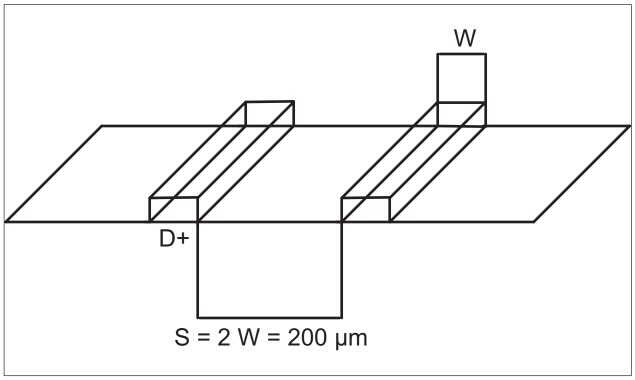

Figure A-24. Ground Guard Illustration

A.4.2.3 Step 2: Length Mismatch Guidelines for OMAP Boards

NOTE

The guidelines for the length mismatch of the PCB differential lines are presented as:

- Intralane skew between N and P < (UI/300)
- Interlane skew between differential pairs < (UI/100)

UI is the bit time of the signal. The intralane length mismatch is the length mismatch between the N and P lines of a differential pair, and the interlane length mismatch between the differential pairs.

The time skew can be converted to the physical length with the below equation as 500 µm for the intralane skew and 1500 µm for the interlane skew for a speed of 1000 Mbps, based on the dielectric material of Er = 4.0.

$$Length = \frac{3x10^8\,(m/s)}{\sqrt{4.0}} \cdot (\text{time interval}) \quad [\text{m}]$$

SWPS040-e003

The length mismatch requirement can be formatted in Table A-7 as (assuming operating speed is 1000 Mbps):

Table A-7. Length Mismatch Guidelines of Differential Lines(1)

PARAMETER	TYPICAL VALUE	UNIT
Operating Speed	1000	Mbps
UI (bit time)	1000	ps
Intralane skew (UI / 300)	3.3	ps
Length between N and P traces	0.5	mm
Interlane Skew (UI / 100)	10	ps
Length between pairs	1.5	mm

(1) The interlane skew is actually applied to data and clock lines.

Step 1 and Step 2 comprise the design guidelines for the PCB differential lines. The PCB designers can draw the PCB differential lines satisfying the Step 1 and Step 2 requirements.

Then, Step 3 in Section A.4.2.4 is a validation methodology for the designed PCB differential lines checking whether the electrical performance of the differential lines is good enough.

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A.4.2.4 Step 3: Frequency-domain Specification Guidelines for OMAP Boards

Although the PCB designers will draw the lines carefully with the Step 1 and Step 2 guidelines, the lines can have poor electrical performance due to many reasons.

The vertical connections such as vias and nonuniform line connection such as the escape traces can degrade the electrical performance of the differential lines.

In addition, the ground design around the lines can also affect the electrical performance. So, to ensure that the differential lines are good, the frequency-domain behavior of the lines needs to be checked and compared to the frequency-domain specification given here.

Then, the S-parameters needs to be extracted with a 3D Maxwell Equations' solver such as high-frequency structure simulator (HFSS) or equivalent. The 2D and 2.5D Maxwell Equations' solvers are not recommended to extract the S-parameter of the differential lines because they could not catch the effect of the vias.

The frequency-domain specification is the frequency-domain behavior of a differential pair that has good electrical performance.

The frequency-domain specification for the PCB differential lines is made up of the intralane frequency-domain specification and the interlane frequency-domain specification, as shown below:

1. Intralane frequency-domain specification
   - Differential-mode characteristics: Sdd12, Sdd11 / Sdd22
   - Common-mode characteristics: Scc11 / Scc22
   - Mode-conversion characteristics: Scd11, Scd12, Scd21, Scd22, Sdc11, Sdc12, Sdc21, Sdc22
2. Interlane frequency-domain specification
   - Differential-mode characteristics: Sdd11 / Sdd22
   - Common-mode characteristics: Scc11 / Scc22

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A.4.2.4.1 Intralane Frequency-domain Specification

The port assignment for the intralane frequency domain specification test is shown in Figure A-25. For the intralane specification test, the four ports are assigned to the N and P lines of a differential pair. The S-parameters can be extracted from dc to 5 GHz.

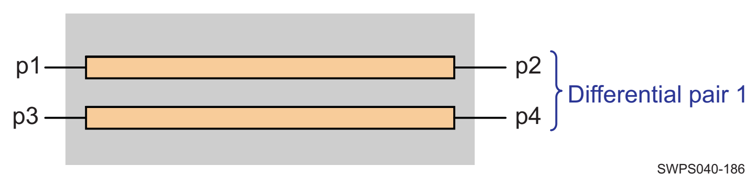
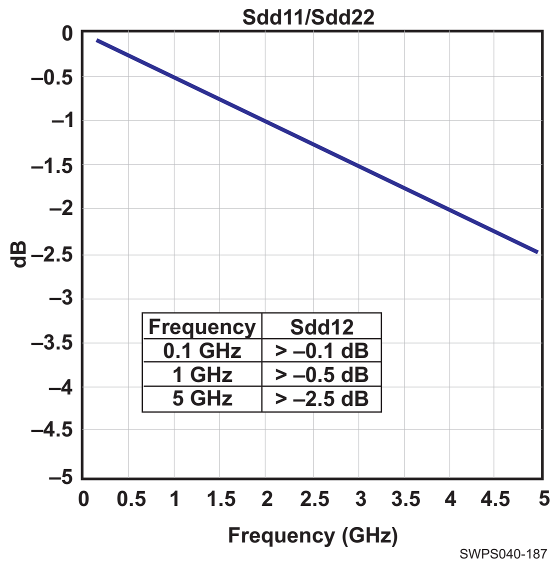


Figure A-25. Port Assignment for the Intralane Frequency-domain Specification

A.4.2.4.1.1 Sdd12

Sdd12 represents the differential-mode insertion loss of the differential line. Bigger Sdd12 indicates that the transmission line has smaller loss. Since the insertion loss is proportional to the length of the lossy transmission line, Sdd12 will be smaller as the length increases.

So for the OMAP board, we recommend that the total conductor length be smaller than 100 mm for the PCB differential lines, whose electrical behavior is similar to that in Figure A-26. The ideal lossless differential line has Sdd12 = 1, which is 0 dB. The Sdd12 is recommended to be larger than the below line from dc to 5 GHz. If the designed differential lines have lower Sdd12 than the specification, the lines can be improved by reducing the length of the differential lines.

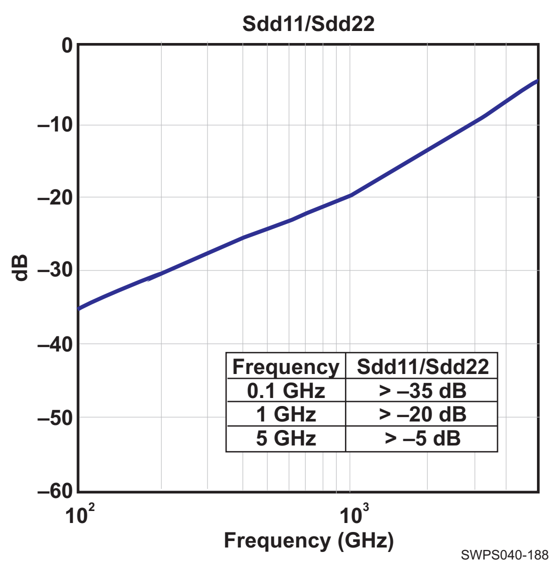


Frequency	Sdd12
0.1 GHz	> –0.1 dB
1 GHz	> –0.5 dB
5 GHz	> –2.5 dB

Figure A-26. Intralane Sdd12 Frequency-domain Specification

A.4.2.4.1.2 Sdd11 / Sdd22

Sdd11 / Sdd22 represents the differential-mode return loss of the differential line. Smaller Sdd11 / Sdd22 indicates that the transmission line has smaller return loss. The ideal differential line with Z_0 = 50 Ω (Z_0diff = 100 Ω) has Sdd11 / Sdd22 = 0, which is –∞ dB. Sdd11 / Sdd22 is tightly related to the differential-mode characteristic impedance of the differential line. Sdd11 / Sdd22 is recommended to be smaller than the below line.



Frequency	Sdd11/Sdd22
0.1 GHz	> –35 dB
1 GHz	> –20 dB
5 GHz	> –5 dB

Figure A-27. Sdd11/Sd22 Frequency-domain Specification

If the designed differential lines have higher Sdd11 / Sdd22 than the specification, the differential lines can be improved by adjusting the space distance between the N and P lines of a differential pair. It is because the differential-mode characteristic impedance is mostly affected by the space.

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A.4.2.4.1.3 Scc11 / Scc22

Scc11 / Scc22 represents the common-mode return loss of the differential transmission line. The smaller of Scc11 / Scc22 indicates the transmission line has smaller return loss. Scc11 / Scc22 is tightly related to the common-mode characteristic impedance of the differential line. The ideal differential line with Z_0 = 50 Ω (Z_0diff = 100 Ω) has Scc11 / Scc22 = 0, which is –∞ dB. Scc11 / Scc22 is recommended to be smaller than the line below.

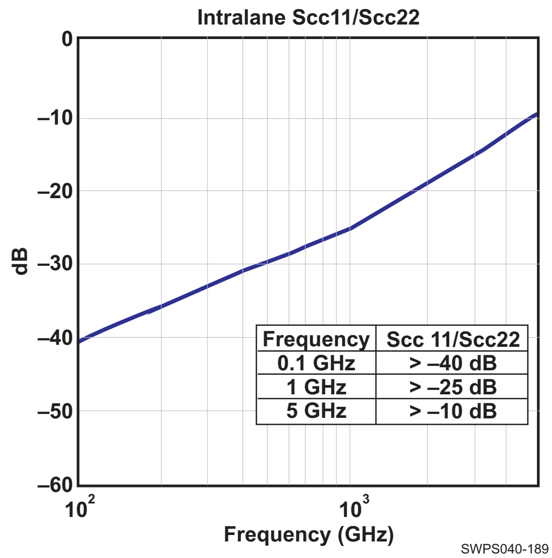

Figure A-28. Intralane Scc11/Scc22 Frequency-domain Specification

If the designed differential lines have higher Scc11 / Scc22 than the specification, the differential lines can be improved by changing the power and ground nets around the lines. It is because the common-mode characteristic impedance is mostly affected by the power and ground nets around.

A.4.2.4.1.4 Scd11, Scd12, Scd21, Scd22, Sdc11, Sdc12, Sdc21, Sdc22

Scd11, Scd12, Scd21, Scd22, Sdc11, Sdc12, Sdc21 and Sdc22 represent the mode-conversion factors between the common-mode signal and the differential-mode signal. The lower number means that the conversion is smaller. They are recommended to be smaller than the below line. If the designed differential lines have higher mode-conversion factors than the specification, the differential lines can be improved by improving the symmetry between the N and P lines of a differential pair. If the two lines are perfectly symmetric, the mode-conversion factors will be 0, which is –∞ dB.

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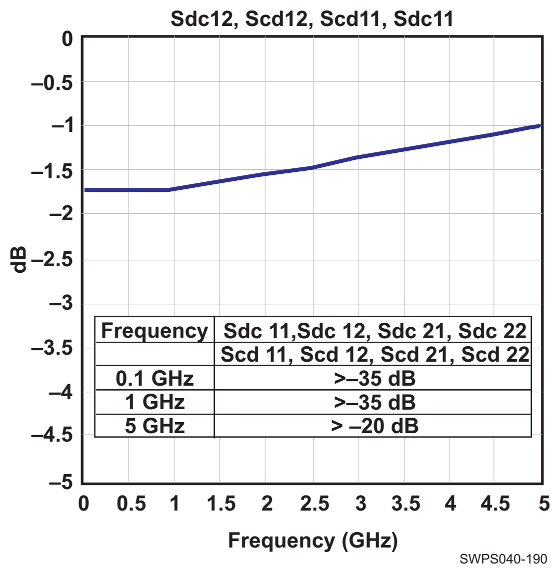

Figure A-29. Intralane Scd11, Scd12, Sdc11, Sdc12 Frequency-domain Specification

A.4.2.4.2 Interlane Frequency-domain Specification

In this section, the interlane frequency-domain specification is described between differential lines. In the interlane specification test, one line is chosen from a differential pair and the other line is chosen from another differential pair, as shown in Figure A-30. Then, the S-parameters will be extracted from dc to 5 GHz with a 3D Maxwell Equation solver such as high-frequency structure simulator (HFSS) or equivalent, and the frequency-domain behavior will be compared to the frequency-domain specification given here. Since it is desired that the crosstalk between differential pairs be smaller, the differential-mode and common-mode characteristics requirement is stricter than the intralane specification.

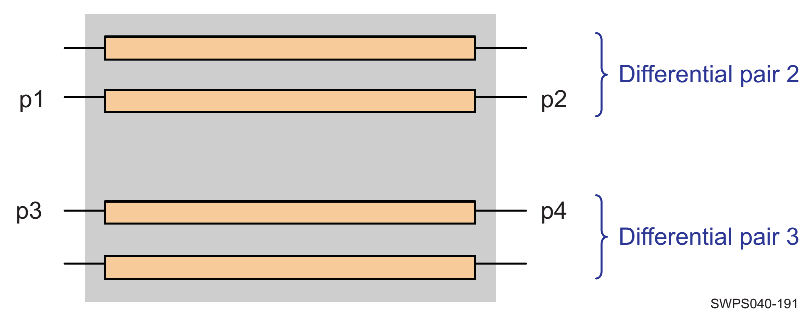

Figure A-30. Port Assignment for the Interlane Frequency-domain Specification

A.4.2.4.2.1 Sdd11 / Sdd22

Sdd11 / Sdd22 represents the differential-mode return loss of the two lines. The ideal condition for the interlane specification is to place the two lines far away from each other not to have any crosstalk. Then, the ideal interlane Sdd11 / Sdd22 = 0, which is –∞ dB. Sdd11 / Sdd22 is recommended to be smaller than the below line.

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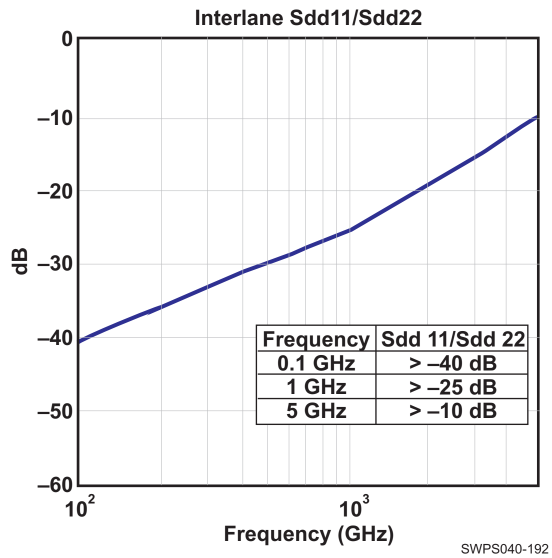

Figure A-31. Interlane Sdd11 / Sdd22 Frequency-domain Specification

If the designed differential lines have higher Sdd11 / Sdd22 than the specification, the differential lines can be improved by two ways. One way is to adjust the space distance between the N and P lines of a differential pair, and the other way is to put ground/power nets between the two lines to reduce the crosstalk.

A.4.2.4.2.2 Scc11 / Scc22

Scc11 / Scc22 represents the common-mode return loss of the two lines. The ideal interlane Scc11 / Scc22 =0, which is –∞ dB. Scc11 / Scc22 is recommended to be smaller than the below line. If the designed differential lines have higher Scc11 / Scc22 than the specification, the differential lines can be improved by putting ground/power nets between the two lines.

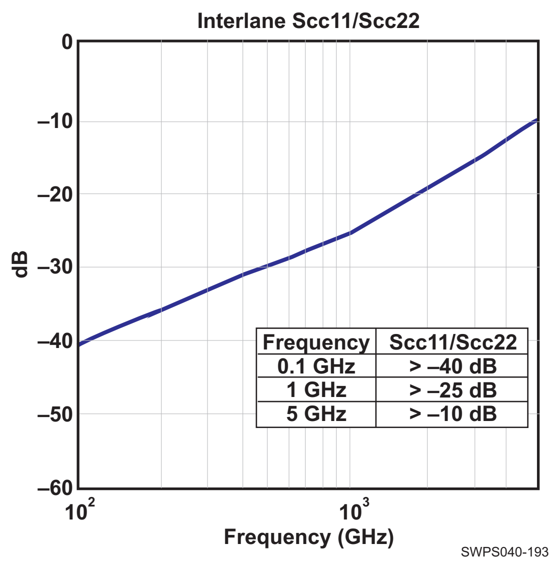

Figure A-32. Interlane Scc11 / Scc22 Frequency-domain Specification

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A.4.3 MIPI D-PHY PCB Guidelines in OMAP4

The MIPI D-PHY signals include the CSI21, CSI22, DSI1, and DSI2 interfaces to or from the OMAP4430. For more information regarding the MIPI-PHY signals and corresponding balls, see Section 2.4, *Signal Descriptions*.

Note that OMAP4460 features an additional CSI2 lane. For more information, see the OMAP4460 ES1.0 data manual or OMAP4460 vs OMAP4430 DM Delta addendum.

In next section, the PCB guidelines of the following six differential interfaces are presented.

- CSI21 and CSI22 MIPI CSI-2 @ 1.0 Gbps
- CSI21 and CSI22 MIPI CSI-2 @ 824 Mbps
- CSI21 and CSI22 MIPI CSI-2 @ 800 Mbps
- DSI1 and DSI2 MIPI DSI1 @ 900 Mbps
- DSI1 and DSI2 MIPI DSI1 @ 824 Mbps

A.4.3.1 CSI21 and CSI22 MIPI CSI-2 @ 1 Gbps (Up to 3 Data Lanes, OPP100), @ 824 Mbps (Up to 4 Data Lanes, OPP100), @ 800 Mbps (Up to 4 Data Lanes, OPP50) Device PCB Guidelines

CAUTION

If the skew degradation due to the interconnect (from the output transmitter ball to the input receiver ball) between the clock and the data lanes is less than ±170 ps (instead of ±200 ps in the MIPI D-PHY specification), then 1 Gbps per data lane is achievable with 4 data lanes at OPP100 operating point. This must be met for an interconnect length less than 10 cm.

NOTE

The CSI21 and CSI22 MIPI CSI-2 application timings are described in Section 6.5.1.1, *Camera Serial Interface (CSI2)* (especially, the timing conditions are specified in the “Timing Conditions” tables of this section).

First, the following PCB guidelines for CSI2 working up to 1.0 Gbps are presented based on the three-step design and validation methodology described in Section A.4.2, *Three-step Design and Validation Methodology for OMAP Boards*.

For the design of the PCB differential lines on the OMAP board, the PCB designers need to keep in mind the requirements of Step 1 and Step 2: the characteristic impedance must be 50 Ω, the total length must be smaller than 100 mm, and the length mismatch requirements must be satisfied.

Then, after the PCB design is finished, the S-parameters of the PCB differential lines will be extracted with a 3D Maxwell Equation Solver such as high-frequency structure simulator (HFSS) or equivalent, and compared to the frequency-domain specification as outlined in Step 3 of design methodology. If the PCB lines satisfy the frequency-domain spec, the design is done. Otherwise, the design needs to be improved.

A.4.3.1.1 Step 1: General Guidelines

The general guidelines for the PCB differential lines of CSI2 are given as:

- Single-ended Z_0 = 50 Ω
- Total conductor length on OMAP board < 100 mm.

In the step, the general rule of thumb for the space S = 2 * W is not designated (see Figure A-24). It is because although the S = 2 * W rule is a good rule of thumb, it is not always the best solution. The electrical performance will be checked with the frequency-domain specification in Step 3. Even though the designers does not follow the S = 2 * W rule, the differential lines are ok if the lines satisfy the frequency-domain specification in Step 3.

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A.4.3.1.2 Step 2: Length Mismatch Guidelines

A.4.3.1.2.1 Step 2: Length Mismatch Guidelines—CSI21 and CSI22 MIPI CSI-2 @ 1.0 Gbps

The guidelines of the length mismatch for CSI-2 are presented in Table A-8. The intralane length mismatch must be less than 0.5 mm, and the interlane length mismatch must be less than 1.5 mm.

Table A-8. Length Mismatch Guidelines for CSI-2 @ 1.0 Gbps

PARAMETER	TYPICAL VALUE	UNIT
Operating speed	1000	Mbps
UI (bit time)	1000	ps
Intralane skew (UI / 300)	3	ps
Length between N and P traces	0.5	mm
Interlane skew (UI / 100)	10	ps
Length between pairs	1.5	mm

A.4.3.1.2.2 Step 2: Length Mismatch Guidelines—CSI21 and CSI22 MIPI CSI-2 @ 824 Mbps

The guidelines of the length mismatch for CSI-2 are presented in Table A-9.

Table A-9. Length Mismatch Guidelines for CSI-2 @ 824 Mbps

PARAMETER	TYPICAL VALUE	UNIT
Operating speed	824	Mbps
UI (bit time)	1213	ps
Intralane skew (UI / 300)	4	ps
Length between N and P traces	0.6	mm
Interlane skew (UI / 100)	12	ps
Length between pairs	1.8	mm

A.4.3.1.2.3 Step 2: Length Mismatch Guidelines—CSI21 and CSI22 MIPI CSI-2 @ 800 Mbps

The guidelines of the length mismatch for CSI-2 are presented in Table A-10. The intralane length mismatch must be less than 0.6 mm, and the interlane length mismatch must be less than 1.8 mm.

Table A-10. Length Mismatch Guidelines for CSI-2 @ 800 Mbps

PARAMETER	TYPICAL VALUE	UNIT
Operating speed	800	Mbps
UI (bit time)	1250	ps
Intralane skew (UI / 300)	4	ps
Length between N and P traces	0.6	mm
Interlane skew (UI / 100)	12	ps
Length between pairs	1.8	mm

A.4.3.1.3 Step 3: Frequency-domain Specification Guidelines

With the information in Step 1 and Step 2, the PCB designers can draw the PCB differential lines satisfying the Step 1 and Step 2 requirements.

However, although the PCB designers draw the lines carefully, the lines can have poor electrical performance due to many reasons.

The vertical connections such as vias and nonuniform line connection can degrade the electrical performance of the differential lines. And the ground design around the lines can also affect the electrical performance.

So, to ensure that the differential lines are well designed, the frequency-domain behavior must be compared to the frequency-domain specification in Section A.4.2.4, *Step 3: Frequency-domain Specification Guidelines for OMAP Boards*.

1. Intralane frequency-domain specification
   – Differential-mode characteristics: Sdd12, Sdd11 / Sdd22
   – Common-mode characteristics: Scc11/Scc22
   – Mode-conversion characteristics: Scd11, Scd12, Scd21, Scd22, Sdc11, Sdc12, Sdc21, Sdc22
2. Interlane frequency-domain specification
   – Differential-mode characteristics: Sdd11 / Sdd22
   – Common-mode characteristics: Scc11 / Scc22

A.4.3.2 DSI1 and DSI2 MIPI DSI1 @ 900 Mbps (Up to 3 Data Lanes), @ 824 Mbps (Up to 4 Data Lanes) Device PCB Guideline

NOTE

The DSI1 and DSI2 MIPI DSI1 application timings are described in Section 6.5.2.3, *Display Serial Interface (DSI)* (especially, the timing conditions specified in the "Timing Conditions" tables of this section).

In this section, the PCB guidelines for DSI1 working up to 900 Mbps are presented based on the three-step design and validation methodology described on Section A.4.2, *Three-step Design and Validation Methodology for OMAP Boards*.

A.4.3.2.1 Step 1: General Guidelines

The general guidelines for the PCB differential lines of DSI1 are given as:

- Single-ended $Z_0 = 50\ \Omega$
- Total conductor length on OMAP board < 100 mm.

In the step, the general rule of thumb for the space S = 2*W is not designated (see Figure A-24). It is because although the S = 2*W rule is a good rule of thumb, it is not always the best solution. The electrical performance will be checked with the frequency-domain specification in Step 3. Even though the designers does not follow the S = 2*W rule, the differential lines are ok if the lines satisfy the frequency-domain specification in Step 3.

A.4.3.2.2 Step 2: Length Mismatch Guidelines

A.4.3.2.2.1 Step 2: Length Mismatch Guidelines—DSI1 and DSI2 MIPI DSI1 @ 900 Mbps

The guidelines of the length mismatch for DSI1 are presented in Table A-11.

Table A-11. Length Mismatch Guidelines for DSI1 @ 900 Mbps

PARAMETER	TYPICAL VALUE	UNIT
Operating speed	900	Mbps
UI (bit time)	1111	ps
Intralane skew (UI / 300)	3.7	ps
Length between N and P traces	0.55	mm
Interlane skew (UI / 100)	11.1	ps
Length between pairs	1.66	mm

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A.4.3.2.2.2 Step 2: Length Mismatch Guidelines—DSI1 and DSI2 MIPI DSI1 @ 824 Mbps

The guidelines of the length mismatch for DSI1 are presented in Table A-12. The intralane length mismatch must be less than 0.6 mm, and the interlane length mismatch must be less than 1.8 mm.

Table A-12. Length Mismatch Guidelines for DSI1 @ 824 Mbps

PARAMETER	TYPICAL VALUE	UNIT
Operating speed	824	Mbps
UI (bit time)	1213.59	ps
Intralane skew (UI / 300)	4	ps
Length between N and P traces	0.6	mm
Interlane skew (UI / 100)	12	ps
Length between pairs	1.8	mm

A.4.3.2.3 Step 3: Frequency-domain Specification Guidelines

The frequency-domain specification is given in Section A.4.2.4, *Step 3: Frequency-domain Specification Guidelines for OMAP Boards*.

A.4.4 USBA0 PHY Interface in OMAP4

The USBA0 interface DP and DM signals are the positive and negative signals from the USB transceiver contained within the OMAP4430. These signals (DP or D+ (usba0_otg_dp) and DM or D– (usba0_otg_dm)) are connected to the OMAP4430 on balls B5 and B4, respectively.

Section A.4.4.1 describes the USBA0 DP and DM PCB guidelines recommended for the OMAP4430 device.

A.4.4.1 USBA0 PHY PCB Guideline

The length of DP / DM traces measured between OMAP4 and the common mode choke must follow the requirements detailed in Table A-13 to make sure that the reflections always hit the eye diagram at an optimum point in the unit interval.

NOTE

Distance between the common mode choke filter (ACM2012H in Figure A-33) and IEC ESD protection (TPD4S012 in Figure A-33) device must be as short as possible: < 30 ps

Similarly, the distance between IEC ESD protection device (TPD4S012DRY in Figure A-33) and the USB connector (Mini A-B receptacle in Figure A-33) must be as short as possible: < 30 ps

USB standard connector must be used (micro-AB or mini-AB)

USB grounds must be shorted to the board ground plane with minimum routing (only VIA must be used to connect to ground plane to avoid loop creation and so to reduce electromagnetic interference (EMI) effect.

Table A-13. USB Optimized Trace Length

PARAMETER		MIN	TYP	MAX	UNIT
DP and DM differential impedance			90	100	Ω
DP and DM individual impedance		45		49	Ω
Trace length delay for 1 mm				6.66	ps
Recommended intralane mismatch between DP and DM	Distance			1	mm
	Skew			6.66	ps

Table A-13. USB Optimized Trace Length (continued)

PARAMETER	MIN	TYP	MAX	UNIT
HS operating speed		480		Mbps
Unit interval (bit time)		2080		ps
Recommended board delay for optimum eye aperture between OMAP and CMF-ESD(1)	510	530	680	ps
Recommended distance between OMAP and CMF-ESD(2)	76.58	79.58	102.10	mm

(1) The board delay is the delay between DP and DM OMAP4 ball levels (usba0_otg_dp and usba0_otg_dm) and the common mode choke filter (CMF, ACM2012H).
For more information see Figure A-33, *USB Implementation Proposal with TWL6030 PMIC*.

(2) The board distance between the DP and DM OMAP ball level (usba0_otg_dp and usba0_otg_dm) and the common mode choke filter (CMF, ACM2012H) is calculated based on the trace length delay for 1 mm (6.66 ps).

If the above recommended requirement are not possible on customer board, the following requirements are also possible between the OMAP and the common mode choke. These values have been computed to minimize the bad effect of the reflection on the eye diagram.

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Table A-14. USB Trace Length With N Multiple

PARAMETER		MIN	TYP	MAX	UNIT
Unit interval (480 Mbps)			2080		ps
Recommended board characteristics for optimum eye aperture(1)(2)(3)	N = 0 (Recommended Value)	510	530	680	ps
	N = 1	1550	1570	1720	ps
	N = 2	2590	2610	2760	ps
	N = 3	3630	3650	3800	ps

(1) The board delay is the delay between DP and DM OMAP ball levels (usba0_otg_dp and usba0_otg_dm) and the common mode choke filter (CMF, ACM2012H). For more information see Figure A-33, *USB Implementation Proposal with TWL6030 PMIC.*

(2) The possible board delay value is calculated as follows:
N * ½ * UI + Optimum Board delay (530 ps), with N = 0, 1, 2, or 3.

(3) The board distance between the DP and DM OMAP ball level (usba0_otg_dp and usba0_otg_dm) and the common mode choke filter (CMF, ACM2012H) is calculated based on the trace length delay for 1 mm (6.66 ps).

NOTE

Remember that the distance between the common mode choke filter (ACM2012H in Figure A-33) and IEC ESD protection (TPD4S012 in Figure A-33) device must be as short as possible (< 30 ps).

Similarly, for the distance between IEC ESD protection device (TPD4S012DRY in Figure A-33) and the USB connector (Mini A-B receptacle in Figure A-33) must be as short as possible (< 30 ps).

A.4.4.2 USBA0 PHY Implementation Example

Figure A-33 proposes an example of USBA0 PHY implementation with a TWL6030 PMIC and a TPD4S012 component.

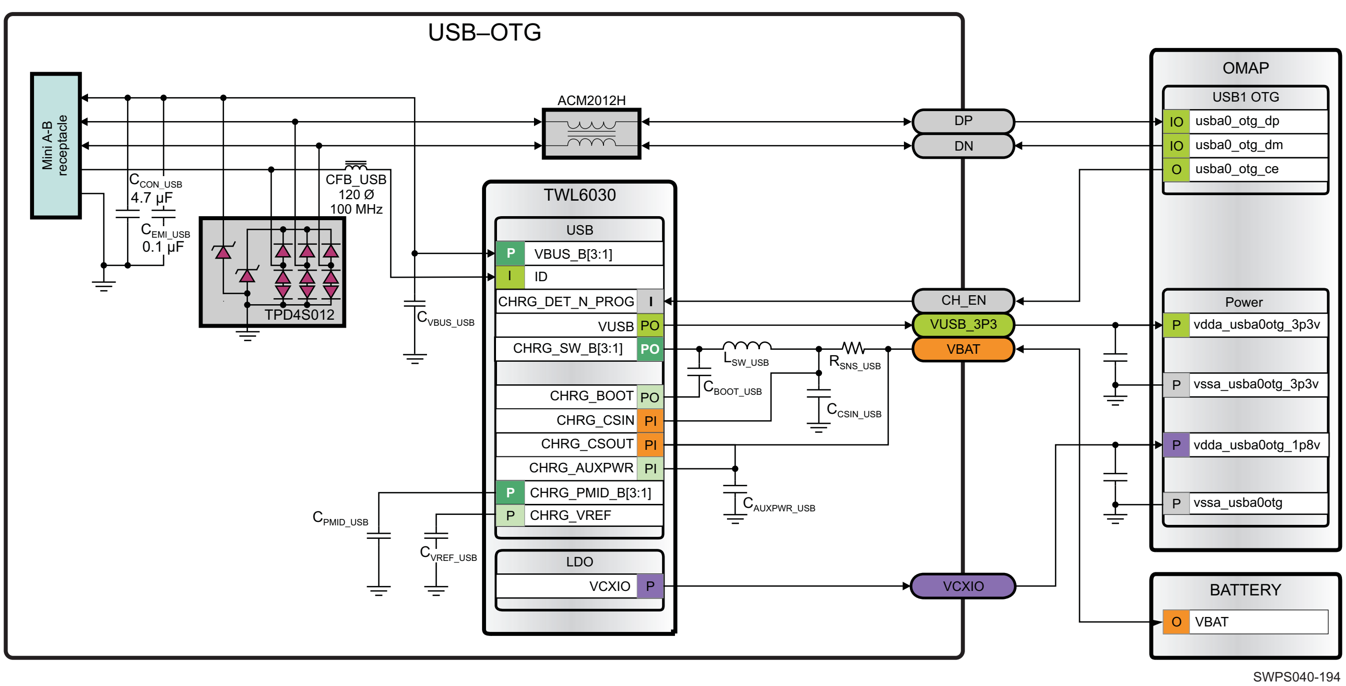

Figure A-33. USB Implementation Proposal with TWL6030 PMIC

A.4.4.3 ESD Implementation—USBA0 PHY

> **NOTE**
> For more information on system ESD, see Section A.2.4, *System ESD Generic Guideline*.

- ESD: USB standard connector has 4 pins: DP and DM attached to OMAP4430 and ID and VBUS pins attached to the TLW6030 PMIC IC device.
  - For DP and DM pins:
    - ESD protection device must be preferably an array with a low capacitance (≤ 1.0 pF typical) and a low turn-on resistance (Rdyn ≤ 1.2 Ω) while VBUS pin is designed to tolerate 20 V.
    - Common mode choke filter (CMF) must be placed between the ESD protection and the OMAP4430 to minimize electromagnetic interference (EMI).
    - If CMF is implemented, no isolation resistor is required and system ESD is greatly strengthened.
    - DC series resistance of the CMF needs to be 1 Ω maximum. Common mode bandwidth (Scc21) must not exceed 50 MHz.
  - For VBUS and ID pins:
    - For the VBUS pin, a broadband decoupling capacitor reduces noise in the VBUS power line. In addition, a large decoupling capacitor will absorb the ESD pulse energy.
    - For the ID pin, a chip ferrite bead placed between the ESD protection and the PMIC is recommended.

> **NOTE**
> System level ESD results (following IEC 61000-4-2 standard) are dependent on the components being connected to the product.
>
> Part numbers that are different than the reference board specification described in Table A-15 are not assured to meet system level ESD requirements.

Table A-15. USB Component References

INTERFACE	DEVICE	SUPPLIER	PART NUMBER
USBPHY	TVS	TI	TPD4S012DRY
	CMF	TDK	ACM2012H-900-2P
	CFB	Murata	BLM15PD121SN1
	C	Murata	[1 µF /25V/0603] GRM188R71E105KA12D
	EMICAP	Murata	[0.1 µF /16V] NFM18PC104R1C3

A.4.5 HDMI Interface in OMAP4

> **NOTE**
> For more information on HDMI, please contact your TI representative.

> **NOTE**
> For more information on system ESD, see Section A.2.4, *System ESD Generic Guideline*.

A.5 TVOUT Interface in OMAP4

> **NOTE**
> For more information, see Section 5, *Video DAC Specifications*.

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A.5.1 TV-OUT PCB Requirements

The total parasitic seen on analog I/O node have severe impact on the performance of the Video DAC. Table A-16 shows the total parasitic that can be tolerated by the module.

Table A-16. Video DAC Total Parasitic

NODE	R (Ω)	L (nH)	C (pF)	COMMENTS
cvideo_vfb (VFB)	See[(1)]	See[(1)]	1	Very sensitive node. Increased resistance introduces gain error.
cvideo_tvout (TVOUT)	See[(1)]	See[(1)]	14	Increased resistance introduces nonlinearity.
vdda_hdmi_vdac (VDDA)	0.08	2.5	-	Low resistance is critical to avoid headroom issues.
vssa_hdmi_vdac (VSSA)	0.08	3	-	Low resistance is critical to avoid headroom issues.
cvideo_rset (RSET)	0.06	1.1	5	Low resistance results in better noise performance.

(1) On-board trace lead to the Video DAC node needs to have a characteristic impedance of 75 Ω.

A.5.1.1 Self Parasitic Requirements

Table A-17. TV-OUT PCB Requirements (Self Parasitics)[(1)]

NODE	R (Ω)	L (nH)	C (pF)	COMMENTS
cvideo_vfb (VFB)	See[(1)]	See[(1)]	1	Very sensitive node. Increased resistance introduces gain error.
cvideo_tvout (TVOUT)	See[(1)]	See[(1)]	14	Increased resistance introduces nonlinearity.
vdda_hdmi_vdac (VDDA)	0.08	2.5	-	Low resistance is critical to avoid headroom issues.
vssa_hdmi_vdac (VSSA)	0.08	3	-	Low resistance is critical to avoid headroom issues.
cvideo_rset (RSET)	0.06	1.1	5	Low resistance results in better noise performance.

(1) On-board trace lead to the TVOUT node needs to have a characteristic impedance of 75 Ω.

A.5.1.2 Mutual Capacitance Requirements

Table A-18. TV-OUT PCB Requirements (Mutual Capacitance)

NODE1	NODE2	CAPACITOR NAME	CAPACITOR VALUE (fF)	COMMENTS
cvideo_rset (RSET)	cvideo_vfb (VFB)	C1	See[(1)]	Maximum total coupling including parasitics from PCB
cvideo_rset (RSET)	cvideo_tvout (TVOUT)	C2	16	Maximum total coupling including parasitics from PCB
cvideo_rset (RSET)	Any other net accept for cvideo_tvout (TVOUT), vdda_hdmi_vdac (VDDA), vssa_hdmi_vdac (VSSA), and cvideo_vfb (VFB)	C3	30	Maximum total coupling including parasitics from PCB

(1) There is some flexibility for budgeting the coupling between RSET and VFB and between RSET and TVOUT since the VFB signal follows the TVOUT signal. C1 or C2 can be greater than 60 fF but the sum of C1 plus C2 must be less than or equal to 120 fF. C3 must be less than or equal to 30 fF even if the sum of C1 plus C2 is less than 120 fF.

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A.5.1.3 Mutual Inductance Requirements

Table A-19. TV-OUT PCB Requirements (Mutual Inductance)(1)

NODE1	NODE2	MUTUAL INDUCTANCE NAME	INDUCTANCE VALUE (nH)	COMMENTS
cvideo_rset (RSET)	cvideo_vfb (VFB)	M1	2.4	Maximum total coupling including parasitics from PCB
cvideo_rset (RSET)	cvideo_tvout (TVOUT)	M2	2.25	Maximum total coupling including parasitics from PCB
cvideo_rset (RSET)	Any other net accept for cvideo_tvout (TVOUT), vdda_hdmi_vdac (VDDA), vssa_hdmi_vdac (VSSA), and cvideo_vfb (VFB)	M3	1.25	Maximum total coupling including parasitics from PCB

(1) It is recommended to shield RSET with VSSA to achieve above requirements for low mutual coupling.

A.5.2 TV-OUT Implementation Proposal

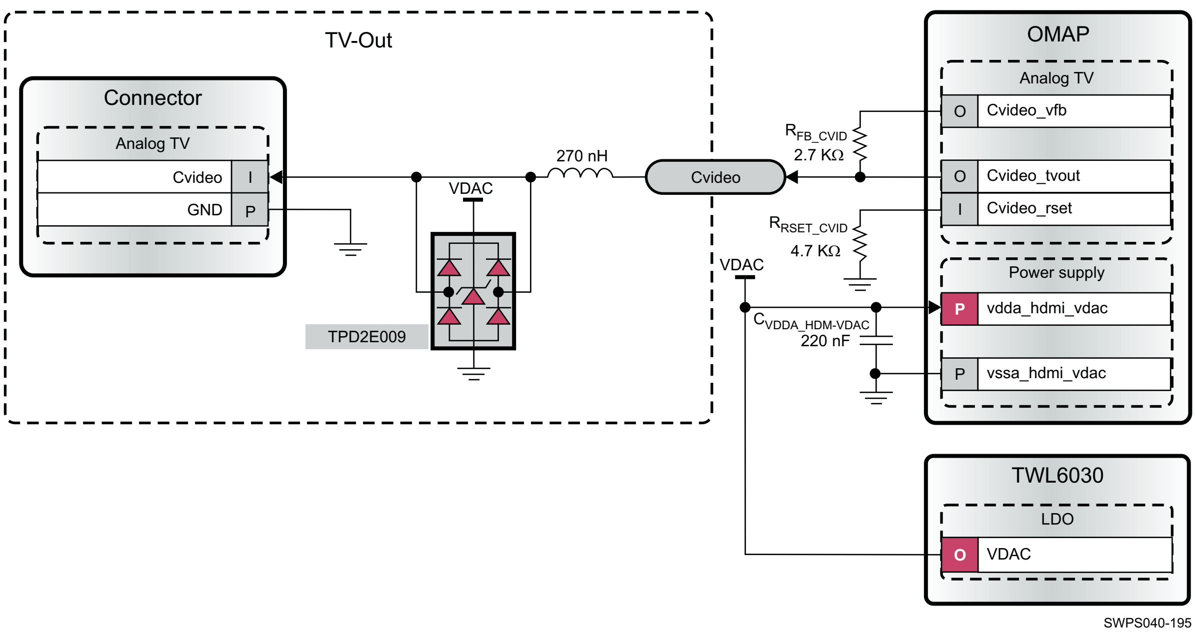

Figure A-34. TV-Out—Full Scale DC-Coupled Interconnections

A.5.3 ESD Implementation—TV-OUT

NOTE

For more information on system ESD, see Section A.2.4, *System ESD Generic Guideline*.

If the ac or dc modes are used, then external ESD protection is required for the TVOUT pin.

The TV-OUT interface has been designed for a maximum application mode ESD strike of 8 kV with an external protection circuit consisting of a series inductor of at least 270 nH with one of its terminals connected to TVOUT and its other terminal connected to an ESD diode clamp.

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It is recommended to use at least two ESD diode clamps in parallel. The TI-TPD2E009 ESD diode clamp is recommended for IEC protection.

NOTE

System level (IEC) ESD results are dependent on the components being connected to the product.

Part numbers that are different than the reference board specification are not assured to meet the system level requirements.

Table A-20. TVOUT Component Reference

	DEVICE	SUPPLIER	PART NUMBER
TVOUT	TVS	TI	TPD2E009DRY
	L		0402/270 nH

A.6 Clock Guidelines

NOTE

For more information on system clocks, see Section 4, *Clock Specifications*.

A.6.1 32-kHz Oscillator Routing

When designing the printed-circuit board:

- Keep the crystal as close as possible to the crystal pins X1 and X2.
- Keep the trace lengths short and small to reduce capacitor loading and prevent unwanted noise pickup.
- Place a guard ring around the crystal and tie the ring to ground to help isolate the crystal from unwanted noise pickup.
- Keep all signals out from beneath the crystal and the X1 and X2 pins to prevent noise coupling.
- Finally, an additional local ground plane on an adjacent PCB layer can be added under the crystal to shield it from unwanted pickup from traces on other layers of the board. This plane must be isolated from the regular PCB ground plane and tied to the GND pin of the RTC. The plane mustn't be any larger than the perimeter of the guard ring. Make sure that this ground plane doesn't contribute to significant capacitance (a few pF) between the signal line and ground on the connections that run from X1 and X2 to the crystal.

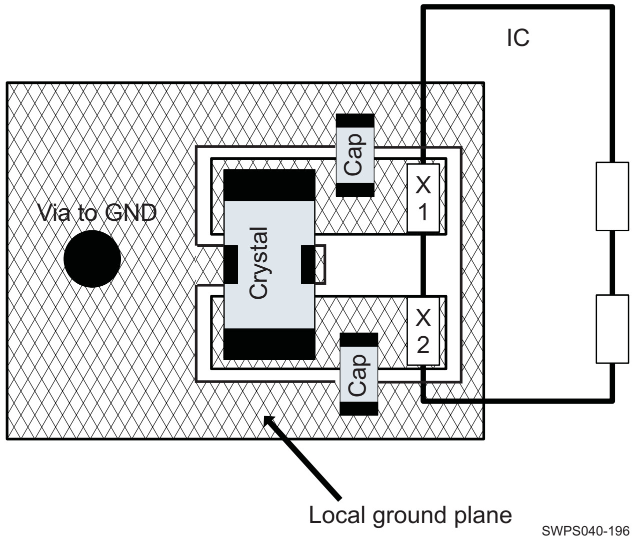

Figure A-35. Slow Clock PCB Requirements

A.6.2 Oscillator Ground Connection

Although the impedance of a ground plane is low it is, of course, not zero. Therefore, any noise current in the ground plane causes a voltage drop in the ground. If the two capacitors of the oscillator are connected directly to the ground plane, the voltage drop in the red portion of the ground in Figure A-36 will be overlaid to the oscillator signals. If the noise related voltage drop is big enough, the oscillator may be disturbed.

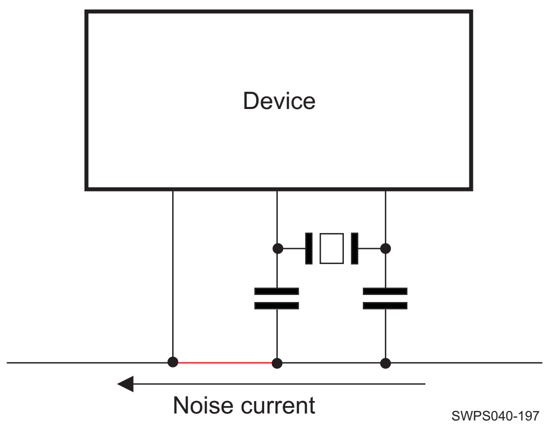

Figure A-36. Poor Oscillator Ground Connection

The overlay of ground noise may be avoided by providing an extra ground trace for the oscillator ground as indicated in green in Figure A-37. Even in a multilayer PCB this is a powerful measure to improve the susceptibility of the oscillator.

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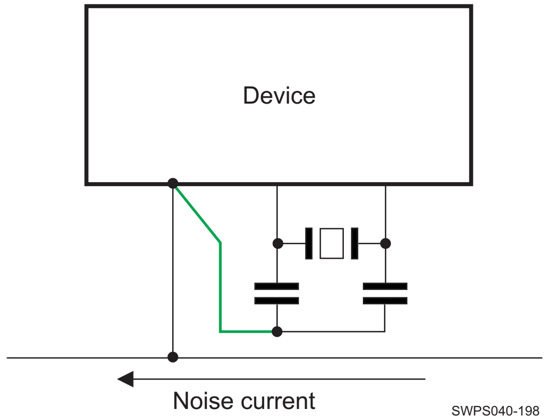

Figure A-37. Optimized Oscillator Ground Connection

A.6.3 Electromagnetic Interference (EMI) Prevention in Clock Distribution

The following section gives a series of guidelines and methods to reduce EMI. Here are some of these methods:

- Place the clock drivers near the center of the PCB rather than at the periphery. A periphery location increases the magnetic dipole moments.
- For clock traces that are routed on the surface plane, to further reduce EMI, it is better to route parallel ground traces on either side of the clock trace. However, it is even better to place the clock traces in the layer in between ground and the Vcc plane.
- Not use right angles or ‘T’ crosses. Right angles increase trace capacitance and also add an impedance discontinuity that effect the signal degradation.
- Impedance must be matched as closely as possible. Usually cases impedance mismatches cause emissions. Signal integrity mainly depends on impedance matching.
- Do not run long clock traces parallel to each other because they affect crosstalk that contributes to EMI.
- It is a good idea to make sure that the spacing between traces is at least equal to the trace width.

A.7 Ground Guidelines

A.7.1 Guard Ring on PCB Edges

The mayor advantage of a multilayer PCB with ground-plane is the ground return path below each and every signal or power trace.

As shown in Figure A-38 the field lines of the signal return to PCB ground as long as an “infinite” ground is available.

Traces near the PCB-edges do not have this “infinite” ground and therefore may radiate more than others. Thus signals (clocks) or power traces (core power) identified to be critical must not be routed in the vicinity of PCB-edges, or, if not avoidable, must be accompanied by a guard ring on the PCB edge.

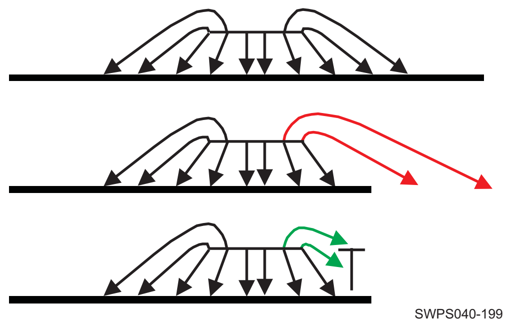

Figure A-38. Field Lines of a Signal Above Ground

Figure A-39. Guard Ring Routing

The intention of the guard ring is that HF-energy, that otherwise would have been emitted from the PCB-edge, is reflected back into the board where it partially will be absorbed. For this purpose ground traces on the borders of all layers (including power layer) must be applied as shown in Figure A-39.

As these traces must have the same (HF–) potential as the ground plane they must be connected to the ground plane at least every 10 mm.

A.7.2 Analog and Digital Ground

For the optimum solution, the AGND and the DGND planes must be connected together at the power supply source in a same point. This ensures that both planes are at the same potential, while the transfer of noise from the digital to the analog domain is minimized.

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B Glossary

B.1 Glossary

AC or ac	Alternating Current
APLL	Analog Phase-Locked Loop
ARM	Advanced RISC Machine
ASIC	Application-Specific Integrated Circuit
BG	Bandgap
BGA	Ball Grid Array
CAM	Parallel Camera Interface
CCP	Compact Camera Port
CDM	Charged Device Modem
cJTAG	Component Joint Test Action Group, IEEE 1149.1 Standard
CM	Clock Manager
CMF	Common Mode Filter
CMOS	Complementary Metal Oxide Silicon
CSI	Camera Serial Interface
DAC	Digital-to-Analog Converter
DC or dc	Direct Current
DDR	Double Data Rate
DISPC	Display Controller
DLL	Delay-Locked Loop
DMA	Direct Memory Access
DMIC	Digital Microphone
DPLL	Digital Phase-Locked Loop
DSI	Display Serial Interface
DSS	Display Subsystem
eFuse	Electrical Fuse
EMC	ElectroMagnetic Compatibility
EMI	ElectroMagnetic Interference
EMIF	External Memory Interface
EMU	Emulation
ESD	Electrostatic Discharge
ESL	Equivalent Series Inductance
ESR	Equivalent series resistance
ETK	Embedded Trace kit
ETM	Embedded Trace Macrocell
FIR	Fast Infrared
FSR	Full-Scale Range
FSUSB	Full-Speed Universal Serial Bus
GP	General-Purpose
GPIN	General-Purpose Input
GPIO	General-Purpose Input Output
GPMC	General-Purpose Memory Controller
HBM	Human Body Model
HDI	High Density Interconnect
HDMI	High-Definition Multimedia Interface
HDQ	High-Speed Data Queue
HDTV	High-Definition Television

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HFSS	High Frequency Structure Simulator
HS	High speed or high security
HSI	High-speed Synchronous Interface
HSUSB	High-Speed Universal Serial Bus
HWDBG	Hardware Debug
HYS	Hysteresis
I^2C	Inter-Integrated Circuit
I2S	Inter IC Sound
IC	Integrated Circuit
ICE	In-Circuit Emulator
IEC	International Electrotechnical Commission (standard organization)
IEEE	Institute of Electrical and Electronics Engineers
IO	Input Output
IR	Infrared
IrDA	Infrared Data Association
IR Drop	I * R Drop or Voltage Drop
ISI	Interference InterSymbol
ISP	Image Sensing Product
ITU	International Telecommunications Union
IVA	Image and Video Accelerator
JEDEC	Joint Electron Device Engineering Council
JPEG	Joint Photographic Experts Group (Image format)
JTAG	Joint Test Action Group, IEEE 1149.1 standard
LCD	Liquid-Crystal Display
LDO	Low Dropout
LJF	Left-Justified Format
LP	Low Power
LVCMOS	Low-Voltage CMOS
LVDS	Low-Voltage Differential Signaling
McBSP	Multichannel Buffered Serial Port
McSPI	Multichannel Serial Port Interface
MIPI®	Mobile Industry Processor Interface (MIPI® is a registered trademark of Mobile Industry Processor (MIPI) Alliance.)
MIR	Medium Infrared
MMC	MultiMedia Card
MPU	Microprocessor Unit
MS-PRO	Memory Stick PRO
NA	Not Applicable
NAND	Not AND (Boolean Logic)
NOR	Not OR (Boolean Logic)
OMAP	Open Multimedia Applications Platform
PBGA	Plastic Ball Grid Array
PCB	Printed Circuit Board
PCM	Pulse Code Modulation
PD	Pull Down
PDM	Pulse Density Modulation
PDN	Power Delivery Network
PHY	Physical Layer Controller
PLL	Phase-Locked Loop
PMIC	Power Management Integrated Circuit

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POP	Package On Package
PTH	Plated Though Holes
PU	Pull Up
QXGA	Quad eXtended Graphics Array
RAW	Raw (Image format)
RFBI	Remote Frame Buffer Interface
RGB	Red Green Blue (Image format)
RMS	Root Mean Square
RX	Receiver / Receive
SAP	TBD
SCL	Serial Clock: programmable serial clock used in the I^2C interface (can be called also SCLK).
SDA	Serial Data: serial data bus in the I^2C interface.
SDI	Serial Display Interface
SDIO	Secure Digital Input Output
SDMMC	Secure Digital MultiMedia Card
SDR	Single Data Rate
SDRAM	Synchronous Dynamic Random Access Memory
SDRC	SDRAM Controller
SDTI	System Debug Trace Interface
SIM	Subscriber Identity Module
SIR	Slow Infrared
SMPS	Switching-Mode Power Supply
SPI	Serial Port Interface
SRAM	Synchronous Random Access Memory
SSI	Synchronous Serial Interface
STN	Super Twist Nematic (LCD Panel)
SYNC	Synchronous
SYS	System
TAP	Test Access Point
TBD	To Be Defined
TDM	Time Division Multiplexing
TFT	Thin Film Transistor (LCD Panel)
TLIS	Transmission Line Interconnect System
TLL	Transceiver-less Link Logic
TX	Transmitter / Transmit
UART	Universal Asynchronous Receiver Transmitter
UI	Unit Interval
ULPI	UTMI Low Pin Interface
USB	Universal Serial Bus
USIM	Universal Subscriber Identity Module
UTMI	USB2.0 Transceiver Macrocell Interface
WKUP	Wake-Up
YUV	Luminance + 2 Chrominance Difference Signals (PAL Y, Cr, Cb) Color Encoding

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